MAPLST0822-002PP

RF Power Field Effect Transistor
LDMOS, 800—2200 MHz, 2W, 28V

4/14/05

Preliminary

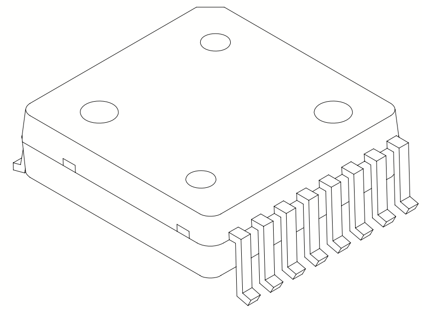
Features

- Designed for broadband commercial applications up to 2.2GHz
- High Gain, High Efficiency and High Linearity
- Ease of Design for Gain and Insertion Phase Flatness
- Excellent Thermal Stability

- W-CDMA Performance at 2.17GHz, 28Vdc
  - Average Output Power: 28dBm @ -39dBc ACPR
  - Gain: 14.5dB (typ.)
  - Efficiency: 23% (typ.)
  - 10:1 VSWR Ruggedness at 2W (CW), 28V, 2.11GHz

- Performance at 960MHz, 26Vdc, P_{1dB}
  - Average Output Power: 2W min.
  - Gain: 20dB (typ.)
  - Efficiency: 50% (typ.)
  - 10:1 VSWR Ruggedness at 2W, 26V, 960MHz

Package Style



PFP-16

Maximum Ratings

Parameter	Symbol	Rating	Units
Drain—Source Voltage	V_{DSS}	65	V_{dc}
Gate—Source Voltage	V_{GS}	+15, -0.5	V_{dc}
Total Power Dissipation @ T_C = 25 °C	P_D	6.9	W
Storage Temperature	T_{STG}	-65 to +150	°C
Junction Temperature	T_J	150	°C

Thermal Characteristics

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\Theta JC}$	18	ºC/W

NOTE—**CAUTION**—MOS devices are susceptible to damage from electrostatic charge. Precautions in handling and packaging MOS devices should be observed.

4/14/05

Preliminary

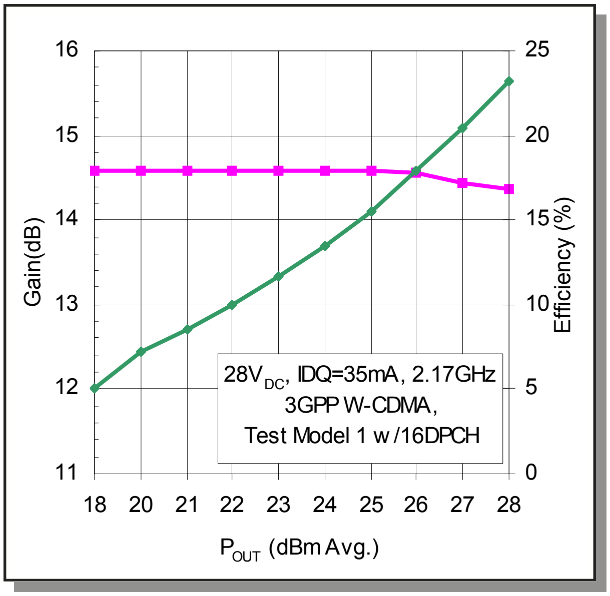
Characteristic	Symbol	Min	Typ	Max	Unit
DC CHARACTERISTICS @ 25ºC					
Drain-Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 30 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Gate Threshold Voltage (V_{ds} = 26 Vdc, I_d = 25 mA)	$V_{GS(th)}$	2	—	5	Vdc
Gate Quiescent Voltage (V_{ds} = 26 Vdc, I_d = 25 mA)	$V_{GS(Q)}$	3	—	5	Vdc
Drain-Source On-Voltage (V_{gs} = 10 Vdc, I_d = 0.1 A)	$V_{DS(on)}$	—	0.30	—	Vdc

Preliminary

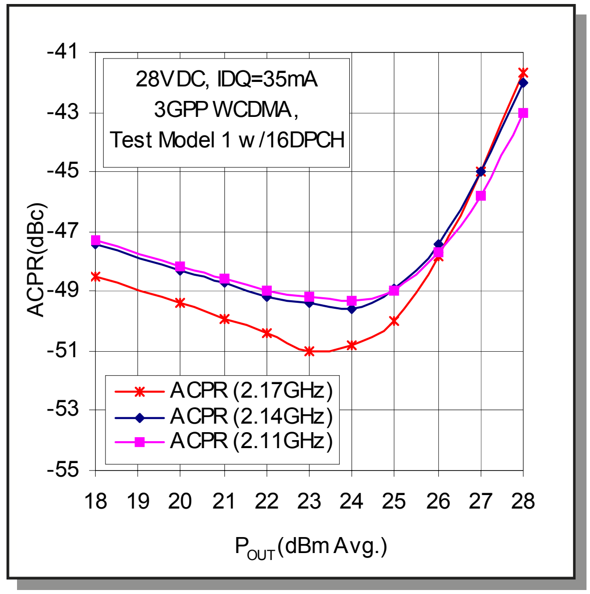
Characteristic	Symbol	Min	Typ	Max	Unit
RF FUNCTIONAL TESTS @ 25ºC (In M/A-COM Test Fixture)					
Common Source Amplifier Gain (V_{DD} = 28 Vdc, I_{DQ} = 35 mA, f = 2170 MHz, P_{OUT} = 2 W)	G_P	—	14	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, I_{DQ} = 35 mA, f = 2170 MHz, P_{OUT} = 2 W)	EFF (η)	—	38	—	%
Input Return Loss (V_{DD} = 28 Vdc, I_{DQ} = 35 mA, f = 2170 MHz, P_{OUT} = 2 W)	IRL	—	-9	—	dB
Output VSWR Tolerance (V_{DD} = 28 Vdc, I_{DQ} = 35 mA, f = 2170 MHz, P_{OUT} = 2 W, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			
RF FUNCTIONAL TESTS @ 25ºC (In M/A-COM Test Fixture shown in Figure 10)					
Common Source Amplifier Gain (V_{DD} = 26 Vdc, I_{DQ} = 35 mA, f = 1900 MHz, P_{OUT} = 2 W)	G_P	—	14.5	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, I_{DQ} = 35 mA, f = 1900 MHz, P_{OUT} = 2 W)	EFF (η)	—	40	—	%
Input Return Loss (V_{DD} = 26 Vdc, I_{DQ} = 35 mA, f = 1900 MHz, P_{OUT} = 2 W)	IRL	—	-10	—	dB
Output VSWR Tolerance (V_{DD} = 26 Vdc, I_{DQ} = 35 mA, f = 1900 MHz, P_{OUT} = 2 W, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			
RF FUNCTIONAL TESTS @ 25ºC (In M/A-COM Test Fixture)					
Common Source Amplifier Gain (V_{DD} = 26 Vdc, I_{DQ} = 35 mA, f = 1670 MHz, P_{OUT} = 2 W)	G_P	—	15	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, I_{DQ} = 35 mA, f = 1670 MHz, P_{OUT} = 2 W)	EFF (η)	—	45	—	%
Input Return Loss (V_{DD} = 26 Vdc, I_{DQ} = 35 mA, f = 1670 MHz, P_{OUT} = 2 W)	IRL	—	-11	—	dB
Output VSWR Tolerance (V_{DD} = 26 Vdc, I_{DQ} = 35 mA, f = 1670 MHz, P_{OUT} = 2 W, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			
RF FUNCTIONAL TESTS @ 25ºC (In M/A-COM Test Fixture shown in Figure 12)					
Common Source Amplifier Gain (V_{DD} = 26 Vdc, I_{DQ} = 50 mA, f = 960 MHz, P_{OUT} = 2 W)	G_P	—	20	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, I_{DQ} = 50 mA, f = 960 MHz, P_{OUT} = 2 W)	EFF (η)	—	50	—	%
Input Return Loss (V_{DD} = 26 Vdc, I_{DQ} = 50 mA, f = 960 MHz, P_{OUT} = 2 W)	IRL	—	-12	—	dB
Output VSWR Tolerance (V_{DD} = 26 Vdc, I_{DQ} = 50 mA, f = 960 MHz, P_{OUT} = 2 W, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

4/14/05

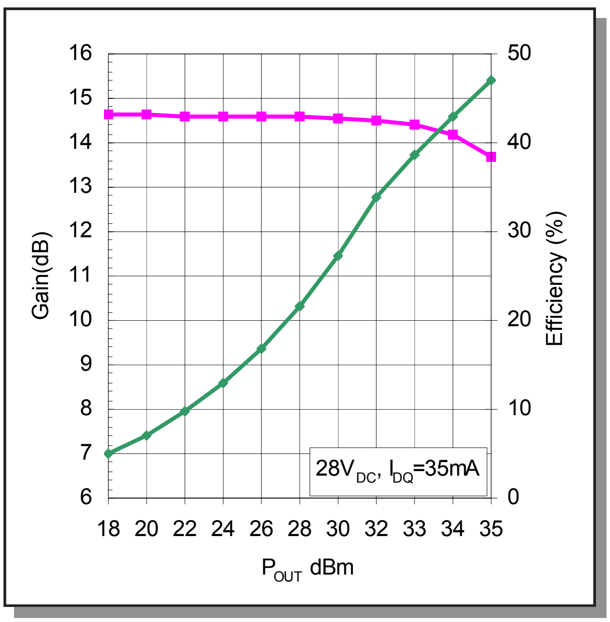
Preliminary



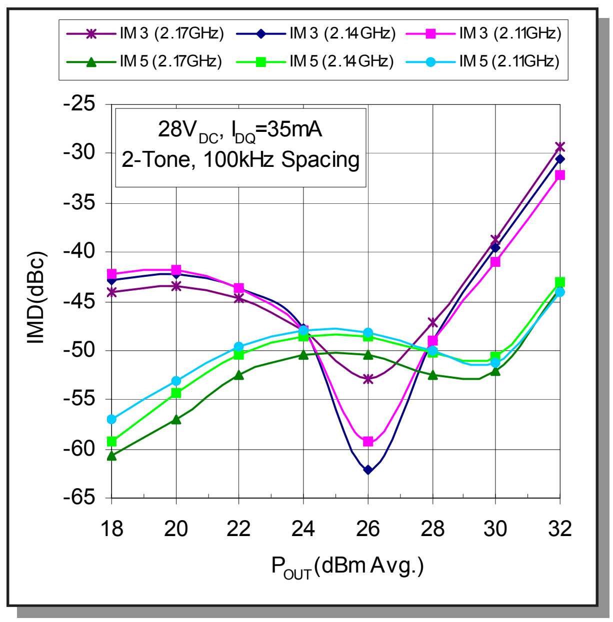
Graph 1. W-CDMA: Gain and Efficiency versus Output Power



Graph 2. W-CDMA: ACPR versus Output Power

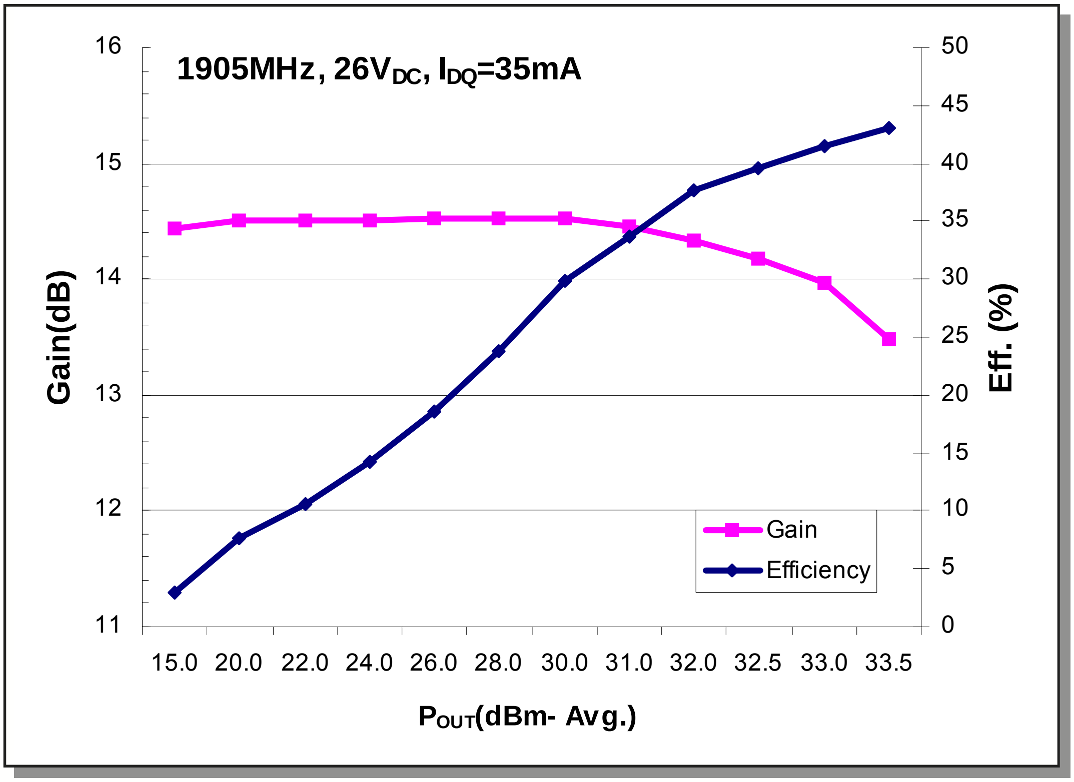


Graph 3. CW: Gain and Efficiency versus Output Power

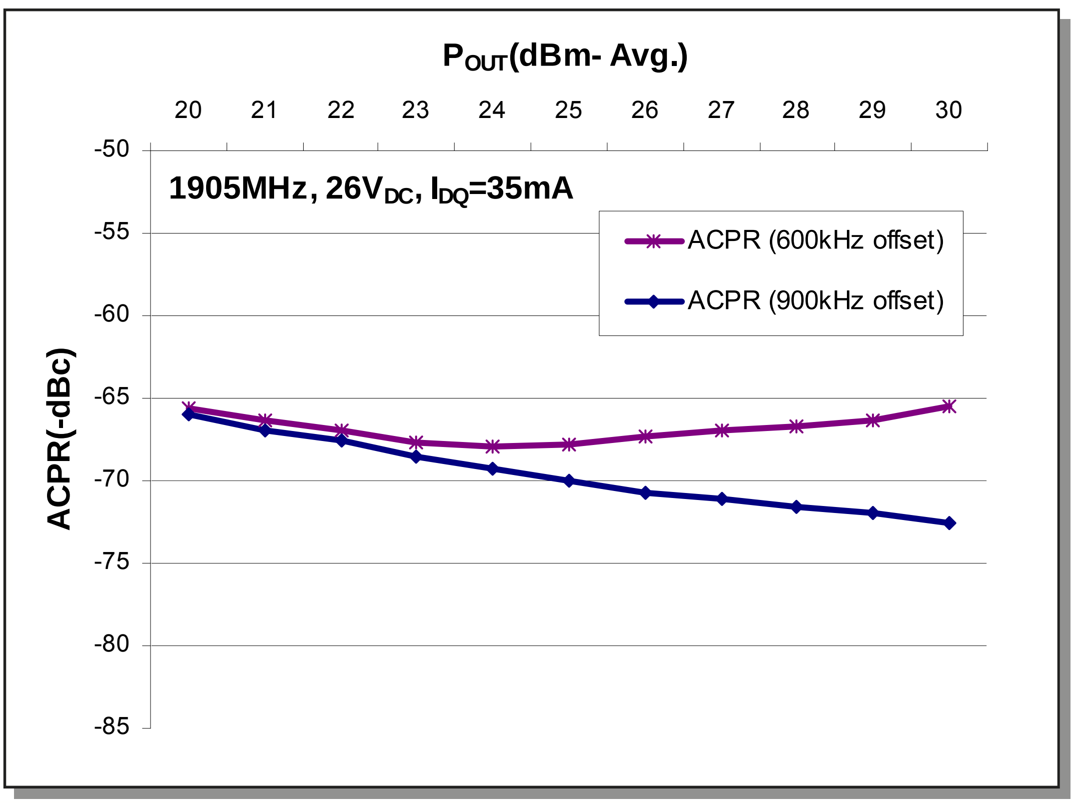


Graph 4. Two Tone: Intermodulation Distortion versus Output Power

Preliminary

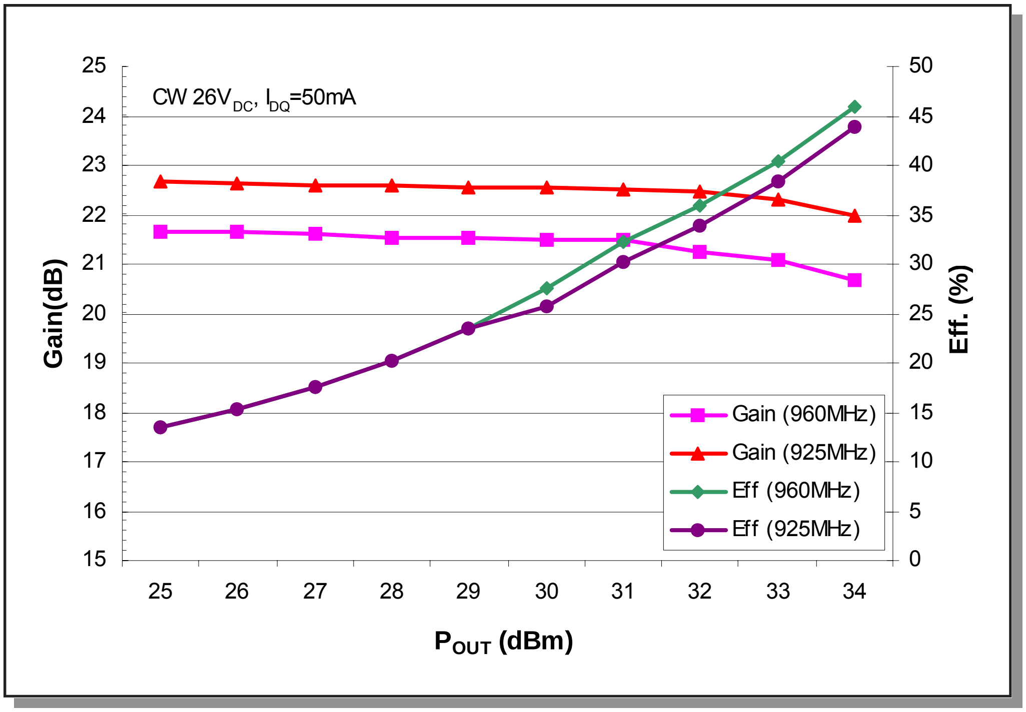


Graph 5. PHS Power Gain and Drain Efficiency vs. Output Power

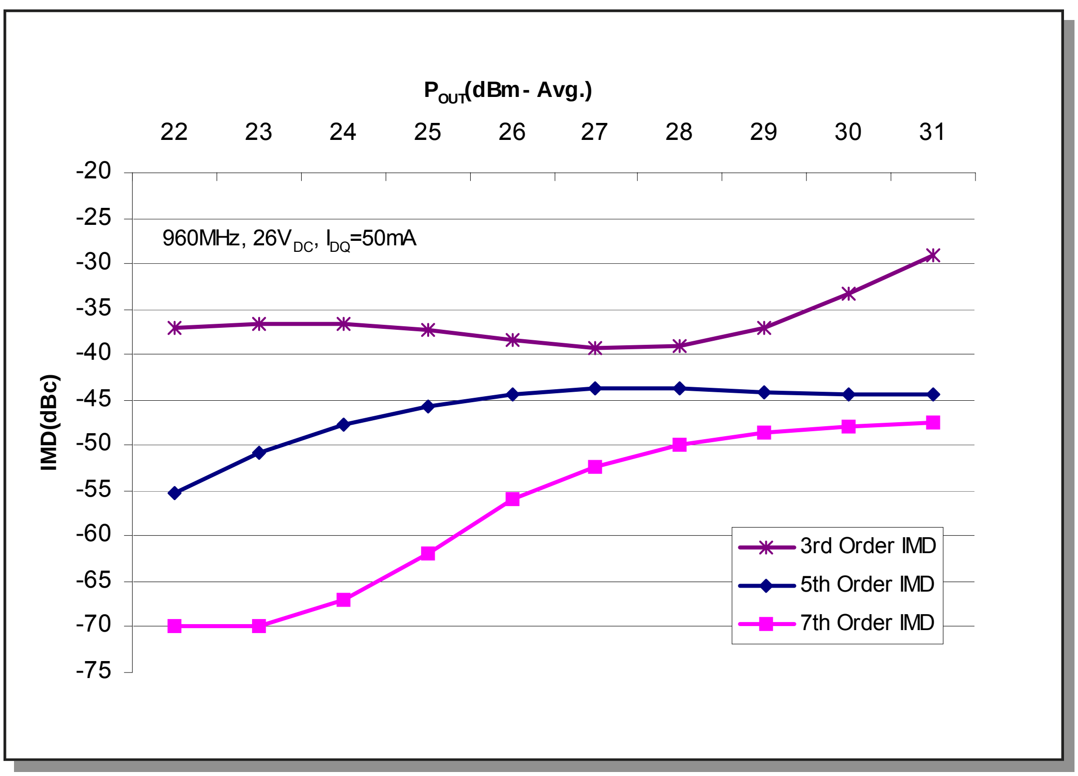


Graph 6. PHS ACPR vs. Output Power

Preliminary

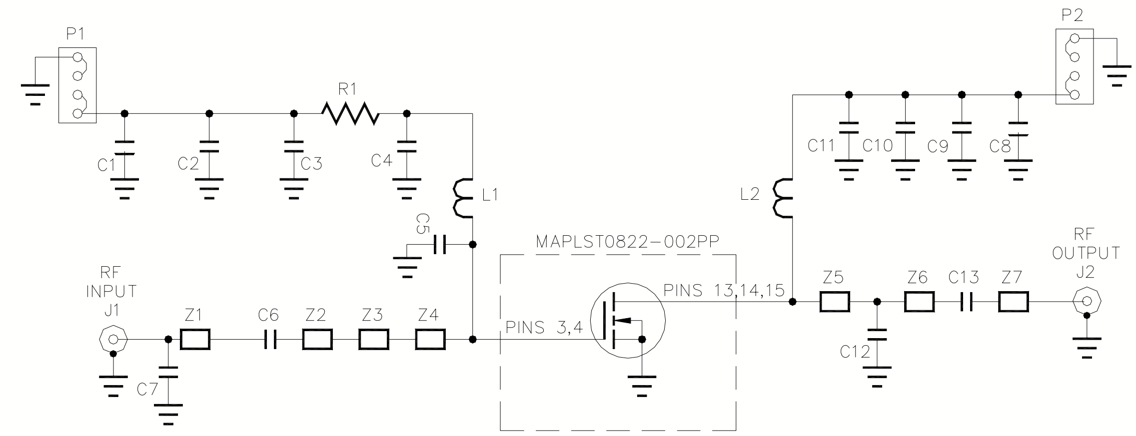


Graph 7. Power Gain and Drain Efficiency vs. Output Power



Graph 8. Intermodulation Distortion vs. Output Power

Preliminary



C1,C8	Tantalum Surface Mt. Cap., 100 µF, 35 V	Z1	Distributed Microstrip Element, 0.040” x 0.046”
C2,C9	Ceramic Chip Capacitor, 0.1 µF	Z2	Distributed Microstrip Element, 0.490” x 0.046”
C3,C10	Ceramic Chip Capacitor, 1000 pF	Z3	Distributed Microstrip Element, 0.180” x 0.026”
C4,C6,C11,C13	Chip Capacitor, 33 pF ATC100A	Z4	Distributed Microstrip Element, 0.135” x 0.100”
C5,C7,C12	Chip Capacitor, 2.7 pF ATC100A	Z5	Distributed Microstrip Element, 0.175” x 0.046”
J1,J2	SMA Connector, Omni Spectra 2052-5636-02	Z6	Distributed Microstrip Element, 1.035” x 0.046”
L1,L2	Inductor, 8 nH, CoilCraft A03T	Z7	Distributed Microstrip Element, 0.125” x 0.046”
P1,P2	Connector, AMP 640457-4		
Q1	Transistor, MAPLST0822-002PP	PC Board Rogers (RO4350) Duroid, 0.020:” thick,	
R1	Chip Resistor (0805), 100 Ohm		Er=3.5, 1 Oz Copper Both Sides

Figure 9. 1880—1920 MHz Test Fixture Schematic

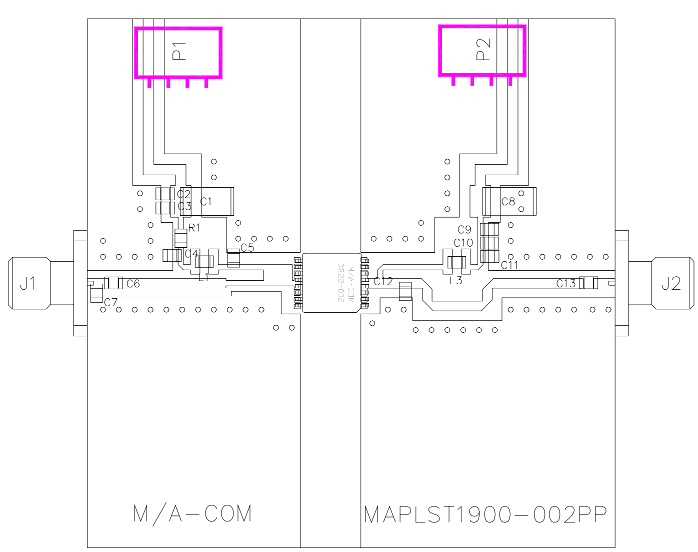
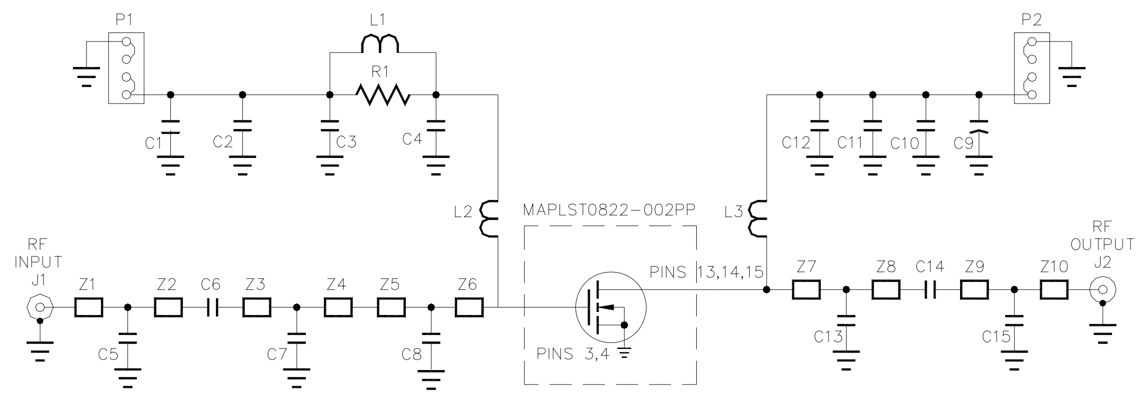


Figure 10. 1880—1920 MHz Test Fixture Component Layout



C1,C9	Tantalum Surface Mt. Cap., 100 µF, 35 V
C2,C10	Ceramic Chip Capacitor, 0.1 µF
C3,C11	Ceramic Chip Capacitor, 1000 pF
C4,C6,C12,C14	Chip Capacitor, 33 pF ATC100A
C5,C7,C15	Chip Capacitor, 2.7 pF ATC100A
C8,C13	Chip Capacitor, 1.2 pF ATC100A
J1,J2	SMA Connector, Omni Spectra 2052-5636-02
L1,L2,L3	Inductor, 8 nH, CoilCraft A03T
P1,P2	Connector, AMP 640457-4
Q1	Transistor, MAPLST0822-002PP
R1	Chip Resistor (0805), 100 Ohm

Z1	Distributed Microstrip Element, 0.050” x 0.046”
Z2	Distributed Microstrip Element, 0.050” x 0.046”
Z3	Distributed Microstrip Element, 0.235” x 0.046”
Z4	Distributed Microstrip Element, 0.273” x 0.046”
Z5	Distributed Microstrip Element, 0.105” x 0.026”
Z6	Distributed Microstrip Element, 0.229” x 0.026”
Z7	Distributed Microstrip Element, 1.036” x 0.046”
Z8	Distributed Microstrip Element, 0.180” x 0.046”
Z9	Distributed Microstrip Element, 0.050” x 0.046”
Z10	Distributed Microstrip Element, 0.050” x 0.046”

PC Board Rogers (RO4350) Duroid, 0.020:” thick,
Er=3.5, 1 Oz Copper Both Sides

Figure 11. 920—960 MHz Test Fixture Schematic

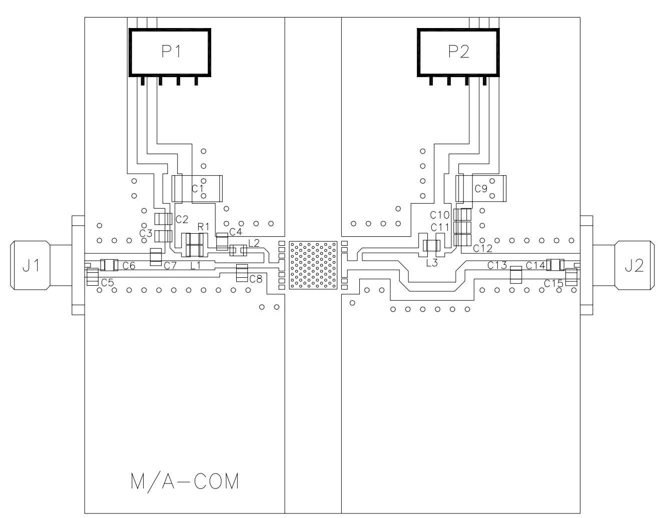


Figure 12. 920—960 MHz Test Fixture Component Layout

Preliminary

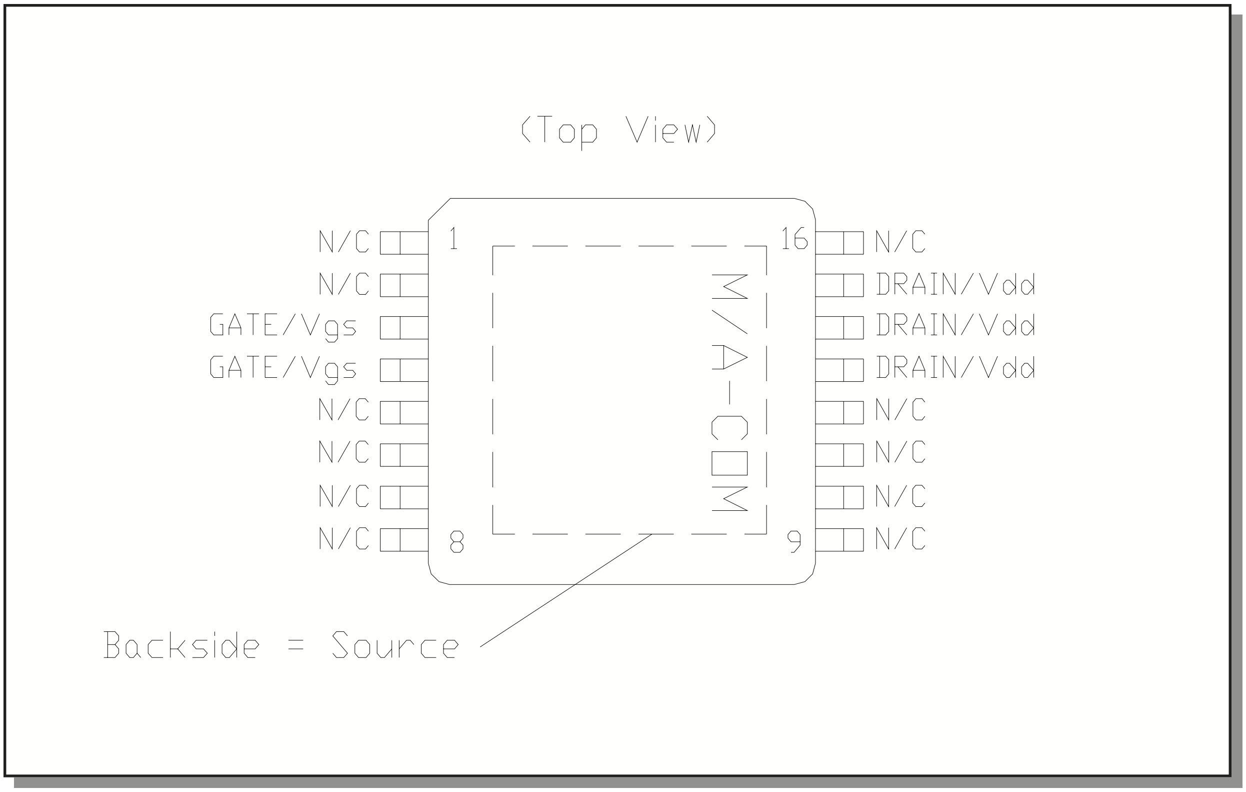
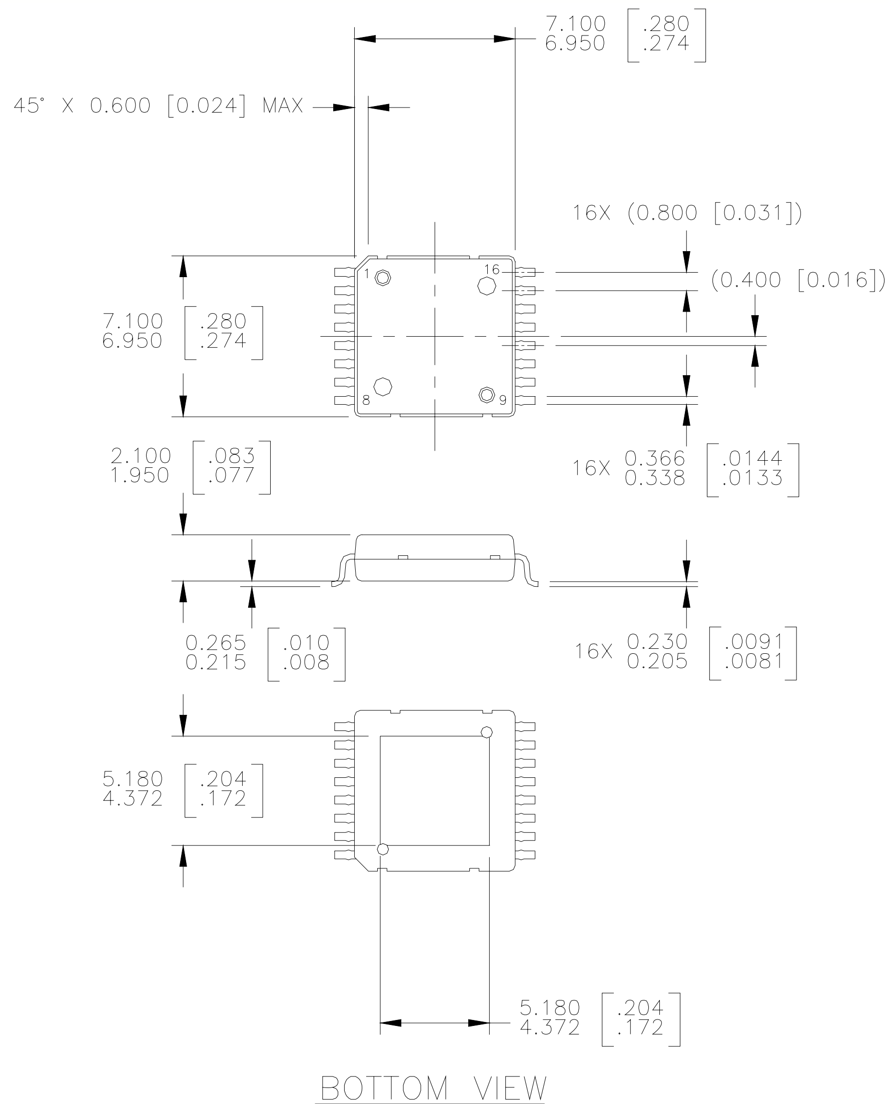


Figure 13. PFP-16 Pin Connections

Package Dimensions



- **North America:** Tel. (800) 366-2266
- **Asia/Pacific:** Tel.+81-44-844-8296, Fax +81-44-844-8298
- **Europe:** Tel. +44 (1344) 869 595, Fax+44 (1344) 300 020