3.3V CMOS 20-BIT BUFFERS

IDT74FCT163827A/B/C

Integrated Device Technology, Inc.

FEATURES:

- 0.5 MICRON CMOS Technology
- **Typical tsκ(o) (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015;
  > 200V using machine model (C = 200pF, R = 0)
- Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP and 15.7 mil pitch TVSOP
- Extended commercial range of -40°C to +85°C
- V_{CC} = 3.3V ±0.3V, Normal Range or
  V_{CC} = 2.7 to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

DESCRIPTION:

The FCT163827A/B/C 20-bit buffers are built using advanced dual metal CMOS technology. These 20-bit bus drivers provide high-performance bus interface buffering for wide data/address paths or busses carrying parity. Two pairs of NAND-ed output enable controls offer maximum control flexibility and are organized to operate the device as two 10-bit buffers or one 20-bit buffer. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT163827A/B/C have series current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors.

The inputs of the FCT163827A/B/C can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V supply system.

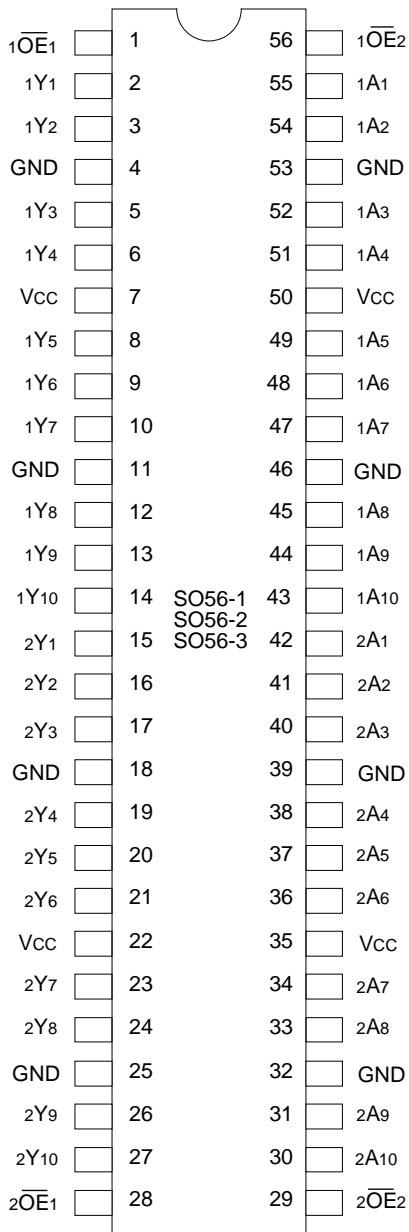## FUNCTIONAL BLOCK DIAGRAM

TO 9 OTHER CHANNELS

3083 drw 01

TO 9 OTHER CHANNELS
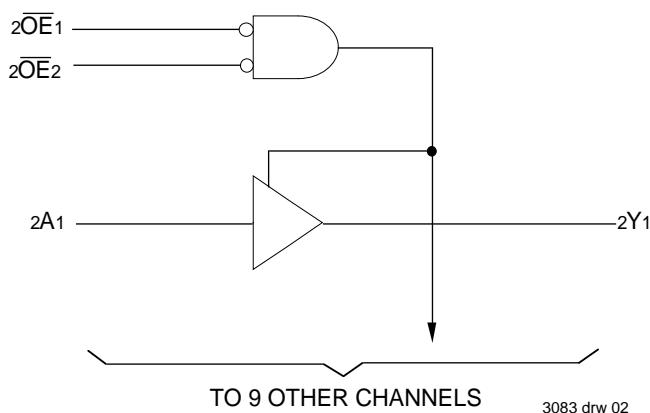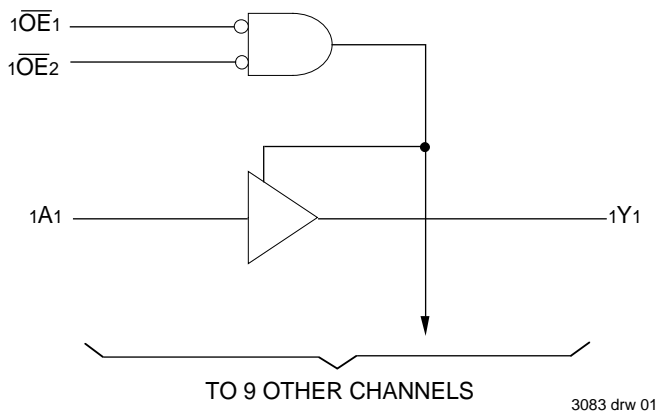
3083 drw 02

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COMMERCIAL TEMPERATURE RANGE

AUGUST 1996

DSC-3083/3

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PIN CONFIGURATIONS

$1\overline{OE}_1$	1	56	$1\overline{OE}_2$
$1Y_1$	2	55	$1A_1$
$1Y_2$	3	54	$1A_2$
GND	4	53	GND
$1Y_3$	5	52	$1A_3$
$1Y_4$	6	51	$1A_4$
V_{CC}	7	50	V_{CC}
$1Y_5$	8	49	$1A_5$
$1Y_6$	9	48	$1A_6$
$1Y_7$	10	47	$1A_7$
GND	11	46	GND
$1Y_8$	12	45	$1A_8$
$1Y_9$	13	44	$1A_9$
$1Y_{10}$	14	43	$1A_{10}$
$2Y_1$	15	42	$2A_1$
$2Y_2$	16	41	$2A_2$
$2Y_3$	17	40	$2A_3$
GND	18	39	GND
$2Y_4$	19	38	$2A_4$
$2Y_5$	20	37	$2A_5$
$2Y_6$	21	36	$2A_6$
V_{CC}	22	35	V_{CC}
$2Y_7$	23	34	$2A_7$
$2Y_8$	24	33	$2A_8$
GND	25	32	GND
$2Y_9$	26	31	$2A_9$
$2Y_{10}$	27	30	$2A_{10}$
$2\overline{OE}_1$	28	29	$2\overline{OE}_2$

SO56-1
SO56-2
SO56-3

**SSOP/
TSSOP/TVSOP
TOP VIEW**

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PIN DESCRIPTION

Pin Names	Description
$x\overline{OE}x$	Output Enable Inputs (Active LOW)
xAx	Data Inputs
xYx	3-State Outputs

3083 tbl 01

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Description	Max.	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	−0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	−0.5 to V_{CC} + 0.5	V
T_{STG}	Storage Temperature	−65 to +150	°C
I_{OUT}	DC Output Current	−60 to +60	mA

NOTES: 3083 lnk 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RAT-
   INGS may cause permanent damage to the device. This is a stress rating
   only and functional operation of the device at these or any other conditions
   above those indicated in the operational sections of this specification is
   not implied. Exposure to absolute maximum rating conditions for ex-
   tended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

FUNCTION TABLE[1]

Inputs			Outputs
$x\overline{OE}_1$	$x\overline{OE}_2$	xAx	xYx
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

NOTE: 3083 tbl 02
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8.0	pF

NOTE: 3083 lnk 04
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3.0	—	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8mA	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.55	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.50	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.1	10	µA

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} –0.6V at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max.	V_{IN} = V_{CC} −0.6V[3]	—	2.0	30	μA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}_1$ = $x\overline{OE}_2$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	50	75	μA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	0.5	0.7	mA
		50% Duty Cycle $x\overline{OE}_1$ = $x\overline{OE}_2$ = GND One Bit Toggling	V_{IN} = V_{CC} −0.6V V_{IN} = GND	—	0.5	0.8	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz	V_{IN} = V_{CC} V_{IN} = GND	—	2.5	3.7[5]	
		50% Duty Cycle $x\overline{OE}_1$ = $x\overline{OE}_2$ = GND Twenty Bits Toggling	V_{IN} = V_{CC} −0.6V V_{IN} = GND	—	2.5	4.1[5]	

NOTES: 3083 tbl 06

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula.   These limits are guaranteed but not tested.
6. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
   I_C = I_{CC} + ΔI_{CC} $D_H N_T$ + I_{CCD} ($f_{CP} N_{CP}$/2 + $f_i N_i$)
   I_{CC} = Quiescent Current ($I_{CCL,}$ I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[4]

| Symbol	Parameter	Conditions[1]	FCT163827A Min.[2]	FCT163827A Max.	FCT163827B Min.[2]	FCT163827B Max.	FCT163827C Min.[2]	FCT163827C Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay xAx to xYx	$C_L = 50pF$ $R_L = 500\Omega$	1.5	8.0	1.5	5.0	1.5	4.4	ns
		$C_L = 300pF$[4] $R_L = 500\Omega$	1.5	15.0	1.5	13.0	1.5	10.0	
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$x to xYx	$C_L = 50pF$ $R_L = 500\Omega$	1.5	12.0	1.5	8.0	1.5	7.0	ns
		$C_L = 300pF$[4] $R_L = 500\Omega$	1.5	23.0	1.5	15.0	1.5	14.0	
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$x to xYx	$C_L = 5pF$[4] $R_L = 500\Omega$	1.5	9.0	1.5	6.0	1.5	5.7	ns
		$C_L = 50pF$ $R_L = 500\Omega$	1.5	10.0	1.5	7.0	1.5	6.0	
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	ns

3083 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. Propagation Delays and Enable/Disable times are with $V_{CC} = 3.3V \pm 0.3V$, Normal Range. For $V_{CC} = 2.7V$ to $3.6V$, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

TEST CIRCUITS AND WAVEFORMS

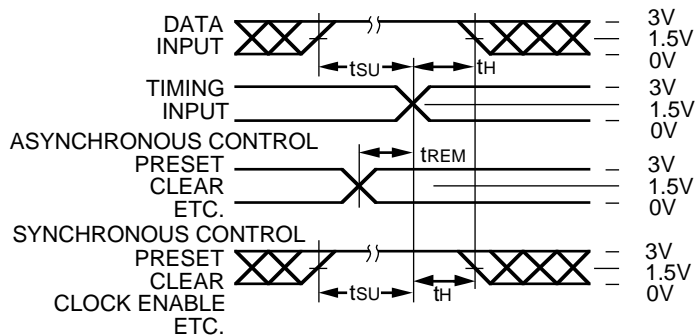## TEST CIRCUITS FOR ALL OUTPUTS
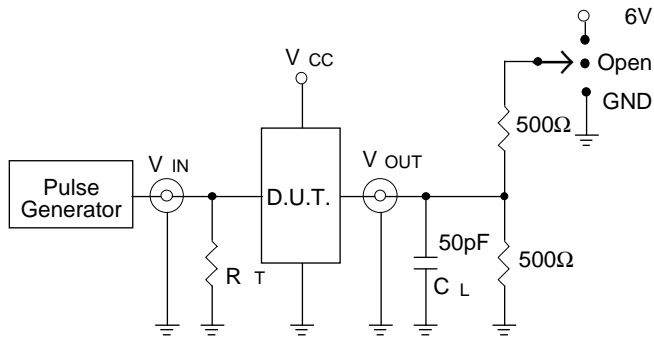
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SWITCH POSITION

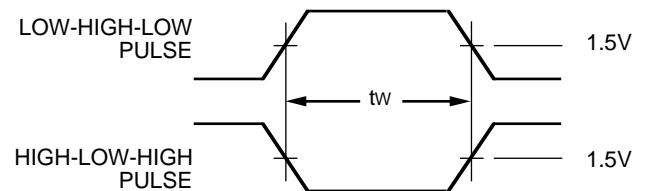| Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.
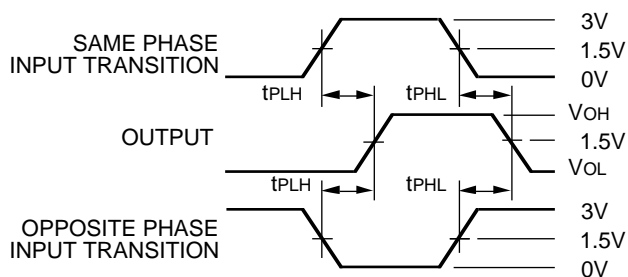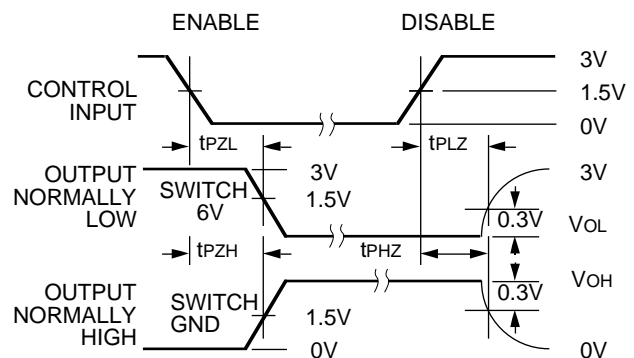
SET-UP, HOLD AND RELEASE TIMES

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PULSE WIDTH

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PROPAGATION DELAY
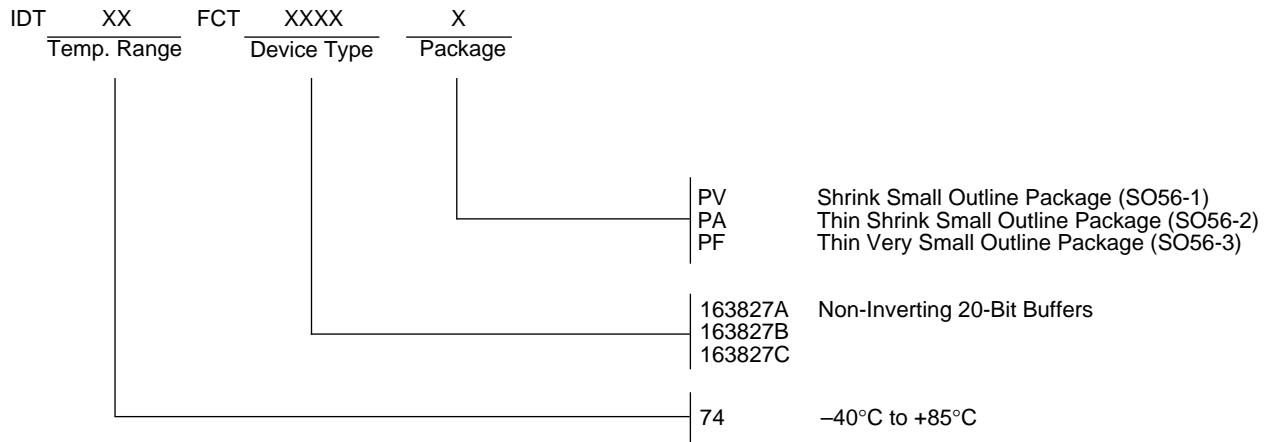

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ENABLE AND DISABLE TIMES

3083 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate $\leq$ 1.0MHz; $t_F \leq$ 2.5ns; $t_R \leq$ 2.5ns.
3. If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC}.

ORDERING INFORMATION

IDT   XX   FCT   XXXX   X

Temp. Range   Device Type   Package

PV	Shrink Small Outline Package (SO56-1)
PA	Thin Shrink Small Outline Package (SO56-2)
PF	Thin Very Small Outline Package (SO56-3)

163827A	Non-Inverting 20-Bit Buffers
163827B	
163827C	

74	−40°C to +85°C

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