## Features

- **Smart Card Interface**
  - **Compliance with Standards**
    - **ISO/IEC 7816-1, 2, 3 and 4**
    - **EMV V96**
    - **CB**
    - **Mondex®, Proton, ZKA, Other: Contact Gemplus®**
  - **Supported Smart Cards**
    - **Number of Smart Cards Supported: 1**
    - **Asynchronous Cards: T=0 and T=1**
    - **Synchronous/Memory Cards Using a Command Interpreter**
    - **EMV or Non EMV Cards**
- **Electrical Interface**
  - **Transmission Speed: 9.6 Kbps to 115 Kbps**
  - **Card Power Supply: 1.8V/3V/5V**
  - **ESD Protection On Card Pins: 4 KV - Human Body Model**
  - **Card Presence or Insertion Detection**
  - **Short Circuit Current Limitation**
- **Host Interface**
  - **Physical Layer**
    - **Serial Asynchronous Link**
    - **Programmable Transmission Speed From 1,200 bps to 115,200 bps**
    - **Format: 8 bits, No Parity, 1 Stop Bit**
    - **Adjustable Signal Voltage**
  - **Protocol**
    - **Gemplus Block Protocol (GBP)**
    - **GBP Interface Library Kit Source Code**
- **Chip Power Supply**
  - **Voltage: V_{CC}- 2.85V to 5.4V**
  - **Consumption: 8 mA Typical, 150 mA Max - Smart Card Powered**
  - **Power Down Mode**
    - **100 µA Max Power Down Current**
    - **Power-down/Power-up by Host Command**
- **Additional Features**
  - **Operating Temperature Range: 0°C to +70°C (-40°C to +85°C)**
  - **Package: SS0P24**
  - **LED Management: The LED is On When the Card is Powered On**

Description

AT83C21GC is designed to simplify the integration of smart card interfaces in electronic devices.

It manages the electrical interface and communication with ISO 7816 –1/2/3/4 compatible smart cards and memory cards.

Figure 1. Basic Architecture of a Smart Card Reader
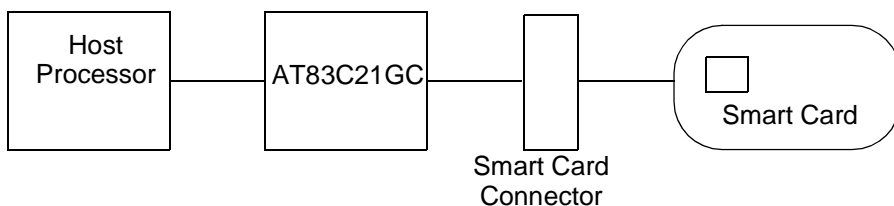
The connection with the host processor is achieved via a serial asynchronous link; the rate can be selected from a range from 1200 to 115,200 bps.

The software inside the GemCore chip handles a communication protocol with the host system called the Gemplus Block Protocol (GBP).

A complete set of documentation is available on the Gemplus web site: http://www.gemplus.com.

A GBP Interface Library Kit can be provided, upon request. It consists of the source code of the GBP communication layer between the host and GemCore. It is written in the C language. See the Gemplus developers' site at www.gemplus.com. Enquiries can also be posted to cardreader@atmel.com.

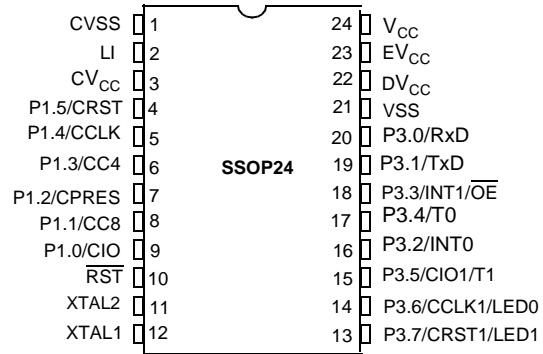## Pin Description

Figure 2. 24-pin SSOP Pinout

Table 1. Port Signal Description

Port	Signal Name	Internal Power Supply	ESD	Type	Description
P1.0	CIO	CV_{CC}	4 kV	I/O	**Smart Card Interface Function** Card I/O – Pull-up medium is lower than 20KΩ
P1.1	CC8	CV_{CC}	4 kV	I/O	**Smart Card Interface Function** Card contact 8 – Pull-up medium must be less than 20KΩ
P1.2	CPRES	V_{CC}	4 kV	I	**Smart Card Interface Function** Card presence
P1.3	CC4	CV_{CC}	4 kV	I/O	**Smart Card Interface Function** Card contact 4 – Pull-up medium must be less than 20KΩ
P1.4	CCLK	CV_{CC}	4 kV	O	**Smart Card Interface Function** Card clock
P1.5	CRST	CV_{CC}	4 kV	O	**Smart Card Interface Function** Card reset – Pull-up medium must be less than 20KΩ
P3.0	RxD	EV_{CC}		I	**UART Function** Receive data input
P3.1	TxD	EV_{CC}		O	**UART Function** Transmit data output.
P3.2	INT0	DV_{CC}		I/O	**Input/Output Function** P3.2 is a bi-directional I/O port with internal pull-ups.
P3.3	INT1	EV_{CC}		I/O	**Input/Output Function** P3.3 is a bi-directional I/O port with internal pull-ups.
P3.4		EV_{CC}		I/O	**Input/Output Function** P3.4 is a bi-directional I/O port with internal pull-ups.
P3.5	CIO1	DV_{CC}		I/O	**Alternate Card Function** Card I/O: Pull-up medium must be less than 20K

Table 1. Port Signal Description (Continued)

Port	Signal Name	Internal Power Supply	ESD	Type	Description
P3.6	CCLK1	DV_{CC}		O	**LED function** These pins can be directly connected to the cathode of the standard LED without external current limiting resistors. The typical current of each output can be programmed by software to 2, 4 or 10 mA (LEDCON register).
P3.7	CRST1	DV_{CC}		I/O	**Input/Output Function** P3.7 is a bi-directional I/O port with internal pull-ups.
RST		V_{CC}		I/O	**Reset Input** Holding this pin low for 64 oscillator periods while the oscillatoris running resets the device. The Port pins are driven to their reset conditions when a voltage lower than V_{IL} is applied, whether or not the oscillator is running. This pin has an internal pull-up resistor which allows the device to be reset by connecting a capacitor between this pin and VSS. Asserting $\overline{RST}$ when the chip is in Idle mode or Power-down mode returns the chip to normal operation. The output is active for at least 12 oscillator periods when an internal reset occurs.
XTAL1		V_{CC}		I	**Input to the on-chip Inverting Oscillator Amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin.
XTAL2		V_{CC}		O	**Output of the on-chip Inverting Oscillator Amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, XTAL2 may be left unconnected.
V_{CC}				PWR	**Supply Voltage** V_{CC} is used to power the internal voltage regulators and internal I/O's.
LI				PWR	**DC/DC Input** LI must be tied to V_{CC} through an external coil (typically 4, 7 μH) and provide the current for the pump charge of the DC/DC converter.
CV_{CC}				PWR	**Card Supply Voltage** CV_{CC} is the programmable voltage output for the Card interface. It must be connected to an external decoupling capacitor.
DV_{CC}				PWR	**Digital Supply Voltage** DV_{CC} is used to supply the digital core and internal I/Os. It is internally connected to the output of a 3V regulator and must be connected to an external decoupling capacitor.
EV_{CC}		V_{CC}		PWR	**Extra Supply Voltage** EV_{CC} is used to supply the level shifters of UART interface I/O pins. It must be connected to an external decoupling capacitor. This reference voltage is generated internally (automatically or not), or it can be connected to an external voltage reference.
CVSS				GND	**DC/DC Ground** CVSS is used to sink high shunt currents from the external coil.
VSS				GND	**Ground**

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