

# Measuring HEXFET<sup>®</sup> Characteristics

(HEXFET is the trademark for International Rectifier Power MOSFETs)

## Topics covered:

- *Converting the nomenclature from bipolars to MOSFETs*
- *P-Channel HEXFET Power MOSFETs*
- *Initial settings*
- *Breakdown*
- *Drain leakage*
- *Gate threshold*
- *Gate leakage*
- *Transconductance*
- *On-resistance*
- *Diode drop*
- *Characteristics in synchronous rectification*
- *Transfer characteristics*
- *Measurements without a curve tracer*
- *Device capacitances*
- *Switching times*
- *Gate charge*
- *Reverse recovery*
- *A fixture to speed-up testing time*
- *Related topics*

## 1. General

Curve tracers have generally been designed for making measurements on bipolar transistors. While power MOSFETs can be tested satisfactorily on most curve tracers, the controls of these instruments are generally labeled with reference to bipolar transistors, and the procedure to follow in the case of MOSFETs is not immediately obvious. This application note describes methods for measuring HEXFET Power MOSFET characteristics, both with a curve tracer and with special-purpose test circuits. Testing HEXFET Power MOSFETs on a curve tracer is a simple matter, provided the broad correspondence between bipolar transistor and HEXFET Power MOSFET features are borne in mind. Table 1 matches some features of HEXFET Power MOSFETs with their bipolar counterparts. The HEXFET Power MOSFET used in all the examples is the IRF630. The control settings given in the examples are those suitable for the IRF630. The user must modify these values appropriately when testing a different device. The IRF630 was selected since it is a typical mid-range device with a voltage rating of 200 volts and a continuous current rating of 9 amps (with  $T_C = 25^\circ\text{C}$ ). For measurements with currents above 20 amps, or for pulsed tests not controlled by the gate, the Tektronix 176 Pulsed High Current Fixture must be used instead of the standard test fixture.

The IRF630 is an N-channel device. For a P-channel device, all the test procedures are the same except that the position of the Polarity Selector Switch must be reversed—that is, for P-channel devices, it must be in the PNP position.

The curve tracer used as an example in this application note is a Tektronix 576, since this instrument is in widespread use. However, the principles involved apply equally well to other makes and models. Figure 1 shows the layout of the controls of the Tektronix 576 curve tracer, with major controls identified by the names used in this application note. Throughout this application note, when controls are referred to, the name of the control is printed in capitals. For all tests, when the power is on, the initial state of the curve tracer is assumed to be as follows:

- LEFT/ RIGHT switch in “off” position
- VARIABLE COLLECTOR SUPPLY at zero
- DISPLAY not inverted
- DISPLAY OFFSET set at zero
- STEP/OFFSET POLARITY button OUT (not inverted)
- VERT/HORIZ DISPLAY MAGNIFIER set at NORM (OFF)
- The REP button of the STEP FAMILY selector should be IN
- The AID button of the OFFSET selector should be IN

- The NORM button of the RATE SELECTOR should be IN

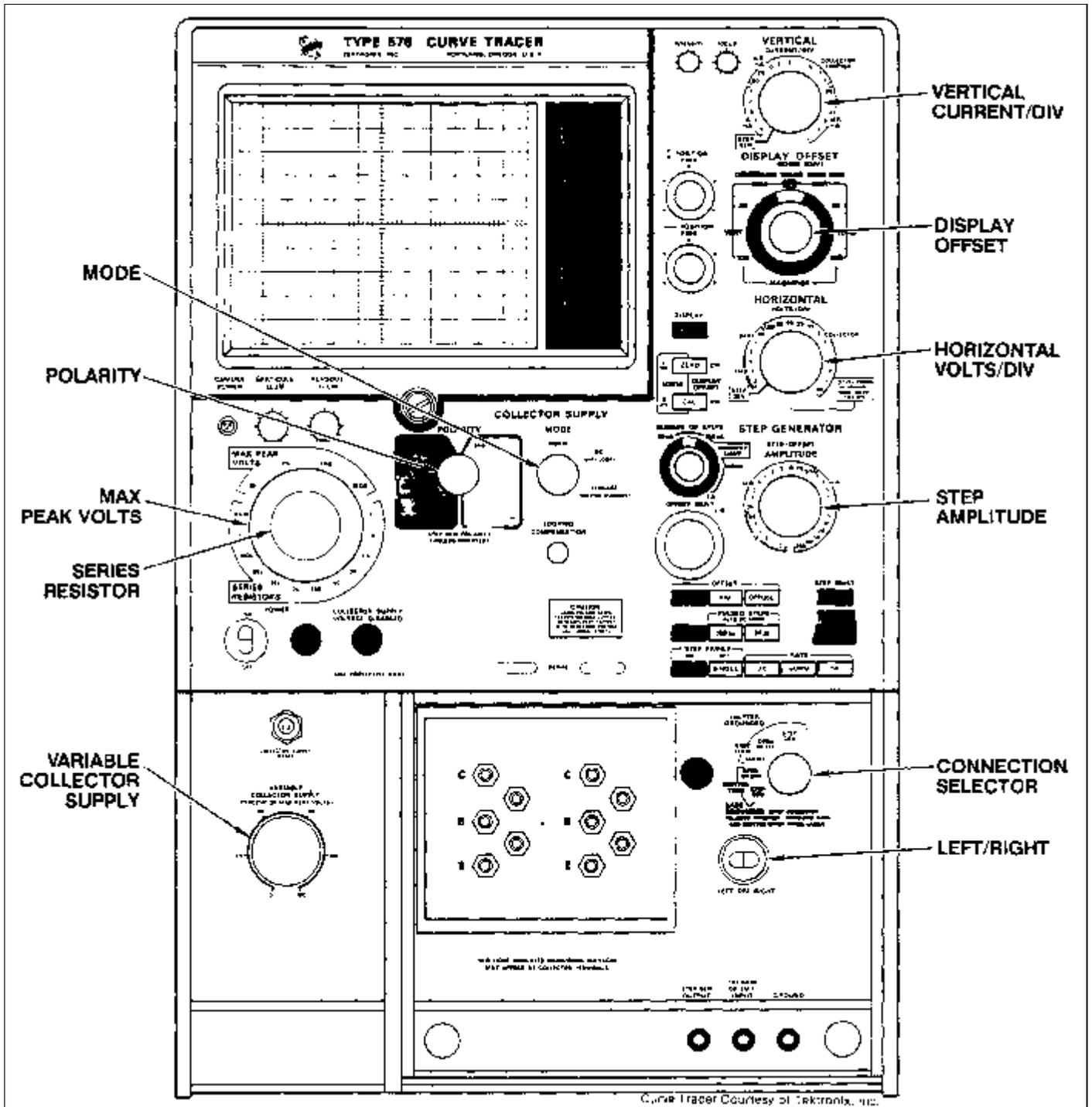


Figure 1. Location of controls in a 576 curve tracer

The accuracy of all tests is predicated on the correct use of the Kelvin connections, as indicated in the instructions for the curve tracer. This is particularly important for power semiconductors, as inductive and resistive drops across sockets and wiring are significant.

Some tests require the use of high voltages. After the device is mounted in the test fixture as described for each test, the test fixture safety cover should be closed and the curve tracer manufacturer's safety warnings heeded. The exposed metal parts of many HEXFET Power MOSFETs (for example, the tab of TO-220 devices) are connected to the drain and are therefore at the potential of the collector supply.

As with any semiconductor device, some of the characteristics of HEXFET Power MOSFETs are temperature dependent. For tests in which there is significant heating of the HEXFET Power MOSFET, a low repetition rate should be used. For tests involving a slow transition through the linear region, a damping resistor of at least 10 ohms should be connected in series with the gate, close to the gate lead to prevent oscillations. If frequent testing of MOS-gated devices is expected, the use of a test fixture that plugs directly into the curve tracer would save a significant amount time. Such a fixture is described in Section 12. MOS-gated transistors are static sensitive. Wrist straps, grounding mats and other ESD precautions must be followed, as indicated in INT-955.

## 2. $BV_{DSS}$

This is the drain-source breakdown voltage (with  $V_{GS} = 0$ ).  $BV_{DSS}$  should be greater than or equal to the rated voltage of the device, at the specified leakage current.

1. Connect the device as follows: drain to "C", gate to "B", source to "E".
2. Set the MAX PEAK VOLTS to 350V.
3. Set the SERIES RESISTOR to limit the avalanche current to a safe value (i.e., tens of milliamps). A suitable value in this case would be 14 kOhms.
4. Set the POLARITY switch to NPN.
5. The MODE control should be set to NORM.
6. HORIZONTAL VOLTS/DIV should be set at 50 volts/div on the "collector" range.
7. VERTICAL CURRENT/DIV should be set at 50 microA/div.
8. On the plug-in fixture, the CONNECTION SELECTOR should be set to "SHORT" in the "EMITTER GROUNDED" sector. This action grounds the gate and disables the step generator.
9. Connect the device using the LEFT/RIGHT switch. Increase the collector supply voltage using the VARIABLE COLLECTOR SUPPLY control until the current (as indicated by the trace on the screen) reaches 250 microA. (See Figure 2.) Read  $BV_{DSS}$  from the screen.

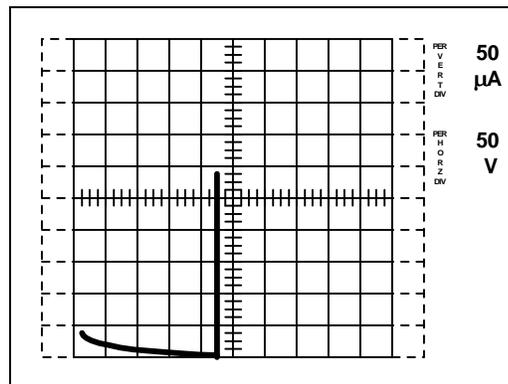


Figure 2. Drain-source breakdown voltage

## 3. $I_{DSS}$

This is the drain current for a drain-source voltage of 100% of rated voltage, with  $V_{GS} = 0$ . This measurement is made in the same manner as  $BV_{DSS}$ , except that:

1. The MODE switch is set to "LEAKAGE".
2. Connect the device using the LEFT/RIGHT switch and adjust the collector supply voltage to the rated voltage of the HEXFET Power MOSFET (200V for the IRF630). Read the value of  $I_{DSS}$  from the display (see Figure 3). The vertical sensitivity may need altering to obtain an appropriately sized display. Often  $I_{DSS}$  will be in the nanoamp range and the current observed will be capacitor currents due to minute variations in collector supply voltage.

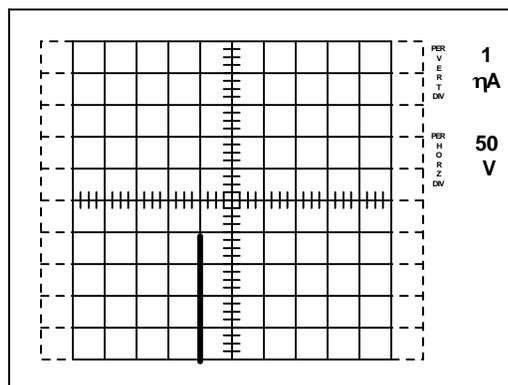


Figure 3. Drain-source leakage current

## 4. $V_{GS(th)}$

This is the gate-source voltage which produces 250 microA of drain current ( $V_{DS} = V_{GS}$ ). At this gate-source voltage the device enters the active region. In circuits where devices are connected in parallel, switching losses can be minimized by using devices with closely matched threshold voltages. This test requires the gate to be connected to the drain and conducted as follows:

1. Connect the device as follows: source to "E", gate to "B", drain to "C". This connection arrangement may require the construction of a special test fixture. Bending of the device leads can cause mechanical stress which results in the failure of the device.

2. Set the MAX PEAK VOLTS to 15V.
3. Set the SERIES RESISTOR to 0.3 ohms.
4. Set POLARITY to PNP. This causes the drain (collector) terminal to be negative with respect to the source (emitter) terminal.
5. Set the MODE CONTROL to NORM.
6. Set the VERTICAL CURRENT/DIV to 50 microA/div.
7. Set the HORIZONTAL VOLTS/DIV to 500 mV/div.
8. Set the CONNECTION SELECTOR to "SHORT" in the "EMITTER GROUNDED" sector.
9. DISPLAY should be inverted.
10. Connect the device using the LEFT/ RIGHT switch. Increase the VARIABLE COLLECTOR VOLTAGE until the drain current reaches 250 microA as indicated by the trace on the screen. Read the voltage on the horizontal center line (since this line corresponds to  $I_D = 250 \text{ mA}$ ) (see Figure 4).

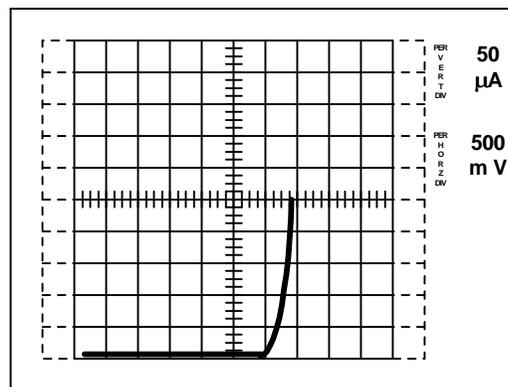


Figure 4. Gate-source threshold voltage

### 5. $I_{GSS}$

This is the gate-source leakage current with the drain connected to the source. An excessive amount of gate leakage current indicates gate oxide damage.

1. The device is connected as follows: gate to "C", drain to "B", source to "E". This is not the usual connection sequence, and a special test fixture will be required if bending of the leads is to be avoided.
2. Set MAX PEAK VOLTS to 75V.
3. Set the SERIES RESISTOR to a low value (for example, 6.5 ohms).
4. Set POLARITY to NPN.
5. Set the MODE switch to LEAKAGE.
6. Set the CONNECTION SELECTOR to the "SHORT" position in the "EMITTER GROUNDED" sector.
7. HORIZONTAL VOLTS/DIV should be set at 5V/div.
8. VERTICAL CURRENT/DIV should be set to an appropriately low range.
9. Connect the device using the LEFT/RIGHT switch. Increase the collector supply voltage using the VARIABLE COLLECTOR SUPPLY control, but do not exceed 20V, the maximum allowable gate voltage. It may be necessary to adjust the vertical sensitivity. Read the leakage current from the display (see Figure 5). In many cases, the leakage current will be in the nanoamp range, in which case the trace will be dominated by currents which flow through the device capacitance as a result of minute fluctuations in the collector supply voltage.
10. The above procedure is for determining gate leakage current with a positive gate voltage. To make the same measurement using a negative voltage, reduce the VARIABLE COLLECTOR SUPPLY voltage to zero, change the POLARITY switch to the PNP position, and reapply the voltage (see Figure 6). The trace will take time to settle because of the gate-source capacitance.

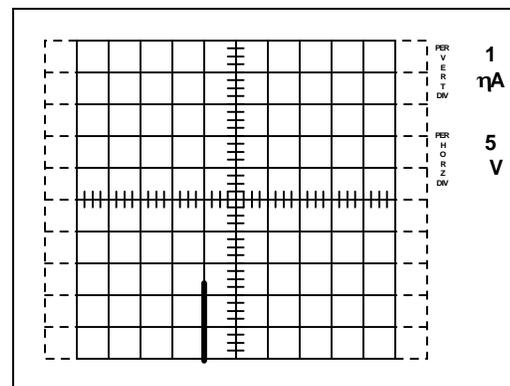


Figure 5. Gate-source leakage current at +20 V

### 6. $g_{fs}$

This is the forward transconductance of the device at a specified value of  $I_D$ .  $g_{fs}$  represents the signal gain (drain current divided by gate voltage) in the linear region. This parameter should be measured with a small ac superimposed on a gate bias and the curve tracer is not the appropriate tool for this measurement. Even with specific test equipment, as indicated in Section 11, the dc bias tends to overheat the MOSFET very rapidly and care should be exercised to insure that the pulse is suitably short.

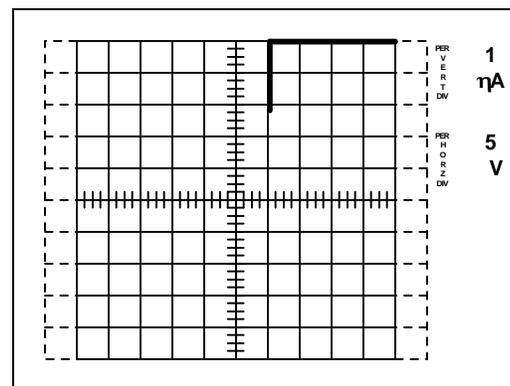


Figure 6. Gate-source leakage current at -20 V

## 7. $R_{DS(on)}$

This is the drain-source resistance at 25°C with  $V_{GS} = 10V$ . Since  $R_{DS(on)}$  is temperature-dependent, it is important to minimize heating of the junction during the test. A pulse test is therefore used to measure this parameter. The test is set up in the following manner:

1. Connect the device as follows: gate to "B", drain to "C", source to "E".
2. Set the MAX PEAK VOLTS to 15 V.
3. Set the SERIES RESISTOR to 0.3 Ohms.
4. The POLARITY switch should be set to NPN.
5. The MODE switch should be set to "NORM".
6. Set the STEP AMPLITUDE to 1V.
7. Set NUMBER OF STEPS to 10.
8. Set OFFSET MULT to 0.
9. The CURRENT LIMIT should be set to 500 mA.
10. The STEP MULTIPLIER button should be OUT—that is, 0.1X not selected.
11. On the PULSED STEPS selector, the 80 microsec button should be IN (or the 300 microsec, if the 80 is not available).
12. On the RATE selector, the 0.5X button should be IN.
13. Set VERTICAL CURRENT/DIV at 1 amp/div (IRF630). This scale should be chosen according to the on-resistance of the device being tested
14. Set the CONNECTION SELECTOR to the "STEP GEN" position in the "EMITTER GROUNDED" sector.
15. Connect the device using the LEFT/RIGHT switch and raise the VARIABLE COLLECTOR SUPPLY voltage until the desired value of drain current is obtained.  $R_{DS(on)}$  is obtained from the trace by reading the peak values of current and voltage (see Figures 7 and 8).

$$R_{DS(on)} = V_{DS}/I_D$$

Logic level devices would have different settings for 6, 7 and 8 so that the on-resistance is measured at the specified gate voltage

## 8. $V_{SD}$

This is the source-drain voltage at rated current with  $V_{GS} = 0$ . It is the forward voltage drop of the body-drain diode when carrying rated current. If pulsed mode testing is required, use high current test fixture.

1. Connect the device as follows: gate to "B", drain to "C", source to "E".
2. Set the MAX PEAK VOLTS to 15V.
3. Set the SERIES RESISTOR at 1.4 ohms or a value sufficiently low that rated current can be obtained.
4. Set POLARITY to PNP.
5. Set MODE to "NORM".
6. The 80 microsec button of the PULSED STEPS selector should be IN (or the 300 microsec, if the 80 is not available).
7. The CONNECTION SELECTOR should be set to the "SHORT" position in the "EMITTER GROUNDED" sector.
8. HORIZONTAL VOLTS/DIV should be on 200 mV/div.
9. VERTICAL CURRENT DIV should be on 1 amp/div.
10. The DISPLAY button should be set to invert.

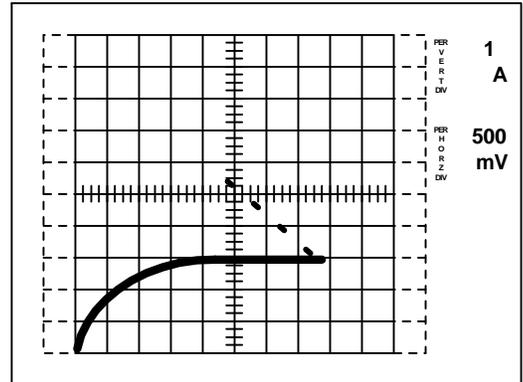


Figure 7. Drain-source resistance, pulsed mode

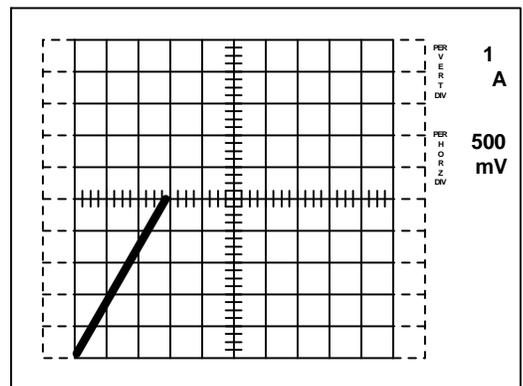


Figure 8. Drain-source resistance

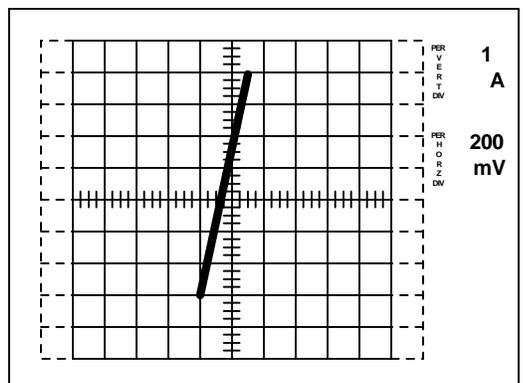


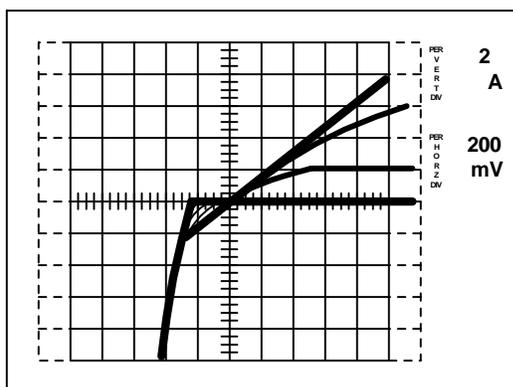
Figure 9. Source-drain voltage (diode)

11. The device is connected using the LEFT/RIGHT switch. Increase the VARIABLE COLLECTOR SUPPLY voltage until rated current is reached (9A for the IRF630). Read  $V_{SD}$  from the trace (see Figure 9).

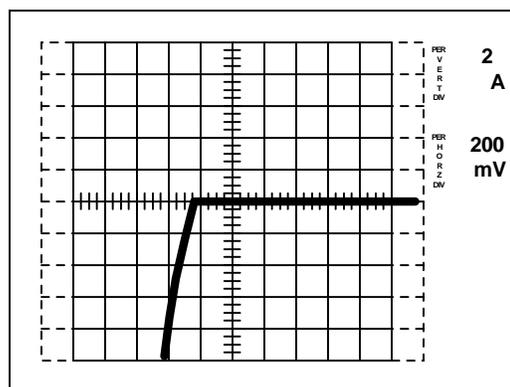
## 9. Composite Characteristics

The forward and reverse characteristics of the HEXFET Power MOSFET may be viewed at the same time. This display can be used to obtain an appreciation of the HEXFET Power MOSFET's behavior in applications in which current flows in the channel in either direction, such as synchronous rectifiers and analog waveform switching. The procedure is the same as for on-resistance except that:

1. OFFSET is set to zero.
2. The POLARITY control is set at "AC".
3. The device is connected using the LEFT/RIGHT switch. The VARIABLE COLLECTOR SUPPLY voltage is increased to obtain the required peak value of  $I_D$ . Beware of device heating. Figure 10 shows the trace obtained with the IRF630. To obtain the reverse characteristics of the diode alone, invert the step polarity. The FET is inoperative, and the display will resemble that shown in Figure 11. The step polarity should also be inverted to obtain the composite characteristics of P-channel devices.



**Figure 10.** Operation in first and third quadrant (synchronous rectification)

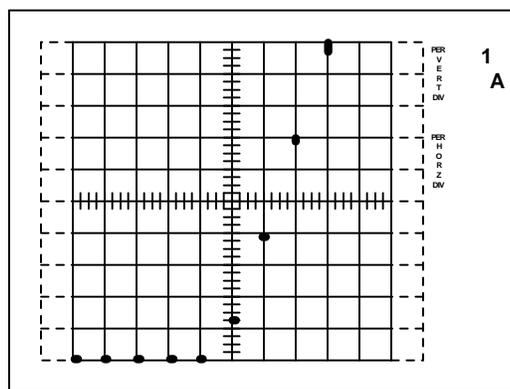


**Figure 11.** Operation in first and third quadrant without gate drive

## 10. Transfer Characteristics

The transfer characteristic curve of  $I_D$  versus  $V_{GS}$  may be displayed using the pulse mode. The test is set up in the same manner as the on-resistance test, except for the following:

1. OFFSET MULTIPLY should be set at zero.
2. Set HORIZONTAL VOLTS/DIV on "STEP GEN".
3. The 300 microsec button of the PULSED STEP SELECTOR should be IN.
4. Increase the VARIABLE COLLECTOR SUPPLY voltage to obtain the trace shown in Figure 12. The transfer characteristic is outlined by the displayed points.



**Figure 12.** Transfer characteristic ( $I_D$  vs  $V_{GS}$ )

## 11. Measurement Of HEXFET Power Mosfet Characteristics Without A Curve Tracer

HEXFET Power MOSFET parameters can be measured using standard laboratory equipment. Test circuits and procedures for doing this are described in the following sections, with the IRF630 used as an example. the test arrangement should be varied appropriately for other devices.

### $BV_{DSS}$ , Drain-Source Breakdown Voltage

The test circuit is shown in Figure 13. The current source will typically consist of a power supply with an output voltage capability of about 3 times  $BV_{DSS}$  in series with a current defining resistor of the appropriate value.

When testing high voltage HEXFET Power MOSFETs it may not be practical or safe to use a supply of 3 times  $BV_{DSS}$ . In such cases, another type of constant current source may be used.

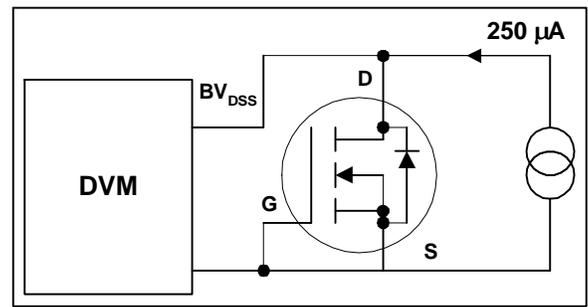


Figure 13. Test circuit for  $BV_{DSS}$

### $V_{GS(th)}$ , Threshold Voltage

The test circuit is shown in Figure 14. The 1 kohm gate resistor is required to suppress potentially destructive oscillations at the gate. the current source may be derived from a voltage source equal to the gate voltage rating of the HEXFET Power MOSFET and a series resistor.

### $V_{DS(on)}$ , On-Resistance

The test circuit is shown in Figure 15. The pulse width should be 300 microsec at a duty cycle of less than 2%.

The value quoted is at a junction temperature of 25°C.  $R_{DS(on)}$  is calculated by dividing  $V_{DS(on)}$  by  $I_D$ . Connect the ground of the gate supply as close to the source lead as possible.

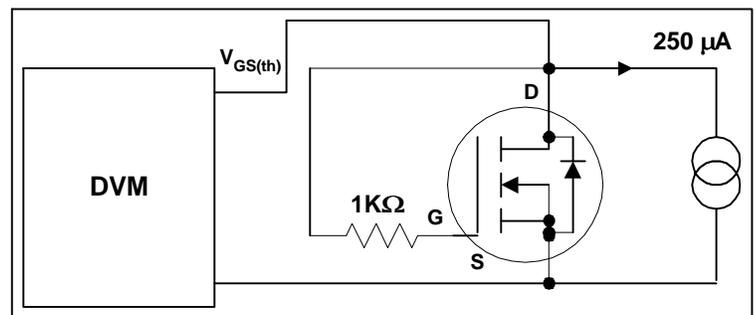


Figure 14. Test circuit for gate threshold voltage

### $g_{fs}$ , Transconductance

Connect a 50V power supply between the device drain and source, as shown in Figure 16. Use a current probe to measure  $I_D$ .

A signal generator operating at low duty cycle to prevent heating of the device, is used to obtain 80 microsec pulses of the required voltage ( $V_{GS}$ ) to obtain the following currents:

$0.015 \times I_D$ ,  $0.05 \times I_D$ ,  $0.15 \times I_D$ ,  $0.5 \times I_D$ , and  $1.5 \times I_D$  where  $I_D$  is the rated value at  $T_C = 25^\circ\text{C}$ . Plot a graph of  $V_{GS}$  versus  $I_D$ .

The transconductance is equal to the slope o

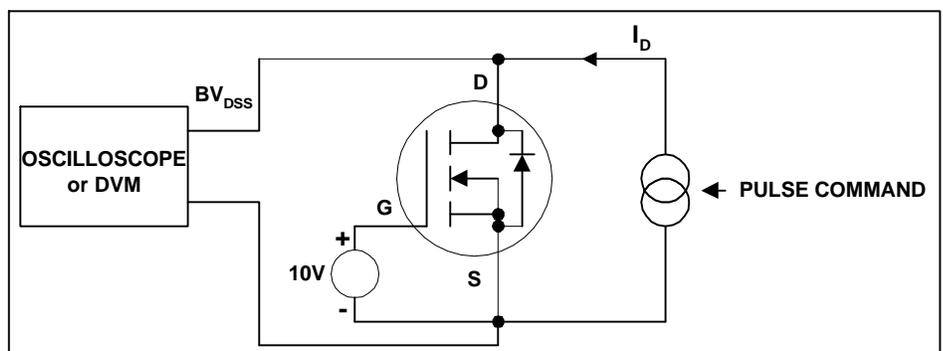


Figure 15. Test circuit for drain on-state voltage

### $C_{iss}$ , $C_{oss}$ , and $C_{rss}$ Output, Input and Reverse Transfer Capacitances

A 1 MHz capacitance bridge is used for all these tests. The capacitance to be measured is connected in series with a capacitance of known value to provide dc isolation. If  $C_u$  is the unknown capacitance,  $C_k$  is the known capacitance, and  $C_m$  is the measured capacitance, then  $C_u$  can be calculated as follows:

$$C_u = \frac{C_k C_m}{C_k - C_m} \quad (1)$$

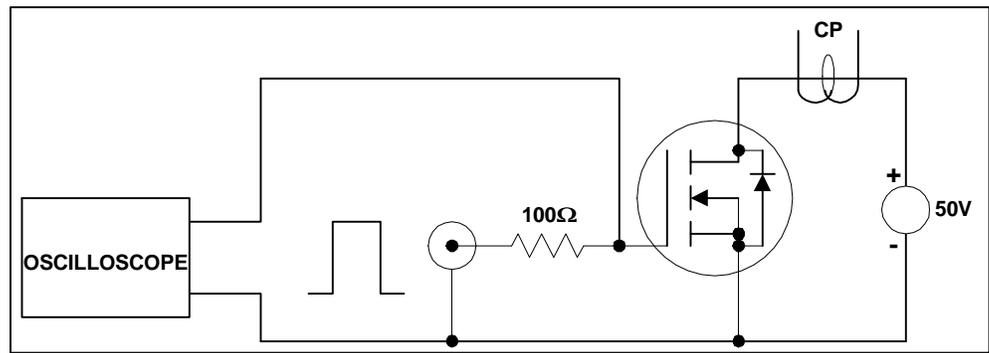


Figure 16. Test circuit for transconductance

Figures 17, 18 and 19 show the circuit connections for the three capacitances that characterize power MOSFETs.

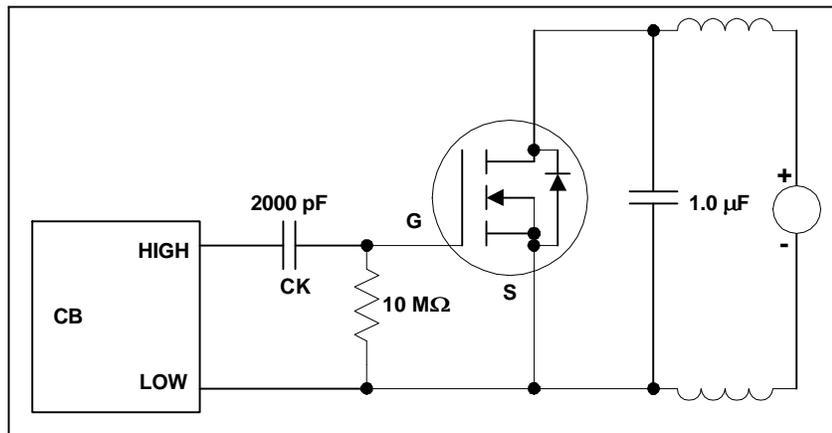


Figure 17. Test circuit for input capacitance

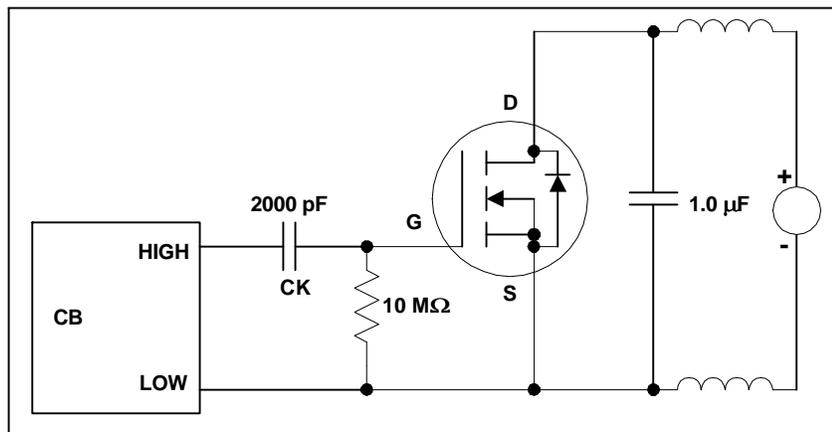


Figure 18. Test circuit for output capacitance

### Turn-on Delay Time, Rise Time, Turn-Off Delay Time, Fall Time

Data sheet values are for a resistive load, as shown in Figure 20, as well as individual data sheets. The gate pulses should be just long enough to achieve complete turn-on, with a duty cycle of the order of 0.1%.

The series resistor is as specified in the data sheet. The definitions of rise, fall and delay times are given in Figure 21.

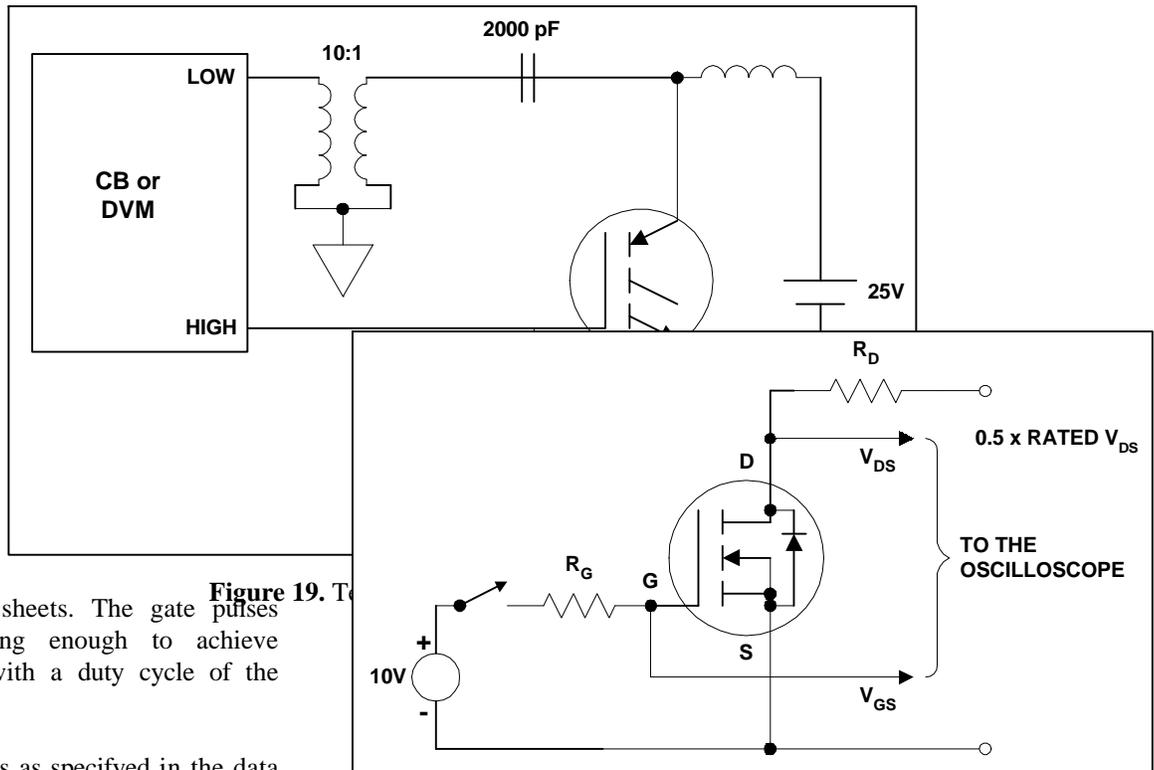


Figure 20. Test circuit for switching times

Power MOSFETs can switch in nanoseconds. Unless the test circuit is laid-out with RF techniques, the measurements will be totally unreliable. Switching time measurements frequently amount to a characterization of the test circuit, rather than the device under test. Gate charge provides a better indication of the switching capability of power MOSFETs.

### $Q_g$ , $Q_{gs}$ , $Q_{gd}$ Total Gate Charge, Gate-Source Charge, Gate-Drain Charge

The total gate charge has two components: the gate-source charge and the gate-drain charge (often called the Miller charge).

INT-944 gives more details on this test. Figures 22 and 23 show the test circuit and waveforms.

From the relationship  $Q = \int i$ , the following results are obtained:

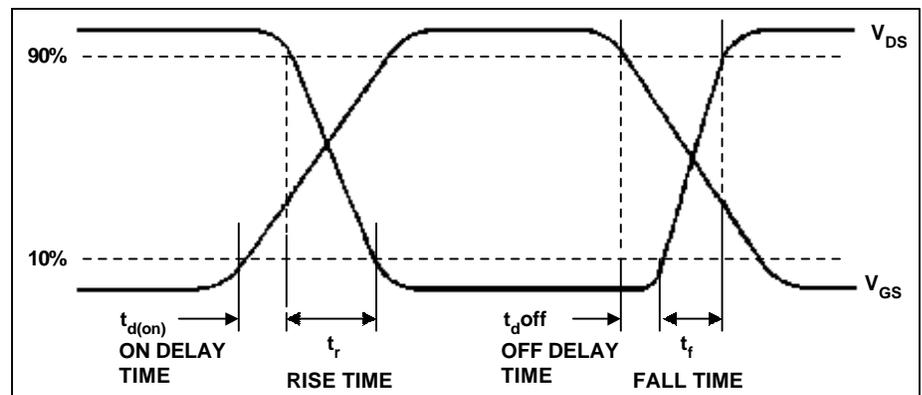


Figure 21. Switching time waveforms

$$Q_g = (t_3 - t_0) i_g,$$

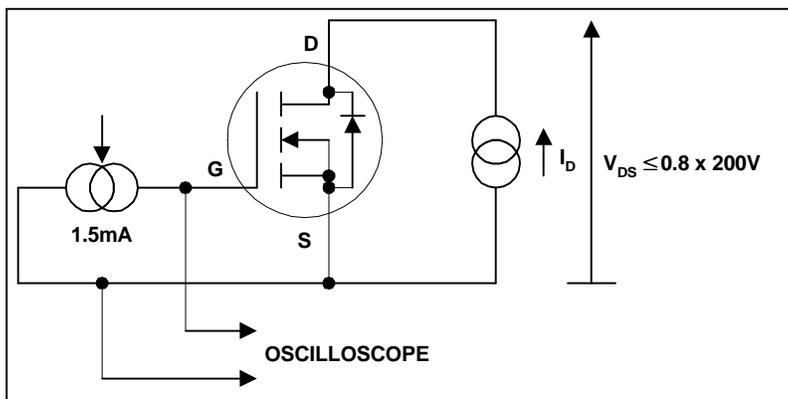
$$Q_{gd} = (t_2 - t_1) i_g,$$

$$Q_{gs} = Q_g - Q_{gd}$$

**V<sub>SD</sub> Body-Drain Diode Voltage Drop**

The current source may consist of a voltage source and a series resistor, as shown in Figure 24.

The voltage should be applied in short pulses (less than 300 microsec) with a low duty cycle (less than 2%).



**t<sub>rr</sub>, Q<sub>rr</sub> Body-Drain Diode Reverse Recovery Time and Reverse Recovery Charge**

Several test circuits are commonly used to characterize these parameters. Some have been qualified by JEDEC. The data sheet indicates the test method used for the specific device.

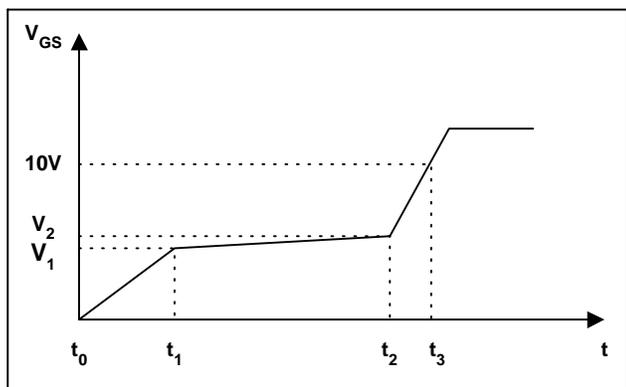


Figure 23. Gate charge waveforms

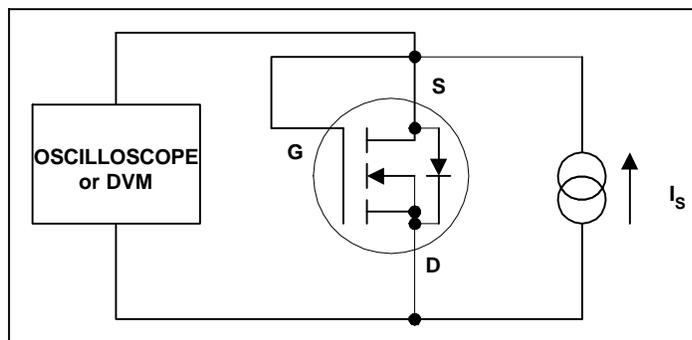


Figure 24. Test circuit MOSFET diode drop

**12. A fixture to speed-up testing time**

The most commonly tested parameters in a MOS-gated transistor are gate-source leakage (I<sub>GS</sub>), drain-source resistance (R<sub>DS(on)</sub>), breakdown voltage (BV<sub>DSS</sub>), drain current (I<sub>DSS</sub>), source-drain voltage (V<sub>SD</sub>), threshold (V<sub>GS(th)</sub>), and so on. These tests can be greatly simplified with the fixture shown in Figure 25.

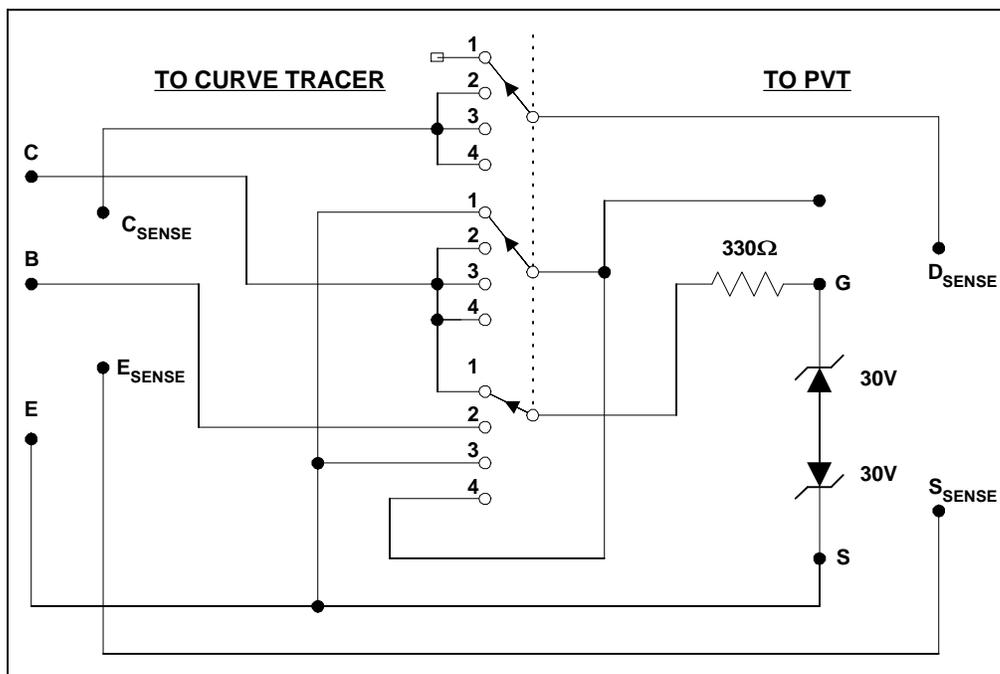


Figure 25. Test fixture for HEXFET test

<u>POSITION</u>	<u>MEASUREMENT</u>	<u>COMMENT</u>
1	$I_{GSS}$	C sense disconnected, Drain Source S/C connected, Collector Voltage applied to gate via 330 $\Omega$ resistor. Note: Gate protected by back to back 30V zeners.
2	$R_{DS(on)}$	Collector Voltage applied to DrainBased Voltage applied to Gate via 330 $\Omega$ resistor.
3	$B_{VDSS} / I_{DSS} / V_{DS}$	Collector Voltage applied to Drain, Gate Source S/C connected via 330 $\Omega$ resistor.
4	$V_{GS(th)}$	Collector Voltage applied to Drain, Gate Drain S/C connected via 330 $\Omega$ resistor.

***Related topics:***

*Parameter definition in IGBTs*

*Gate Charge*

*Thermal characteristics*

*ESD sensitivity*

*ESD test methods*

International  
**IOR** Rectifier

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Data and specification subject to change without notice.

