Integrated Circuit Systems, Inc.

ICS952703
Preliminary Product Preview

Programmable Timing Control Hub for K7™ System

Recommended Application:

SiS741 style chipset with 964 South Bridge.

Output Features:

- 1 - Pair of differential open drain CPU outputs
- 1 - Single-ended open drain CPU output
- 1 - Pair of current mode differential serial reference clock
- 8 - PCICLK @ 3.3V including 2 PCI clock free running
- 2 - AGPCLK @ 3.3V
- 3 - REF @ 3.3V
- 2 - ZCLK @ 3.3V
- 2 - IOAPIC @ 2.5V
- 1 - 12_48MHz @ 3.3V
- 1 - 24_48MHz @ 3.3V

Key Specifications:

- CPU Output Jitter <250ps
- AGP Output Jitter <250ps
- ZCLK Output Jitter <250ps
- PCI Output Jitter <500ps
- CPU-AGP/PCI/ZCLK skew: 2.5ns~3.5ns

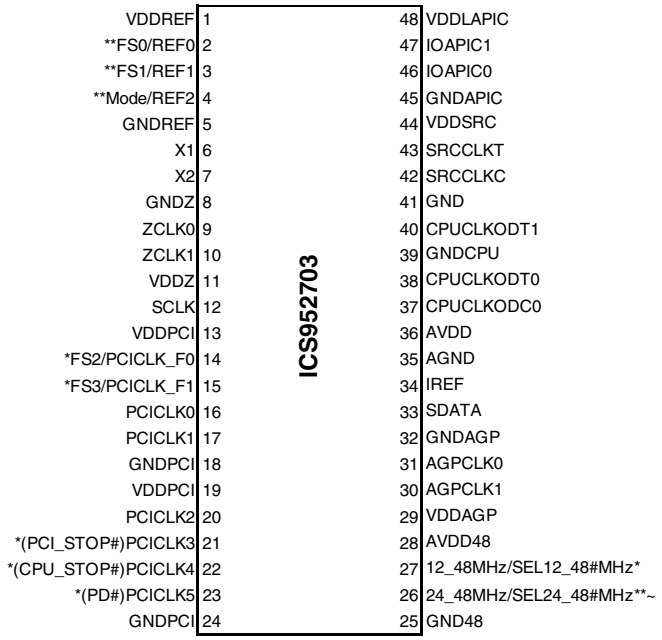
Features/Benefits:

- Selectable synchronous/asynchronous AGP/PCI frequency
- Programmable output frequency.
- Programmable output divider ratios.
- Programmable output rise/fall time.
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watch dog safe frequency.
- Support I2C Index read/write and block read/write operations.
- Uses external 14.318MHz reference input.

Functionality

Bit4	Bit3	Bit2	Bit1	Bit0	CPU	SRC	ZCLK	AGP	PCI
	FS3	FS2	FS1	FS0	MHz	MHz	MHz	MHz	MHz
0	0	0	0	0	200.00	100.00	133.33	66.66	33.33
0	0	0	0	1	200.01	100.00	133.34	66.67	33.33
0	0	0	1	0	200.97	100.00	133.98	66.99	33.49
0	0	0	1	1	190.11	100.00	126.74	63.37	31.69
0	0	1	0	0	100.00	100.00	133.33	66.66	33.33
0	0	1	0	1	100.00	100.00	133.34	66.67	33.33
0	0	1	1	0	100.99	100.00	134.66	67.33	33.66
0	0	1	1	1	95.00	100.00	126.66	63.33	31.67
0	1	0	0	0	166.66	100.00	133.33	66.66	33.33
0	1	0	0	1	166.65	100.00	133.32	66.66	33.33
0	1	0	1	0	161.59	100.00	129.27	64.64	32.32
0	1	0	1	1	151.97	100.00	121.57	60.79	30.39
0	1	1	0	0	133.33	100.00	133.33	66.66	33.33
0	1	1	0	1	133.34	100.00	133.34	66.67	33.33
0	1	1	1	0	133.98	100.00	133.98	66.99	33.49
0	1	1	1	1	126.66	100.00	126.66	63.33	31.67
1	0	0	0	0	206.02	100.00	137.35	68.67	34.34
1	0	0	0	1	210.00	100.00	140.00	70.00	35.00
1	0	0	1	0	214.06	100.00	142.70	71.35	35.68
1	0	0	1	1	217.90	100.00	145.27	72.63	36.32
1	0	1	0	0	103.01	100.00	137.35	68.67	34.34
1	0	1	0	1	105.00	100.00	140.00	70.00	35.00
1	0	1	1	0	106.99	100.00	142.65	71.33	35.66
1	0	1	1	1	109.01	100.00	145.35	72.68	36.34
1	1	0	0	0	164.66	100.00	131.73	65.86	32.93
1	1	0	0	1	167.91	100.00	134.33	67.17	33.58
1	1	0	1	0	171.22	100.00	136.98	68.49	34.24
1	1	0	1	1	174.38	100.00	139.50	69.75	34.88
1	1	1	0	0	137.32	100.00	137.32	68.66	34.33
1	1	1	0	1	140.00	100.00	140.00	70.00	35.00
1	1	1	1	0	142.67	100.00	142.67	71.34	35.67
1	1	1	1	1	145.33	100.00	145.33	72.66	36.33

Pin Configuration



48-SSOP

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

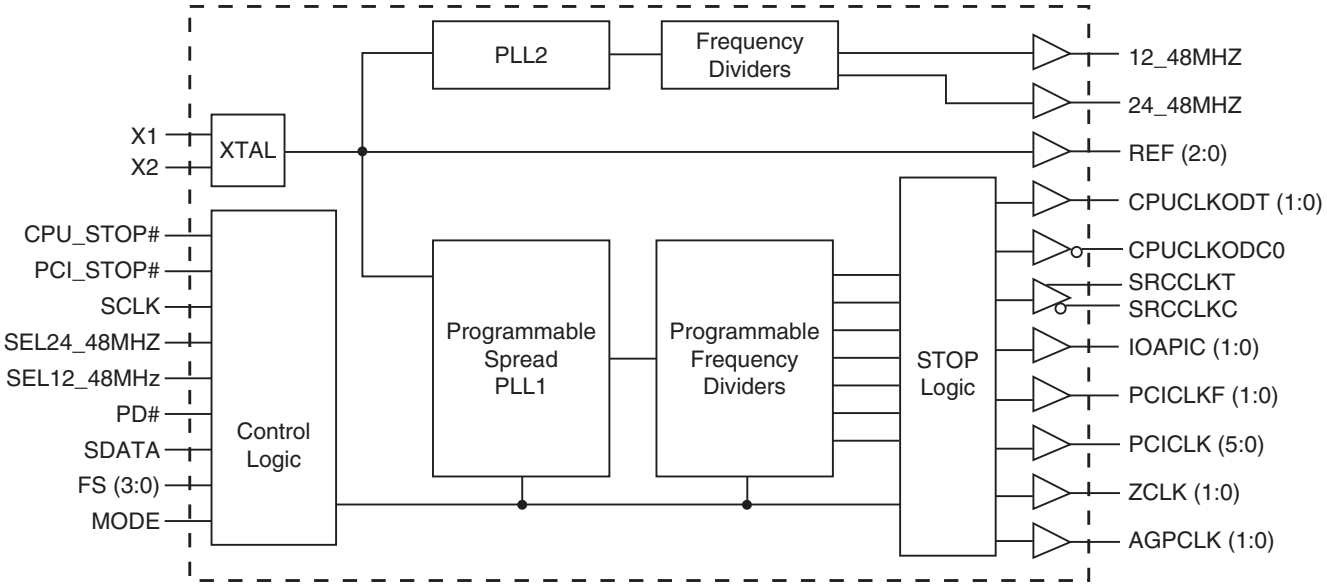
~ This output have 1.5X Drive Strength

General Description

The **ICS952703** is a two chip clock solution for desktop designs using SiS741 style chipsets. When used with a zero delay buffer such as the ICS9179-16 for PC133 or the ICS93735 for DDR applications it provides all the necessary clocks signals for such a system.

The **ICS952703** is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). ICS is the first to introduce a whole product line which offers full programmability and flexibility on a single clock device. Employing the use of a serially programmable I^2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. TCH also incorporates ICS's Watchdog Timer technology and a reset feature to provide a safe setting under unstable system conditions. M/N control can configure output frequency with resolution up to 0.1MHz increment.

Block Diagram



Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
2	**FS0/REF0	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
3	**FS1/REF1	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
4	**Mode/REF2	I/O	Function select latch input pin, 0=Desktop Mode, 1=Mobile Mode / Ref clock output.
5	GNDREF	PWR	Ground pin for the REF outputs.
6	X1	IN	Crystal input, Nominally 14.318MHz.
7	X2	OUT	Crystal output, Nominally 14.318MHz
8	GNDZ	PWR	Ground pin for the ZCLK outputs
9	ZCLK0	OUT	3.3V Hyperzip clock output.
10	ZCLK1	OUT	3.3V Hyperzip clock output.
11	VDDZ	PWR	Power supply for ZCLK clocks, nominal 3.3V
12	SCLK	IN	Clock pin of I2C circuitry 5V tolerant
13	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
14	*FS2/PCICLK_F0	I/O	Frequency select latch input pin / 3.3V PCI free running clock output.
15	*FS3/PCICLK_F1	I/O	Frequency select latch input pin / 3.3V PCI free running clock output.
16	PCICLK0	OUT	PCI clock output.
17	PCICLK1	OUT	PCI clock output.
18	GNDPCI	PWR	Ground pin for the PCI outputs
19	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
20	PCICLK2	OUT	PCI clock output.
21	*(PCI_STOP#)PCICLK3	I/O	Stops all PCICLKs besides the PCICLK_F clocks at logic 0 level, when input low. This input is activated by the MODE selection pin / PCI clock output.
22	*(CPU_STOP#)PCICLK4	I/O	Stops all CPUCLKs besides the CPUCLK_F clocks at logic 0 level, when input low. This input is activated by the MODE selection pin / PCI clock output.
23	*(PD#)PCICLK5	I/O	Asynchronous active low input pin used to power down the device into a low power state / PCI clock output.
24	GNDPCI	PWR	Ground pin for the PCI outputs
25	GND48	PWR	Ground pin for the 48MHz outputs
26	24_48MHz/SEL24_48#MHz**~	I/O	24/48MHz clock output / Latched select input for 24/48MHz output. 0=48MHz, 1 = 24MHz.
27	12_48MHz/SEL12_48#MHz*	I/O	12/48MHz clock output / Latched select input for 12/48MHz output. 0=48MHz, 1 = 12MHz.
28	AVDD48	PWR	Power for 24/48MHz outputs and fixed PLL core, nominal 3.3V
29	VDDAGP	PWR	Power supply for AGP clocks, nominal 3.3V
30	AGPCLK1	OUT	AGP clock output
31	AGPCLK0	OUT	AGP clock output
32	GNDAGP	PWR	Ground pin for the AGP outputs
33	SDATA	I/O	Data pin for I2C circuitry 5V tolerant
34	IREF	OUT	This pin establishes the reference current for the SRCCLK pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current.
35	AGND	PWR	Analog Ground pin for Core PLL
36	AVDD	PWR	3.3V Analog Power pin for Core PLL
37	CPUCLKODC0	OUT	"Complememtary" clocks of differential pair CPU outputs. These open drain outputs need an external 1.5V pull-up.
38	CPUCLKODT0	OUT	True clock of differential pair CPU outputs. These open drain outputs need an external 1.5V pull-up.
39	GNDCPU	PWR	Ground pin for the CPU outputs
40	CPUCLKODT1	OUT	True clock of differential pair CPU outputs. These open drain outputs need an external 1.5V pull-up.
41	GND	PWR	Ground pin.
42	SRCCLKC	OUT	Complement clock of differential pair for S-ATA support. +/- 300ppm accuracy required.
43	SRCCLKT	OUT	True clock of differential pair for S-ATA support. +/- 300ppm accuracy required.
44	VDDSRC	PWR	Supply for SRC clocks, 3.3V nominal
45	GNDAPIC	PWR	Ground pin for the IOAPIC outputs.
46	IOAPIC0	OUT	IOAPIC clock outputs, norminal 2.5V.
47	IOAPIC1	OUT	IOAPIC clock outputs, norminal 2.5V.
48	VDDLAPIC	PWR	Power pin for the IOAPIC outputs. 2.5V.

* Internal Pull-Up Resistor ** Internal Pull-Down Resistor ~ 1.5X Drive Strength

General SMBus serial interface information for the ICS952703

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
	O		
	O		O
	O		O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address $D3_{(H)}$			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
		X Byte	Beginning Byte N
ACK			
			O
	O		O
	O		O
	O		
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Table1: Frequency Selection Table

Bit4	Bit3	Bit2	Bit1	Bit0	CPU	SRC	ZCLK	AGP	PCI	Spread %
	FS3	FS2	FS1	FS0	MHz	MHz	MHz	MHz	MHz	
0	0	0	0	0	200.00	100.00	133.33	66.66	33.33	0.5% down
0	0	0	0	1	200.01	100.00	133.34	66.67	33.33	0.35% center
0	0	0	1	0	200.97	100.00	133.98	66.99	33.49	0.35% center
0	0	0	1	1	190.11	100.00	126.74	63.37	31.69	0.35% center
0	0	1	0	0	100.00	100.00	133.33	66.66	33.33	0.5% down
0	0	1	0	1	100.00	100.00	133.34	66.67	33.33	0.35% center
0	0	1	1	0	100.99	100.00	134.66	67.33	33.66	0.35% center
0	0	1	1	1	95.00	100.00	126.66	63.33	31.67	0.35% center
0	1	0	0	0	166.66	100.00	133.33	66.66	33.33	0.5% down
0	1	0	0	1	166.65	100.00	133.32	66.66	33.33	0.35% center
0	1	0	1	0	161.59	100.00	129.27	64.64	32.32	0.35% center
0	1	0	1	1	151.97	100.00	121.57	60.79	30.39	0.35% center
0	1	1	0	0	133.33	100.00	133.33	66.66	33.33	0.5% down
0	1	1	0	1	133.34	100.00	133.34	66.67	33.33	0.35% center
0	1	1	1	0	133.98	100.00	133.98	66.99	33.49	0.35% center
0	1	1	1	1	126.66	100.00	126.66	63.33	31.67	0.35% center
1	0	0	0	0	206.02	100.00	137.35	68.67	34.34	0.35% center
1	0	0	0	1	210.00	100.00	140.00	70.00	35.00	0.35% center
1	0	0	1	0	214.06	100.00	142.70	71.35	35.68	0.35% center
1	0	0	1	1	217.90	100.00	145.27	72.63	36.32	0.35% center
1	0	1	0	0	103.01	100.00	137.35	68.67	34.34	0.35% center
1	0	1	0	1	105.00	100.00	140.00	70.00	35.00	0.35% center
1	0	1	1	0	106.99	100.00	142.65	71.33	35.66	0.35% center
1	0	1	1	1	109.01	100.00	145.35	72.68	36.34	0.35% center
1	1	0	0	0	164.66	100.00	131.73	65.86	32.93	0.35% center
1	1	0	0	1	167.91	100.00	134.33	67.17	33.58	0.35% center
1	1	0	1	0	171.22	100.00	136.98	68.49	34.24	0.35% center
1	1	0	1	1	174.38	100.00	139.50	69.75	34.88	0.35% center
1	1	1	0	0	137.32	100.00	137.32	68.66	34.33	0.35% center
1	1	1	0	1	140.00	100.00	140.00	70.00	35.00	0.35% center
1	1	1	1	0	142.67	100.00	142.67	71.34	35.67	0.35% center
1	1	1	1	1	145.33	100.00	145.33	72.66	36.33	0.35% center

I²C Table: Frequency Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SS_EN	Spread Enable	RW	OFF	ON	1
Bit 6	-	SEL12_48MHz	Output Select	RW	48MHz	12MHz	Latch
Bit 5	-	SEL24_48MHz	Output Select	RW	48MHz	24MHz	Latch
Bit 4	-	Bit4	Freq Select Bit 4	RW	See Table1: Frequency Selection Table		0
Bit 3	-	FS3	Freq Select Bit 3	RW			Latch
Bit 2	-	FS2	Freq Select Bit 2	RW			Latch
Bit 1	-	FS1	Freq Select Bit 1	RW			Latch
Bit 0	-	FS0	Freq Select Bit 0	RW			Latch

I²C Table: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	2	REF0	Output Control	RW	Disable	Enable	1
Bit 6	3	REF1	Output Control	RW	Disable	Enable	1
Bit 5	4	REF2	Output Control	RW	Disable	Enable	1
Bit 4	43,42	SRCCLKT/C	Output Control	RW	Disable	Enable	1
Bit 3	14	PCICLK_F0	Output Control	RW	Disable	Enable	1
Bit 2	15	PCICLK_F1	Output Control	RW	Disable	Enable	1
Bit 1	16	PCICLK0	Output Control	RW	Disable	Enable	1
Bit 0	17	PCICLK1	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	20	PCICLK2	Output Control	RW	Disable	Enable	1
Bit 6	21	PCICLK3	Output Control	RW	Disable	Enable	1
Bit 5	22	PCICLK4	Output Control	RW	Disable	Enable	1
Bit 4	23	PCICLK5	Output Control	RW	Disable	Enable	1
Bit 3	26	24_48MHz	Output Control	RW	Disable	Enable	1
Bit 2	27	12_48MHz	Output Control	RW	Disable	Enable	1
Bit 1	30	AGPCLK1	Output Control	RW	Disable	Enable	1
Bit 0	31	AGPCLK0	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	1
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	IREF Bit1	IREF Mulitiplier Programming Bits	RW	00 = 5 x Iref	10 = 6 x Iref	1
Bit 4	-	IREF Bit0		RW	01 = 4 x Iref	11 = 7 x Iref	0
Bit 3	-	Vendor_ID3	Vendor ID	RW	-	-	0
Bit 2	-	Vendor_ID2		RW	-	-	0
Bit 1	-	Vendor_ID1		RW	-	-	0
Bit 0	-	Vendor_ID0		RW	-	-	1

I²C Table: Output Skew Control Register

Byte 4	Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-	PCISkw3	CPU-PCI 7 Step Skew Control (ps)	RW	0000:0	0100:150	1000:300	1100:450	X
Bit 6	-	PCISkw2		RW	0001:N/A	0101:N/A	1001:N/A	1101:600	X
Bit 5	-	PCISkw1		RW	0010:N/A	0110:N/A	1010:N/A	1110:750	X
Bit 4	-	PCISkw0		RW	0011:N/A	0111:N/A	1011:N/A	1111:900	X
Bit 3	-	AGPSkw3	CPU-AGP 7 Step Skew Control (ps)	RW	0000:0	0100:150	1000:300	1100:450	X
Bit 2	-	AGPSkw2		RW	0001:N/A	0101:N/A	1001:N/A	1101:600	X
Bit 1	-	AGPSkw1		RW	0010:N/A	0110:N/A	1010:N/A	1110:750	X
Bit 0	-	AGPSkw0		RW	0011:N/A	0111:N/A	1011:N/A	1111:900	X

I²C Table: Output Divider Control Register

Byte 5	Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-	ZCLKDiv3	ZCLK Divider Ratio Programmaing Bits	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 6	-	ZCLKDiv2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 5	-	ZCLKDiv1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 4	-	ZCLKDiv0		RW	0011:/7	0111:/14	1011:/28	1111:/56	X
Bit 3	-	AGPDiv3	AGP Divider Ratio Programmaing Bits	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 2	-	AGPDiv2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 1	-	AGPDiv1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 0	-	AGPDiv0		RW	0011:/7	0111:/14	1011:/28	1111:/56	X

I²C Table: Output Drive Control Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCIStr1	PCICLKF (1:0) Strength Control	RW	00 = 0.63X	10 = 0.88X	1
Bit 6	-	PCIStr0		RW	01 = 0.75X	11 = 1.00X	1
Bit 5	-	PCIStr1	PCICLK (2:0) Strength Control	RW	00 = 0.63X	10 = 0.88X	1
Bit 4	-	PCIStr0		RW	01 = 0.75X	11 = 1.00X	1
Bit 3	-	PCIStr1	PCICLK (5:3) Strength Control	RW	00 = 0.63X	10 = 0.88X	1
Bit 2	-	PCIStr0		RW	01 = 0.75X	11 = 1.00X	1
Bit 1	-	AGPStr1	AGPCLK Strength Control	RW	00 = 0.70X	10 = 0.90X	1
Bit 0	-	AGPStr0		RW	01 = 0.80X	11 = 1.00X	1

I²C Table: Reserved Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	1
Bit 6	-	Reserved	Reserved	RW	-	-	1
Bit 5	-	Reserved	Reserved	RW	-	-	1
Bit 4	-	Reserved	Reserved	RW	-	-	1
Bit 3	-	Reserved	Reserved	RW	-	-	1
Bit 2	-	Reserved	Reserved	RW	-	-	1
Bit 1	-	Reserved	Reserved	RW	-	-	1
Bit 0	-	Reserved	Reserved	RW	-	-	1

I²C Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Byte Count Programming b(7:0)	RW	Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes.		0
Bit 6	-	BC6		RW			0
Bit 5	-	BC5		RW			0
Bit 4	-	BC4		RW			0
Bit 3	-	BC3		RW			1
Bit 2	-	BC2		RW			1
Bit 1	-	BC1		RW			1
Bit 0	-	BC0		RW			1

I²C Table: WD Time Control & Async Frequency Selection Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	ASYNC1	Fix PLL Async Freq Programming bits	RW	See Table 2: Asynchronous Frequency Selection Table		0
Bit 5	-	ASYNC0		RW			0
Bit 4	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 3	-	WDTCtrl	Watch Dog Time base Control	RW	290ms Base	1160ms Base	0
Bit 2	-	WD2	WD Timer Bit 2	RW	These bits represent X*290ms (or 1.16S) the watchdog timer waits before it goes to alarm mode. Default is 7 X 290ms = 2s.		1
Bit 1	-	WD1	WD Timer Bit 1	RW			1
Bit 0	-	WD0	WD Timer Bit 0	RW			1

Table 2: Asynchronous Frequency Selection Table

B9 bit6	B9 bit5	SRC	ZCLK	AGP	PCI
0	0	Main PLL	Main PLL	Main PLL	Main PLL
0	1	100	133.33	66.66	33.33
1	0	100	150.00	75	37.5
1	1	100	133.33	80	40

I²C Table: VCO Control Select Bit & WD Timer Control Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/NEN	M/N Programming Enable	RW	Disable	Enable	0
Bit 6	-	WDEN	Watchdog Enable	RW	Disable	Enable	0
Bit 5	-	WDStatus	WD Alarm Status	R	Normal	Alarm	0
Bit 4	-	WD SF4	Watch Dog Safe Freq Programming bits	RW	Writing to these bit will configure the safe frequency as Byte0 bit (4:0).		0
Bit 3	-	WD SF3		RW			0
Bit 2	-	WD SF2		RW			0
Bit 1	-	WD SF1		RW			0
Bit 0	-	WD SF0		RW			0

I²C Table: VCO Frequency Control Register

Byte 11		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-		N Div9	N Divider Prog bit 9	RW			X
Bit 5	-		M Div5	M Divider Programming bits	RW			X
Bit 4	-		M Div4		RW			X
Bit 3	-		M Div3		RW			X
Bit 2	-		M Div2		RW			X
Bit 1	-		M Div1		RW			X
Bit 0	-		M Div0		RW			X

I²C Table: VCO Frequency Control Register

Byte 12		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		N Div7	N Divider Programming b(7:0)	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-		N Div6		RW			X
Bit 5	-		N Div5		RW			X
Bit 4	-		N Div4		RW			X
Bit 3	-		N Div3		RW			X
Bit 2	-		N Div2		RW			X
Bit 1	-		N Div1		RW			X
Bit 0	-		N Div0		RW			X

I²C Table: Spread Spectrum Control Register

Byte 13		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 6	-		SSP6		RW			X
Bit 5	-		SSP5		RW			X
Bit 4	-		SSP4		RW			X
Bit 3	-		SSP3		RW			X
Bit 2	-		SSP2		RW			X
Bit 1	-		SSP1		RW			X
Bit 0	-		SSP0		RW			X

I²C Table: Spread Spectrum Control Register

Byte 14		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		Reserved	Reserved	R	-	-	0
Bit 6	-		SSP14	Spread Spectrum Programming b(14:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 5	-		SSP13		RW			X
Bit 4	-		SSP12		RW			X
Bit 3	-		SSP11		RW			X
Bit 2	-		SSP10		RW			X
Bit 1	-		SSP9		RW			X
Bit 0	-		SSP8		RW			X

Absolute Maximum Ratings

Core Supply Voltage . . . . . 4.6 V
I/O Supply Voltage 3.6V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C
Case Temperature . . . . . 115°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}			5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			mA
Operating Supply Current	$I_{DD(op)}$	C_L = 0 pF; Select @ 100MHz			180	mA
Power Down Supply Current	I_{DDPD}	C_L = 0 pF; With input address to Vdd or GND			40	mA
Input frequency	F_i	V_{DD} = 3.3 V;	11		16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms
Skew[1]	$T_{CPU-PCI}$	V_T = 1.5 V	1.5		4	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLKT/C

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000			Ω
Output High Voltage	V_{OH3}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 1 mA			0.4	
Rise Time	t_{r3}	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps
Fall Time	t_{f3}	V_{OH} = 0.175V V_{OL} = 0.525V	175		700	ps
Duty Cycle	d_{t3}	V_T = 50%	45		55	%
Skew	t_{sk3}	V_T = 50%			100	ps
Jitter, Cycle to cycle	$t_{jcyc-cyc}$[1]	V_T = 50%			150	ps

Electrical Characteristics - PCICLK

T_A = 0 - 70°C; V_{DD} = 3.3 V,+/-5%; C_L = 30 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -18 mA	2.1			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	16		57	mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45		55	%
Skew[1]	t_{sk1}	V_T = 1.5 V			500	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			500	ps
	t_{jabs1}	V_T = 1.5 V			500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - AGPCLK

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V 3V66			250	ps

Electrical Characteristics - REF

T_A = 0 - 70°C; V_{DD} = 3.3 V , +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.6			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45		55	%
Jitter[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V			1000	ps
	t_{jabs5}	V_T = 1.5 V			800	ps

Electrical Characteristics - ZCLK

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			250	ps

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

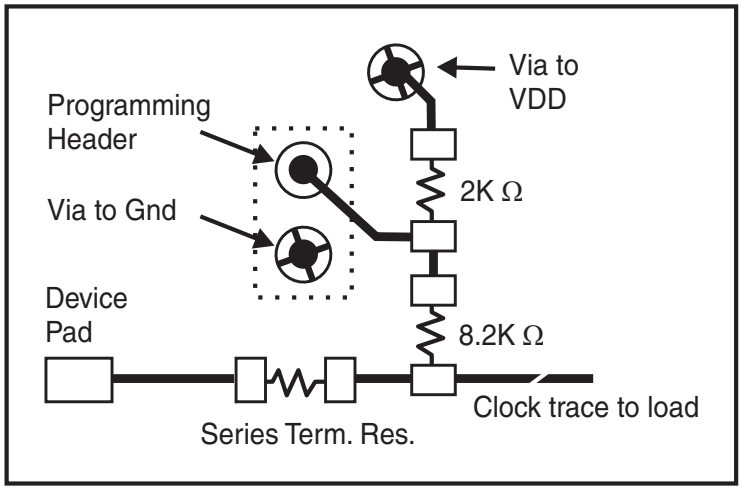
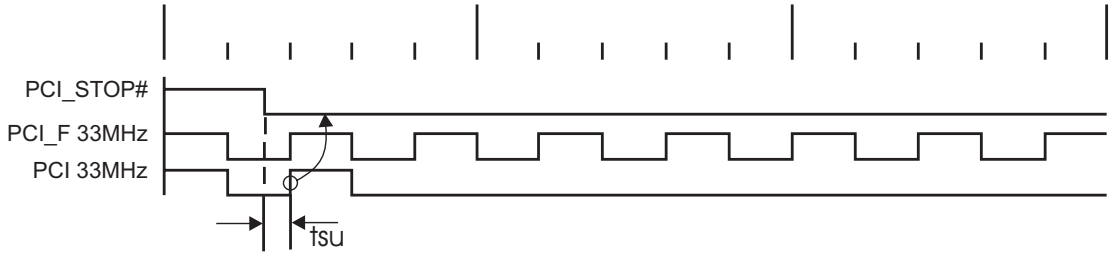


Fig. 1

PCI_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the PCI_STOP# signal will be the following. All PCI and stoppable PCI_F clocks will latch low in their next high to low transition. The PCI_STOP# setup time tsu is 10 ns, for transitions to be recognized by the next rising edge.

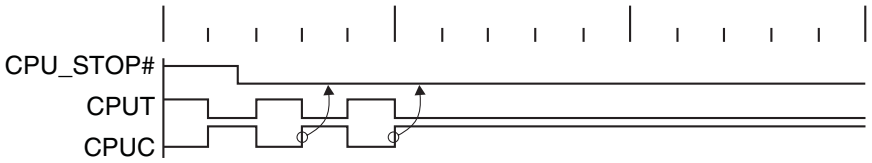
Assertion of PCI_STOP# Waveforms



CPU_STOP# - Assertion (transition from logic "1" to logic "0")

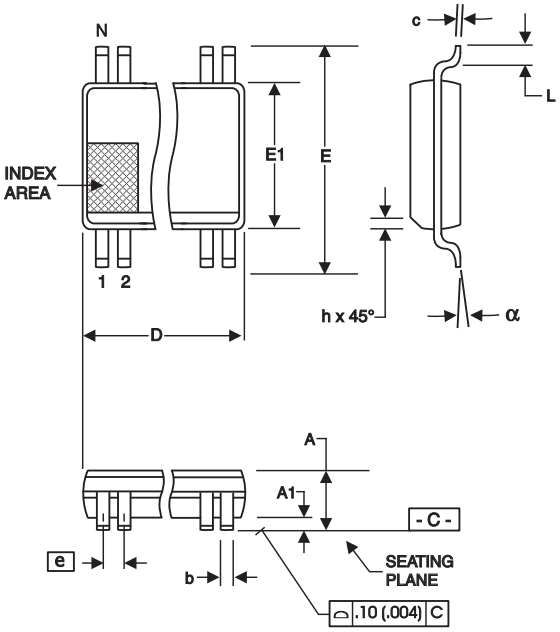
The impact of asserting the CPU_STOP# pin is all CPU outputs that are set in the I^2C configuration to be stoppable via assertion of CPU_STOP# are to be stopped after their next transition following the two CPU clock edge sampling as shown. The final state of the stopped CPU signals is CPUT=Low and CPUC=High. There is to be no change to the output drive current values. The CPUT will be driven high with a current value equal to (MULTSEL0) X (I REF), the CPUC signal will not be driven.

Assertion of CPU_STOP# Waveforms



CPU_STOP# Functionality

CPU_STOP#	CPUT	CPUC
1	Normal	Normal
0	iref * Mult	Float



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS952703yFLFT

Example:

ICS 95XXXX y F LF - T

- **Designation for tape and reel packaging**
- **RoHS Compliant**
- **Package Type**
  - F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  - ICS = Standard Device

0813B—05/17/05

Revision History

Rev.	Issue Date	Description	Page #
B	5/17/2005	Added LF Ordering Information	16