



## 2.0 GHz Super Low Power Dual Modulus Prescaler

The MC12054A is a super low power dual modulus prescaler used in phase-locked loop applications. Motorola's advanced Bipolar MOSAIC™ V technology is utilized to achieve low power dissipation of 5.4 mW at a minimum supply voltage of 2.7 V.

The MC12054A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 2.0 GHz in programmable frequency steps.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 2.0 GHz Toggle Frequency
- The MC12054 is Pin and Functionally Compatible with the MC12031
- Low Power 2.0 mA Typical
- 2.6mA Maximum,  $-40$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 2.7$  to  $5.5$  Vdc
- Short Setup Time ( $t_{set}$ ) 10ns Maximum @ 2.0 GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL
- Maximum Input Voltage Should Be Limited to 6.5 Vdc

MOSAIC V is a trademark of Motorola

### FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

**NOTES:** 1. SW: H =  $V_{CC}$ , L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.  
2. MC: H = 2.0 V to  $V_{CC}$ , L = GND to 0.8 V.

### MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	$V_{CC}$	$-0.5$ to $7.0$	Vdc
Operating Temperature Range	$T_A$	$-40$ to $85$	$^{\circ}\text{C}$
Storage Temperature Range	$T_{stg}$	$-65$ to $150$	$^{\circ}\text{C}$
Modulus Control Input, Pin 6	MC	$-0.5$ to $6.5$	Vdc

**NOTE:** ESD data available upon request.

## MC12054A

### MECL PLL COMPONENTS ÷64/65, ÷128/129 LOW POWER DUAL MODULUS PRESCALER

#### SEMICONDUCTOR TECHNICAL DATA

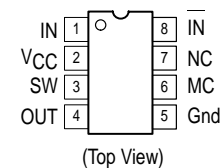


**D SUFFIX**  
PLASTIC PACKAGE  
CASE 751  
(SO-8)



**SD SUFFIX**  
PLASTIC PACKAGE  
CASE 940  
(SSOP-8)

### PIN CONNECTIONS



### ORDERING INFORMATION

Device	Operating Temp Range	Package
MC12054AD	$T_A = -40^{\circ}$ to $+85^{\circ}\text{C}$	SO-8
MC12054ASD		SSOP-8

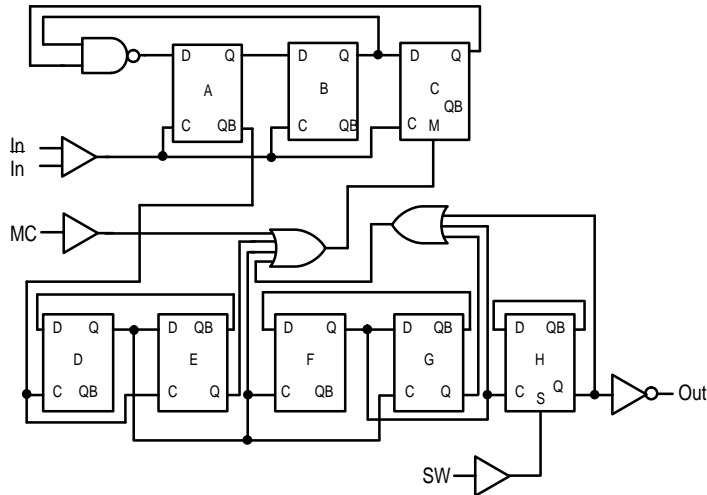
# MC12054A

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 2.7$  to  $5.5$  Vdc,  $T_A = -40$  to  $85^\circ\text{C}$ , unless otherwise noted.)

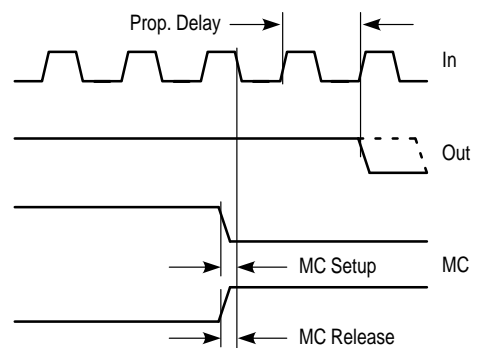
Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	$f_t$	0.1	2.5	2.0	GHz
Supply Current (Pin 2)	$I_{CC}$	–	2.0	2.6	mA
Modulus Control Input High (MC)	$V_{IH1}$	2.0	–	$V_{CC} + 0.5$ V	V
Modulus Control Input Low (MC)	$V_{IL1}$	Gnd	–	0.8	V
Divide Ratio Control Input High (SW)	$V_{IH2}$	$V_{CC} - 0.5$ V	$V_{CC}$	$V_{CC} + 0.5$ V	VDC
Divide Ratio Control Input Low (SW)	$V_{IL2}$	Open	Open	Open	–
Output Voltage Swing (Note 2) ( $C_L = 8.0$ pF, $R_L = 1.65$ k $\Omega$ )	$V_{out}$	0.8	1.1	–	$V_{pp}$
Modulus Setup Time MC to Out @ 2000 MHz	$t_{set}$	–	8.0	10	ns
Input Voltage Sensitivity 250–2000 MHz 100–250 MHz	$V_{in}$	100 400	– –	1000 1000	mVpp
Output Current (Note 1) $V_{CC} = 2.7$ V, $C_L = 8.0$ pF, $R_L = 1.65$ k $\Omega$ $V_{CC} = 5.0$ V, $C_L = 8.0$ pF, $R_L = 3.6$ k $\Omega$	$I_O$	– –	1.0 1.0	4.0 4.0	mA

**NOTES:** 1. Divide ratio of +64/65 @ 2.0 GHz  
2. Valid over voltage range 2.7 to 5.5 V;  $R_L = 1.65$  k $\Omega$  @  $V_{CC} = 2.7$  V;  $R_L = 3.6$  k $\Omega$  @  $V_{CC} = 5.0$  V

**Figure 1. Logic Diagram (MC12054A)**

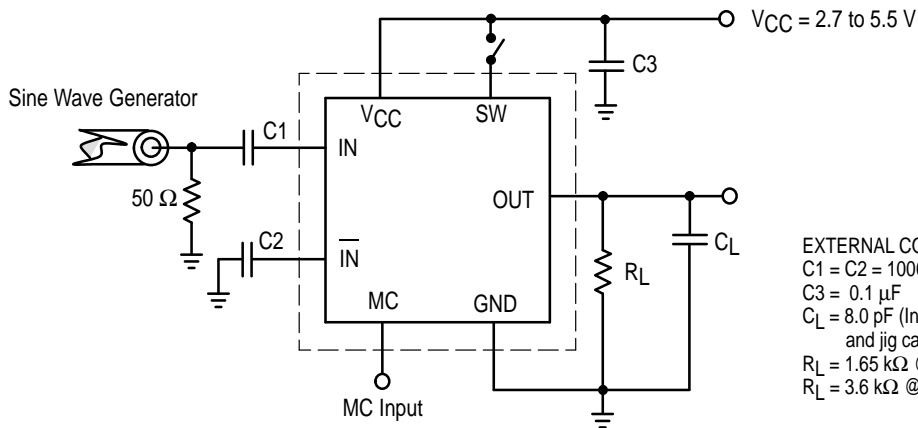


**Figure 2. Modulus Setup Time**



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

**Figure 3. AC Test Circuit**

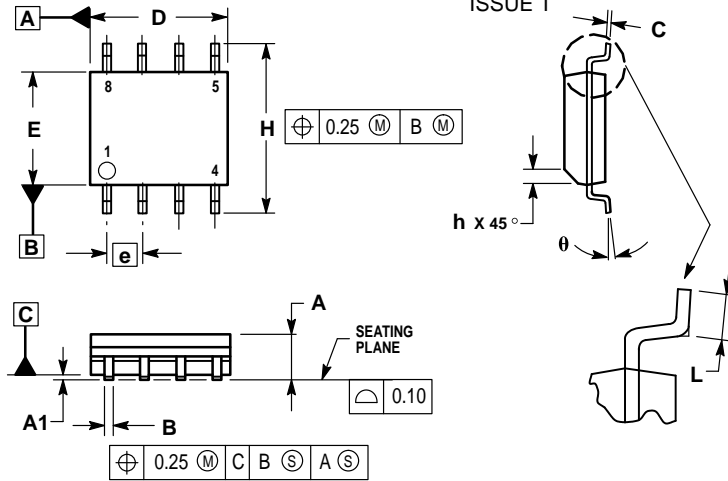


**EXTERNAL COMPONENTS**  
 $C_1 = C_2 = 1000$  pF  
 $C_3 = 0.1$   $\mu\text{F}$   
 $C_L = 8.0$  pF (Including Scope and jig capacitance)  
 $R_L = 1.65$  k $\Omega$  @  $V_{CC} = 2.7$  V  
 $R_L = 3.6$  k $\Omega$  @  $V_{CC} = 5.0$  V

# MC12054A

## OUTLINE DIMENSIONS

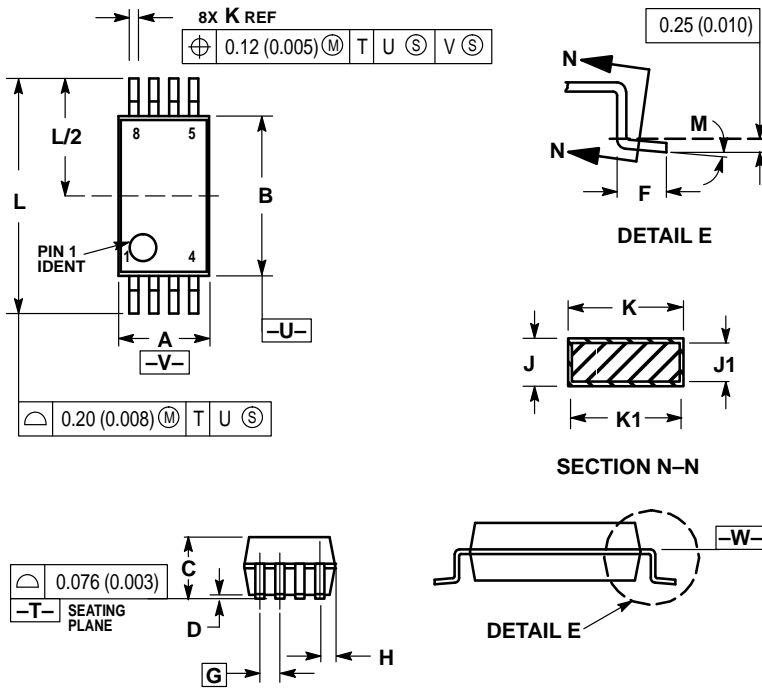
**D SUFFIX**  
**PLASTIC PACKAGE**  
**CASE 751-06**  
**(SO-8)**  
**ISSUE T**



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.


**SD SUFFIX**  
**PLASTIC PACKAGE**  
**CASE 940-03**  
**(SSOP-8)**  
**ISSUE B**



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

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MC12054A/D