

TV VIF & SIF & DEFLECTION SYSTEM

—YD2915

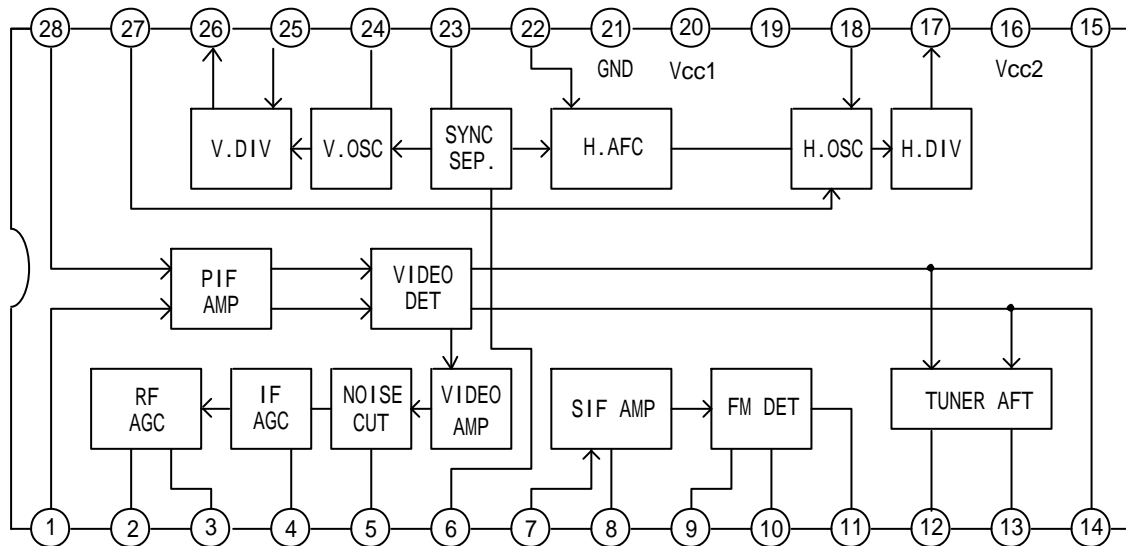
DESCRIPTION

The YD2915 is a monolithic integrated circuit containing all stage for the VIF, SIF and deflection of television receivers.

FEATURES

- *IF Amplifier with IF AGC
- *Video Amplifier, Video Detector
- *Noise Canceller, Forward RF AGC
- *Tuner AFT, Amplifier
- *Sound detector, sync separation
- *Vertical oscillation trigger and driver
- *Horizontal oscillation driver and AFC

BLOCK DIAGRAM



WuXi YouDa Electronics Co., Ltd

Add: E-3-A6, Li Yuan Economic Development Zone, Wuxi Jiangsu China

Tel: 86-510-5166655

Fax: 86-510-5169922

SHENZHEN OFFICE Tel: 86-755-83740369

13823533350

Fax: 86-755-83741418

ABSOLUTE MAXIMUM RATINGS (Tamb=25)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	Vcc(20)		12	V
Supply Current	Icc(20)		85	mA
	Icc(16)		15	
Circuit Voltage	V _{2, V3, V4, V24}	0		V
	V ₈	0	5.5	
	V ₁₃	0	4.2	
	V ₁₇	0		
Circuit Current	I _{5, I6, I11, I23, I26}	-10	0.3	mA
	I ₁₉	-0.6	0.6	
	I ₂₅	0	10	
	I ₁₇	-4	10	
Power Dissipation(Tamb=70)	P _D		1100	W
Operating Temperature	T _{opr}	-20	70	
Storage Temperature	T _{stg}	-55	125	

ELECTRICAL CHARATERISTICS (Tamb=25 , Vcc1=10V, unless otherwise specified)

VIDEO SECTION (fp: 38MHz, AGC: AGC, AM: 87.5%, 1kHz)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Video Output Voltage (Pin5)	V _o	AM; AGC; fp; Vi=10mV	1.8	2.1	2.6	V
Input Sensitivity	V _{SVF}	AM; AGC; fp; V _{OVF(PP)} : -3dB		316	565	μV
Maximum Input	V _{IM}	AM; AGC; fp; V _O >0dB	178	315		mV
Sync. Peak Voltage	V _{SYN}	fp; V ₁ =20mV	1.9	2.3	2.7	V
Noise Inverter Output Level (Pin5)	V _{TB}	V _{AGC} =5.35V; fp=38 ± 10MHz Vi=20mV	1.0	1.4	1.8	V
Noise Inverter Capture Level (Pin5)	V _{KB}	V _{AGC} =5.35V; fp=38 ± 10MHz Vi=20mV	3.0	3.4	3.8	V
AGC Range	AGC	AM; AGC; fp V _{OVF(PP)} =1.8~2.4v	60	63		dB
S/N Ratio	S/N	fp ; Vi=10mV	51	56		dB
Differential Gain	DG	AM; fp; APL=50% Vi=1.0mV		4	8	%
Differential Phase	DP	AM; fp; APL=50% Vi=1.0mV		3	6	DEG

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Video Frequency Characteristics	DW _V	V _{AGC} =5.35V G1 : 38MHz , 10Mv G2 : 37.9-28MHz, 1Mv	4.5	6.0	8.0	MHz
.Sound IF Output	V _{OSIF}	G1 : 38MHz; G2 : 31.5MHz P/S=20dB	100	160	225	mV
Input Resistor	R _i	fp; (Between Pin1 and Pin28)	0.8	1.0	1.2	k
Input Capacitor	C _i	fp; (Between Pin1 and Pin28)	3.0	4.0	5.0	pF
Output Resistor	Z _{OVF}	f=500KHz; V _i =20mV	30	50	150	
RF AGC Gain	A _{RFAGC}	f=10KHz , V _i =3.15mV	37	42	48	dB
AFT Sensitivity	S _{AFT}	fp=38 ± 1MHz, V _i =20mV	12.5	25	35	kHz/V

SOUND SECTION (fo : 6.5MHz , FM/fm : 1000Hz; f= ± 50kHz)

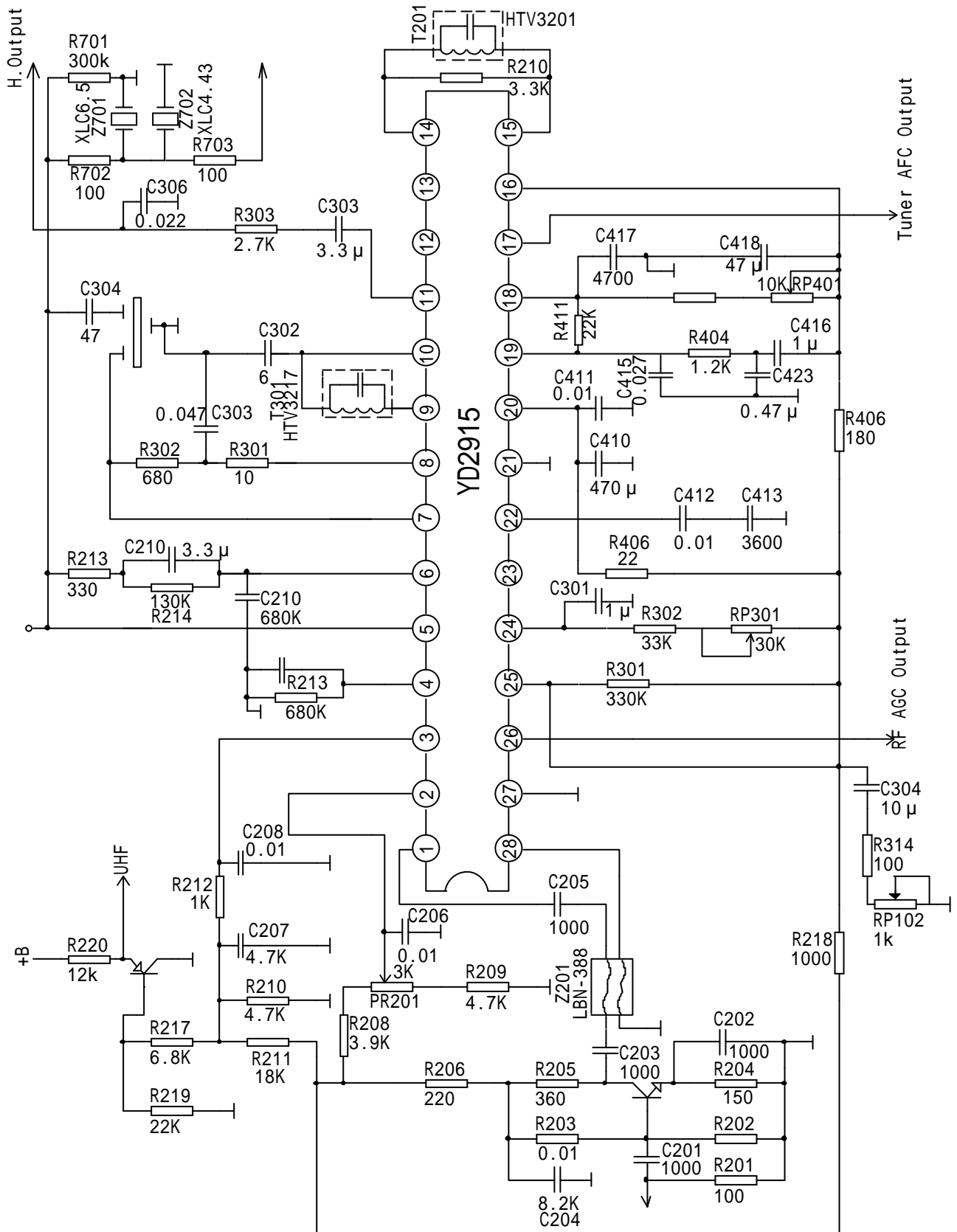
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Sound Det. Output	V _{OD}	fo; FM; f; V _i =100mV	280		800	mV
Input Limit Voltage	V _{IN(LIM)}	fo; FM; f; -3dB point		280	450	μ V
Total Harmonic Distortion	THD	fo; FM; f; V _i =100mV		0.6	1.0	%
AM Rejection Ratio	AMR	fo; FM; f; V _i =100mV AM : m=0.3	37	45		dB
Input Resistor	R _i	fo	6	20	100	k
Input Capacitor	C _i	fo	1.3	4.3	7.3	pF
Detector Input Resistor	R _{ID}	fo; Pin9	2.0	3.0	4.0	k
Detector Input Capacitor	C _{ID}	fo; Pin9	2.1	5.1	8.1	pF
Detector Input Resistor	R _{ID}	fo; Pin10	50	200		k
Detector Input Capacitor	C _{ID}	fo; Pin10	2.9	3.4	3.9	pF

DEFLECTION SECTION

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Vertical Free-Running Frequency	f _v	Pin26	47	50	53	Hz
Vertical OSC Pulse Width	t _{WH}		470	650	830	μ S

Vertical OSC Start Supply Voltage	V_{SV}	$f_{VO}=40\sim 60\text{Hz } V_{O(PP)}>0.7\text{V}$		4.9	6	V
Vertical Full in Range	$\frac{\Delta f_V}{V_{CC1}}$	$V_{CC1}=12\text{V}, 8\text{V}$ $f_{VO}/V_{CC}=f_{VO(12V)}-f_{VO(8V)}$	0	1.0	1.3	Hz
Horizontal OSC Frequency	f_H		15.0	15.75	16.25	KHz
Horizontal OSC Pulse Width	t_{WH}		21	24	27	μS
Horizontal OSC Start Supply Voltage	V_{SH}	$f_{HD}=10\text{-}20\text{Hz } V_{O(PP)}>1.0\text{V}$			5	V
Horizontal Full in Range	$\frac{\Delta f_H}{V_{CC2}}$	$V_{CC2}=12\text{V}, 8\text{V}$ $f_H/V_{CC}=f_{H(12V)}-f_{H(8V)}$	0	50	100	Hz
Horizontal OSC Control Sensitivity		$I_1=100\ \mu\text{A}$ input Variable OSC. Frequency Variable	73	81	89	Hz/ μA
Phase Det. Sensitivity	μp	Video Input $V_{IV(PP)}=2\text{V}$ $R(\ \mu)=3.14\text{k}$	13.5	16.5	19.5	$\mu\text{A}/\mu\text{S}$
Sync Separation Horizontal Pulse Width 1	$t_{SYN.1}$	Video input $V_{IV(PP)}=2.5\text{V}$ APL=50%	4.8	5.1	5.4	μS
Sync Separation Horizontal Pulse Width 2	$t_{SYN.2}$	Video input $V_{IV(PP)}=1.0\text{V}$ APL=50%	4.9	5.2	5.5	μS
Horizontal AFC Horizontal Pulse Width 1	$t_{SYN.3}$	Video input $V_{IV(PP)}=2.5\text{V}$ APL=50%	4.8	5.1	5.4	μS
Horizontal AFC Horizontal Pulse Width 2	$t_{SYN.4}$	Video input $V_{IV(PP)}=1.0\text{V}$ APL=50%	4.9	5.2	5.5	μS

APPLICATION CIRCUIT



OUTLINE DRAWING

