Mask-ROM 8-Bit CMOS Micro-controller

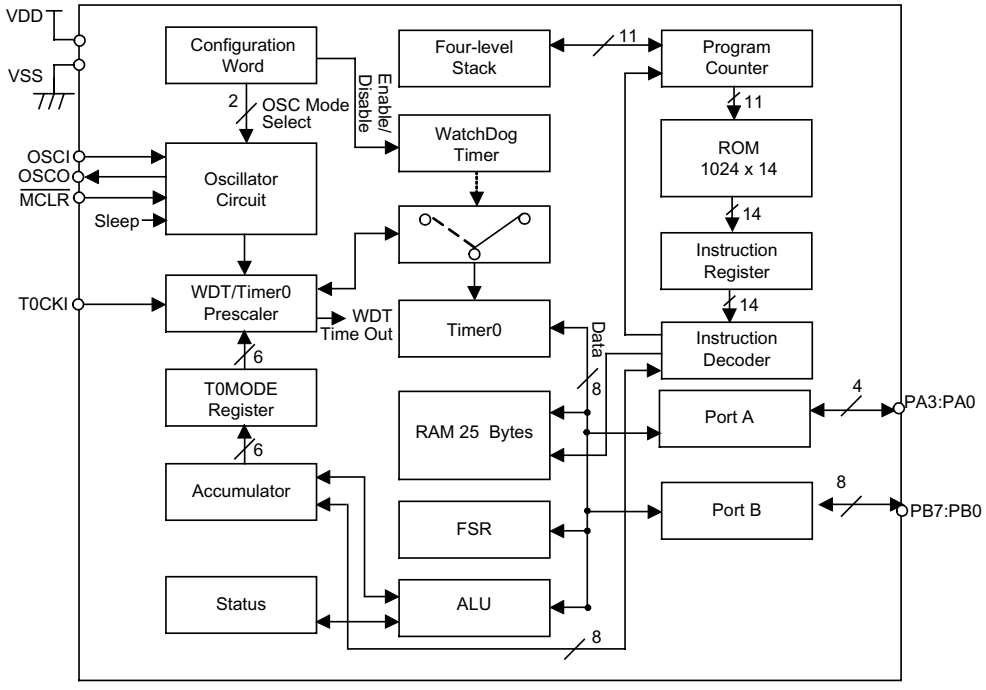
Features

- Total of 33 single word instructions
- The fast execution time may be 200ns for all single cycle instructions under 20MHz operation
- Operating voltage range:
  RC: 2.4V ~ 6.0V
  XTAL: 2.4 V ~ 6.0V
  LFXTAL: 2.4V ~ 6.0V
  HFXTAL: 3.0V ~ 6.0V
- 8-bit data bus
- 14-bit instruction word
- Four-level stacks
- On chip ROM size:
  - 1Kx14 bits for JA58560
- Internal RAM size:
  - 25 bytes for JA58560
- Direct and indirect addressing modes for data accessing
- 8-bit real time clock/counter with 8-bit programmable prescalers
- Internal power-on Reset
- Device Reset Timer
- Code protection
- Sleep mode for power saving
- On chip Watchdog Timer (WDT) based on internal RC oscillator
- Three I/O ports PA, PB and with independent direction control
- 4 types of oscillators can be selected by code options:
  - RC : Low-cost RC oscillator
  - XTAL : Standard crystal oscillator
  - HFXTAL : High frequency crystal oscillator
  - LFXTAL : Low frequency crystal oscillator

General Description

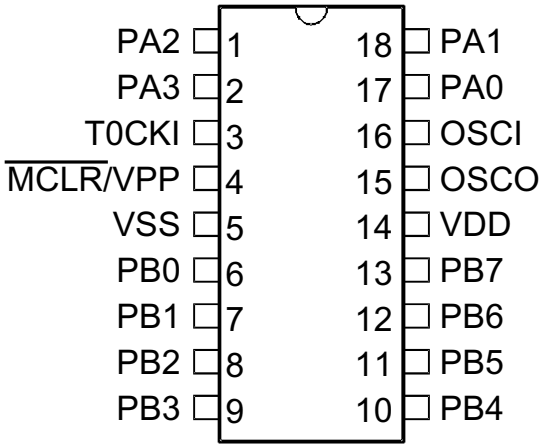
JA58560 series is an ROM based 8-bit microcontroller which employs a full CMOS technology enhanced with low cost, high speed and high noise immunity. Watchdog Timer, RAM, ROM, tri-state I/O port, power down mode, and real time programmable clock / counter are integrated into this chip. JA58560 contains 33 instructions, all are single cycle except for program branches which take two cycles.
On chip memory is available with for 1Kx14 bits of ROM for JA58560 and 25 bytes of static RAM.

Block Diagram



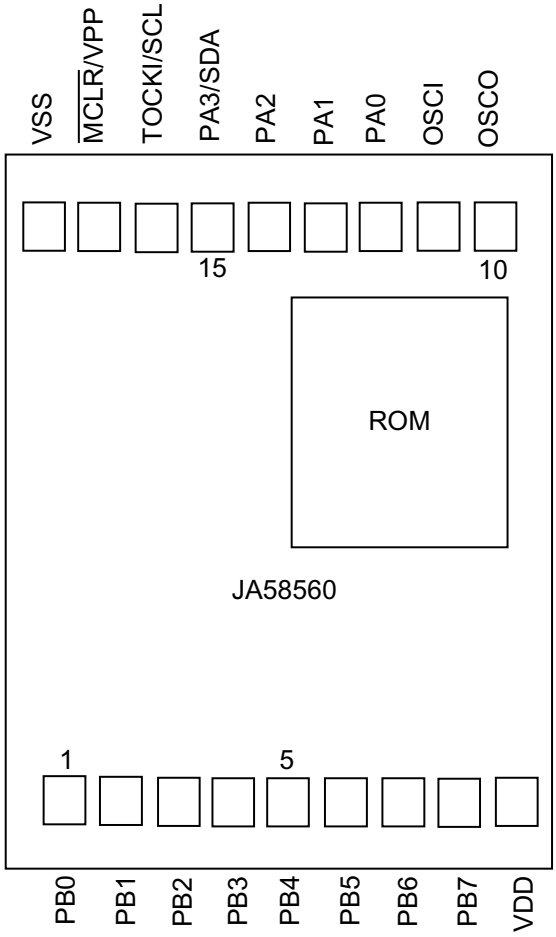
TEL：886-3-5770755 FAX：886-3-5770756 E-mail：sales@jaztek.com.tw Web-site：www.jaztek.com.tw

Pin Assignment



JA58560

Pad Assignment



TEL：886-3-5770755 FAX：886-3-5770756 E-mail：sales@jaztek.com.tw Web-site：www.jaztek.com.tw

Pad Coordinates

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	PB0	115.75	143	10	OSCO	1030.5	1380
2	PB1	235.75	143	11	OSCI	910.5	1380
3	PB2	355.75	143	12	PA0	790.5	1380
4	PB3	475.75	143	13	PA1	670.5	1380
5	PB4	595.75	143	14	PA2	550.5	1380
6	PB5	715.75	143	15	PA3/SDA	430.5	1380
7	PB6	835.75	143	16	TOCKI/SCL	310.5	1380
8	PB7	955.75	143	17	$\overline{\text{MCLR}}$/VPP	190.5	1380
9	VDD	1075.75	143	18	VSS	75.5	1380
Chip size : 1151.05 x 1523.05 μm^2							

Pin Descriptions

Pad Name	I/O	Description
OSCI	I	RC type: Input pin of RC oscillator Crystal type: Input terminal of crystal oscillator
OSCO	O	RC type: OSCO outputs with 1/4 frequency of OSCI to denote the cycle rate for instruction. Crystal type: Output terminal of crystal oscillator
T0CKI/SCL	I	Input pin of real time counter/clock. Must be tied to Vss or Vdd when unused.
$\overline{\text{MCLR}}$	I	Input pin for device reset.
PA0~PA3	I/O	PA0~PA3 as bi-directional I/O port
PB0~PB7	I/O	PB0~PB7 as bi-directional I/O port
VDD	-	Power supply
VSS	-	Ground

Absolute Maximum Rating

Ta = 0 to 70℃ GND=0V

Ambient Operating Temperature .....0℃ to +70℃

Store Temperature ..... -65℃ to +150℃

DC Supply Voltage (V_{DD}) .....0V to +6V

Voltage with respect to Ground (V_{SS}).....0.6V to (V_{DD}+0.6V)

TEL：886-3-5770755 FAX：886-3-5770756 E-mail：sales@jaztek.com.tw Web-site：www.jaztek.com.tw

Operating Conditions

Ta = 0 to 70℃ GND=0V

DC Supply Voltage..... +2.4V to +6.0v

Operating Temperature.....0℃ to 70℃

Electrical Characteristics (Under Operating Conditions)

Electrical characteristics of JA58560

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	I/O port, when V_{DD}=5V	2.0			V
		$\overline{MCLR}$, when V_{DD}=5V	3.7			V
Input Low Voltage	V_{IL}	I/O ports, when V_{DD}=5V			1.2	V
		$\overline{MCLR}$, when V_{DD}=5V			1.5	V
Output Voltage	V_{OH}	I/O ports, V_{DD}=4.5V, I_{OH}=-5.4mA, I_{OL}=8.7mA ; in RC mode I_{OL}=10mA	3.6			V
	V_{OL}				0.6	V
Operating Current	HFXTAL: 20MHz, WDT disable, Cosci=27pF, Cosco=20pF					
	I_{DD}	V_{DD}=6.0V		3.135		mA
		V_{DD}=5.0V		2.365		mA
		V_{DD}=4.0V		1.574		mA
		V_{DD}=3.0V		1.014		mA
	HFXTAL: 12MHz, WDT disable, Cosci=27pF, Cosco=20pF					
	I_{DD}	V_{DD}=6.0V		2.111		mA
		V_{DD}=5.0V		1.497		mA
		V_{DD}=4.0V		1.040		mA
		V_{DD}=3.0V		0.629		mA
		V_{DD}=2.4V		0.451		mA
	XTAL: 12MHz, WDT disable, Cosci=27pF, Cosco=20pF					
	I_{DD}	V_{DD}=6.0V		2.423		mA
		V_{DD}=5.0V		1.697		mA
		V_{DD}=4.0V		1.154		mA
		V_{DD}=3.0V		0.697		mA
		V_{DD}=2.4V		0.476		mA

TEL：886-3-5770755 FAX：886-3-5770756 E-mail：sales@jaztek.com.tw Web-site：www.jaztek.com.tw

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Operating Current	XTAL: 4MHz, WDT disable, Cosci=27pF, Cosco=20pF						
	I_{DD}	V_{DD}=6.0V			1.332		mA
		V_{DD}=5.0V			0.955		mA
		V_{DD}=4.0V			0.613		mA
		V_{DD}=3.0V			0.358		mA
		V_{DD}=2.4V			0.235		mA
	LFXTAL: 32kHz, WDT disable, Cosci=27pF, Cosco=20pF						
	I_{DD}	V_{DD}=6.0V			43.14		μA
		V_{DD}=5.0V			22.45		μA
		V_{DD}=4.0V			10.28		μA
		V_{DD}=3.0V			5.338		μA
		V_{DD}=2.4V			3.355		μA
	V_{DD}=5V, RC mode, WDT Disable. These values include current though Text						
	I_{DD}	C=3P	R=1kΩ	F=14.31MHz		4.56		mA
			R=2kΩ	F=12.5MHz		2.873		mA
			R=3.3kΩ	F=9.883MHz		1.885		mA
			R=4.7kΩ	F=8.191MHz		1.448		mA
			R=5.1kΩ	F=7.847MHz		1.376		mA
			R=10kΩ	F=4.763MHz		0.769		mA
			R=47kΩ	F=1.300MHz		146.8		μA
			R=100kΩ	F=640.7kHz		105.2		μA
			R=300kΩ	F=216kHz		43.1		μA
	I_{DD}	C=20P	R=1kΩ	F=11.54MHz		4.295		mA
			R=2kΩ	F=8.32MHz		2.43		mA
			R=3.3kΩ	F=5.974MHz		1.504		mA
			R=4.7kΩ	F=4.605MHz		1.096		mA
			R=5.1kΩ	F=4.352MHz		1.029		mA
			R=10kΩ	F=2.394MHz		0.543		mA

TEL：886-3-5770755 FAX：886-3-5770756 E-mail：sales@jaztek.com.tw Web-site：www.jaztek.com.tw

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
Operating Current	I_{DD}	C=20P	R=47kΩ	F=591.3kHz		132.8		μA
			R=100kΩ	F=283.8kHz		69.76		μA
			R=300kΩ	F=95.97kHz		29.64		μA
	I_{DD}	C=100P	R=1kΩ	F=5.433MHz		3.53		mA
			R=2kΩ	F=3.329MHz		1.799		mA
			R=3.3kΩ	F=2.168MHz		1.112		mA
			R=4.7kΩ	F=1.583MHz		0.796		mA
			R=5.1kΩ	F=1.482MHz		0.746		mA
			R=10kΩ	F=756.8kHz		0.38		mA
			R=47kΩ	F=173.6kHz		90.72		μA
			R=100kΩ	F=82.72kHz		47.98		μA
			R=300kΩ	F=27.68kHz		21.48		μA
	I_{DD}	C=300P	R=1kΩ	F=2.535MHz		3.1		mA
			R=2kΩ	F=1.459MHz		1.567		mA
			R=3.3kΩ	F=915.1kHz		0.957		mA
			R=4.7kΩ	F=655.4kHz		0.681		mA
			R=5.1kΩ	F=611.6kHz		0.636		mA
			R=10kΩ	F=306.9kHz		0.32		mA
			R=47kΩ	F=68.81kHz		76.78		μA
			R=100kΩ	F=32.62kHz		41.13		μA
			R=300kΩ	F=10.86kHz		19.21		μA
Sleeping Current	WDT Disable, C_{OSCI}=27pF, C_{OSCO}=20pF							
	I_{DD}	V_{DD}=6.0V				1.378		uA
		V_{DD}=5.0V				1.004		uA
		V_{DD}=4.0V				0.725		uA
		V_{DD}=3.0V				0.499		uA
		V_{DD}=2.4V				0.375		uA

TEL：886-3-5770755 FAX：886-3-5770756 E-mail：sales@jaztek.com.tw Web-site：www.jaztek.com.tw

The registers of JA58560

The registers of JA58560	
Address	**Description**
00H	Indirect addressing register
01H	Timer0
02H	PC
03H	Status
04H	FSR
05H	Port A
06H	Port B
07H~1FH	General purpose register

- **INAR (Indirect Address Register) : 00H**

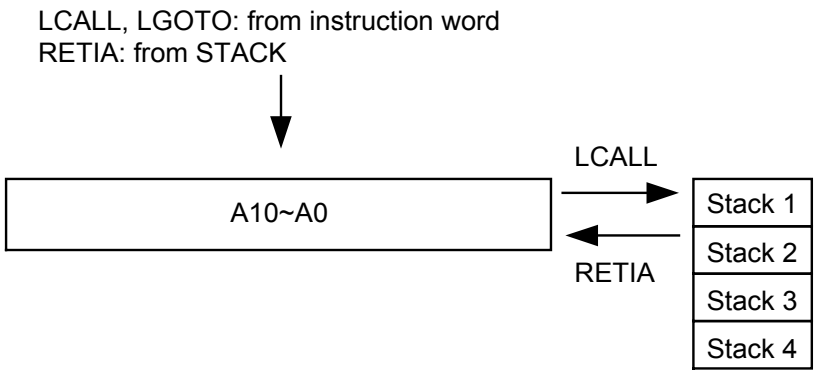
  INAR is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction accessing this register can access data pointed by FSR(04H).

- **Timer0 (8-bit real-time clock/timer) : 01H**

  This register increases by an external signal edge applied to T0CKI pin, or by internal instruction cycle. It can be read or written as any other register.

- **PC (Program Counter) : 02H**

  This register increases itself along with every instruction cycle, except the following condition specified in Figure 3.1:



Program Counter

TEL：886-3-5770755 FAX：886-3-5770756 E-mail：sales@jaztek.com.tw Web-site：www.jaztek.com.tw

- **Status (Status Register) : 03H**

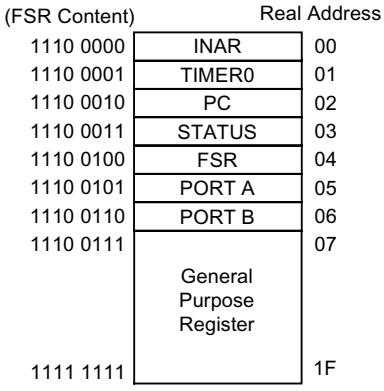
The content of Status register is listed in Table.

Bit	Symbol	Description
0	C	Carry/borrow bit ADDAR = 1, a carry occurred = 0, a carry did not occur SUBAR = 1, a borrow did not occur = 0, a borrow occurred
1	DC	Half carry/half borrow bit ADDAR = 1, a carry from the 4th low order bit of the result occurred = 0, a carry from the 4th low order bit of the result did not occur SUBAR = 1, a borrow from the 4th low order bit of the result did not occur = 0, a borrow from the 4th low order bit of the result occurred
2	Z	Zero bit = 1, the result of a logic operation is zero = 0, the result of a logic operation is not zero
3	PD	Power down flag bit: = 1, after power-up or by the CLRWDT instruction = 0, by the SLEEP instruction
4	TO	Time overflow flag bit: = 1, after power-up or by the CLRWDT or SLEEP instruction = 0, a WDT time-overflow occurred
5~7	-	Reserved

- **FSR (File select register pointer): 04H**

Bit 0~4 are used to select up to 32 registers (address: 00h~1Fh). In JA58560, Bit 5~7 were fixed 1. The indirect addressing mode shows as below:

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	Indirect Address mode location select				



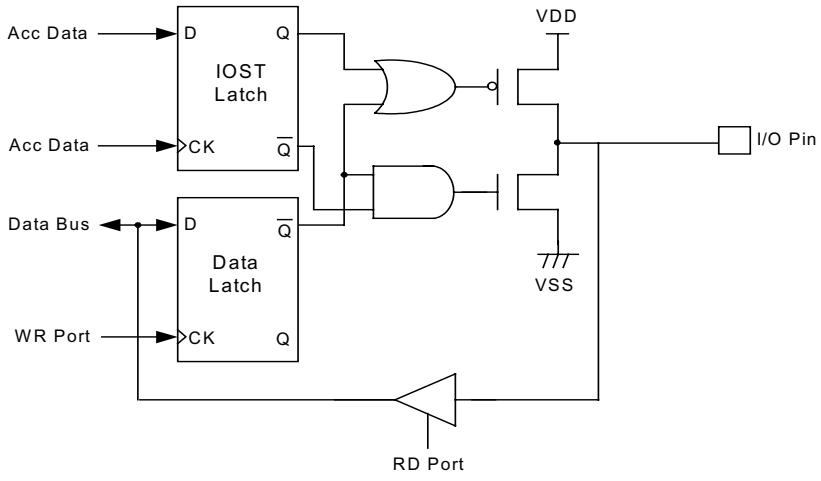
Data Memory Configuration

TEL：886-3-5770755 FAX：886-3-5770756 E-mail：sales@jaztek.com.tw Web-site：www.jaztek.com.tw

- **PORT A: 05H**
  PA3:PA0, bi-directional I/O Register
- **PORT B: 06H**
  PB7:PB0, bi-directional I/O Register
- **T0MODE REGISTER:**
  T0MODE is a write-only register and the content is listed in Table.

Bit	Symbol	Description		
2~0	PS0:PS0	Bit Value	Timer Rate	WDT Ratev
		0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	1:2 1:4 1:8 1:16 1:32 1:64 1:128 1:256	1:1 1:2 1:4 1:8 1:16 1:32 1:64 1:128
3	PSC	Prescaler assign bit: = 0, Timer0 = 1, WDT		
4	TE	Timer0 source signal edge select bit: = 0, increment when low-to-high transition on T0CKI pin = 1, increment when high-to-low transition on T0CKI pin		
5	TS	Timer0 source signal select bit: = 0, internal instruction clock cycle = 1, transition on T0CKI pin		
6~7	-	Reserved		

- **IOST (Control Port I/O Mode Register)**
  The IOST register is “write-only”
  = 0, I/O pin in output mode;
  = 1, I/O pin in input mode.
- **I/O Ports Equivalent Circuit**



TEL：886-3-5770755 FAX：886-3-5770756 E-mail：sales@jaztek.com.tw Web-site：www.jaztek.com.tw

Note:

1. The IOST registers are “write-only” and set upon RESET.
2. If the IOST latch is “0”, the corresponding I/O pin is in output mode;
   if the IOST latch is “1”, the corresponding I/O pin is in input mode.

RESET

This device may be reset by one of the following ways:

(1) Power-on Reset: At power-up, this device is kept in a RESET condition for a period of 18ms after the voltage on $\overline{MCLR}$ pin has reached a logic high level.

(2) $\overline{MCLR}$ reset (normal operation).

(3) WDT reset (normal operation).

(4) $\overline{MCLR}$ wake-up (from sleep mode).

(5) WDT wake-up (from sleep mode) : Executing the SLEEP instruction can force this device to enter sleep mode (power saving mode). While in sleep mode, the WDT is cleared but keeps running. This device can be awakened by WDT time-out or reset input on MCLR pin.

The contents of registers after reset are listed below:

Address	Register	Power-On Reset	MCLR or WDT Reset
00h	INAR	xxxx xxxx	uuuu uuuu
01h	Timer0	xxxx xxxx	uuuu uuuu
02h	PC	1111 1111	1111 1111
03h	STATUS	0001 1xxx	000# #uuu
04h	FSR	111x xxxx	111u uuuu
05h	PORTA	---- xxxx	---- uuuu
06h	PORTB	xxxx xxxx	uuuu uuuu
07h-1Fh	General Purpose Register	xxxx xxxx	uuuu uuuu
N/A	Acc	xxxx xxxx	uuuu uuuu
N/A	IOST	1111 1111	1111 1111
N/A	T0MODE	--11 1111	--11 1111

Note:

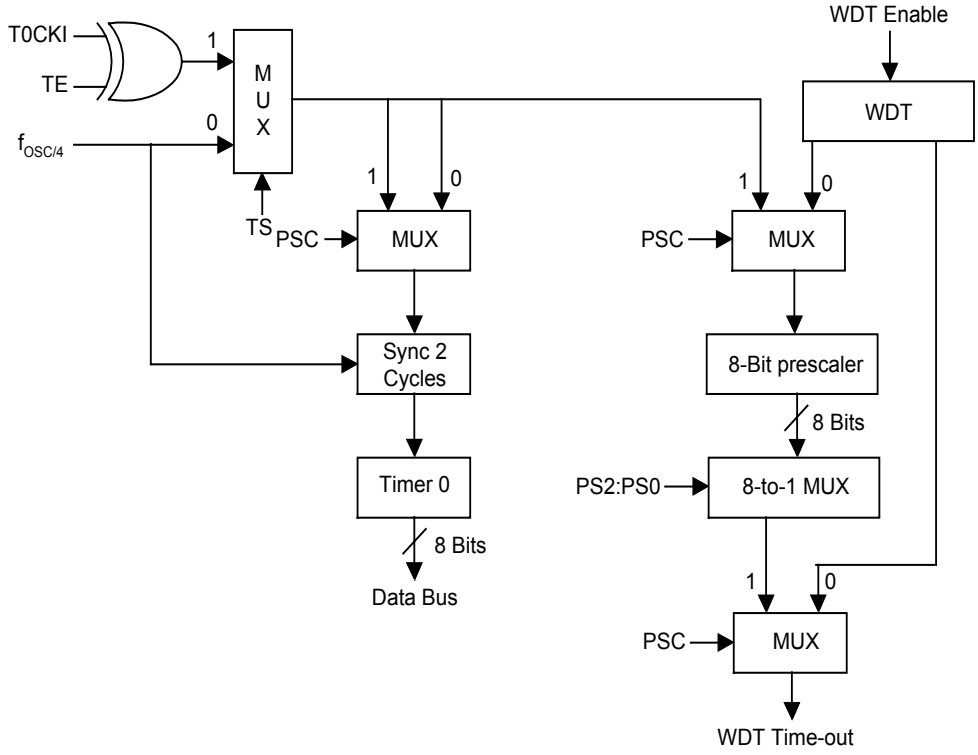
″x″ = unknown, ″u″ = unchanged, ″-″ = unimplemented, read as ″0″,

″#″ = refer to the following table

Condition	Status: bit 4	Status: bit 3
$\overline{MCLR}$ Reset (not during SLEEP)	u	u
$\overline{MCLR}$ Reset during SLEEP	1	0
WDT Reset (not during SLEEP)	0	1
WDT Reset during SLEEP	0	0

TEL：886-3-5770755 FAX：886-3-5770756 E-mail：sales@jaztek.com.tw Web-site：www.jaztek.com.tw

Real Time Clock (Timer0) and Watchdog Timer



- **Timer0**

  Timer0 is an 8-bit timer/counter. The clock source of Timer0 may come from the internal clock or by an external clock source presented at the T0CKI pin.

  To select the internal clock source, bit 5 of the T0MODE register should be clear. In this mode, Timer0 increases 1 on every instruction cycle (without prescaler).

  To select the external clock source, bit 5 of the T0MODE register should be set. In this mode, Timer0 increases 1 on every falling or rising edge of T0CKI pin, which was be controlled by bit 4 of T0MODE register.

- **Watchdog Timer (WDT)**

  The Watchdog Timer is a free running on-chip RC oscillator. This RC oscillator is separated from the RC oscillator of the OSCI pin. That means the WDT keeps running even when the oscillator driver is turned off, such as in sleep mode. During normal operation or in sleep mode, a WDT time-out causes the device reset and the TO bit (bit 4 of STATUS register) is cleared.

  Without prescaler, the WDT time-out period is 18ms. This period can be increase by using the prescaler. The division ratio of prescaler is up to 1:128. Thus, the longest time-out period is approximately 2.3s.

- **Prescaler**

  The 8-bit prescaler may be assigned to either the Timer0 or the WDT through the PSC bit (bit 3 of the T0MODE register). Setting this bit assigns the prescaler to the WDT. Resetting this bit assigns the prescaler to the Timer0. The PS2:PS0 bits determine the prescale ratio. The prescaler can not be assigned to both the Timer0 and WDT simultaneously.

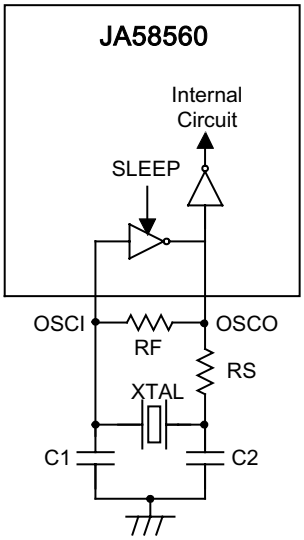
TEL：886-3-5770755 FAX：886-3-5770756 E-mail：sales@jaztek.com.tw Web-site：www.jaztek.com.tw

Oscillator Configuration

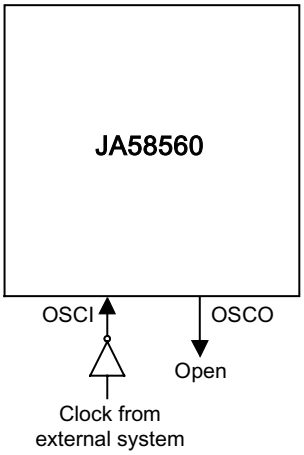
This device supports four oscillator modes. Users can program two configuration bits to select the appropriate mode. These oscillator modes offered as:

- RC: Low-cost oscillator
- XTAL: Standard crystal oscillator
- HFXTAL: High frequency crystal oscillator
- LFXTAL: Low frequency crystal oscillator

- **XTAL, HFXTAL or LFXTAL modes**

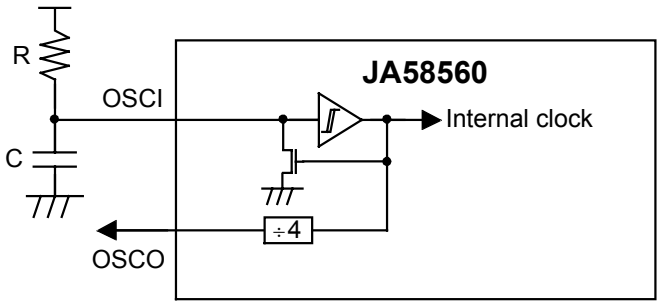


(a) Crystal operation (or ceramic resonator)



(b) External clock input operation

- **RC Oscillator Mode**



TEL：886-3-5770755 FAX：886-3-5770756 E-mail：sales@jaztek.com.tw Web-site：www.jaztek.com.tw

Instruction Table

Mnemonic Operands	Description	Cycles	Instruction Code	Status Affected
BCR R, bit	Clear bit in R	1	11 11bb brrr rrrr	None
BSR R, bit	Set bit in R	1	11 10bb brrr rrrr	None
BTRSC R, bit	Test bit in R and skip if clear	1 or 2(skip)	11 01bb brrr rrrr	None
BTRSS R, bit	Test bit in R and skip if set	1 or 2(skip)	11 00bb brrr rrrr	None
CLRWDT	Clear Watchdog Timer	1	01 0000 0000 0001	$\overline{TO}$, $\overline{PD}$
T0MODE	Load T0MODE Register	1	01 0000 0000 0010	None
SLEEP	Go into standby mode	1	01 0000 0000 0011	$\overline{TO}$, $\overline{PD}$
IOST R	Load IOST Register	1	01 0000 0000 0rrr	None
ANDIA I	AND immediate with Acc	1	00 1001 iiii iiii	Z
XORIA I	Exclusive OR immediate with Acc	1	00 1000 iiii iiii	Z
MOVIA I	Move immediate to Acc	1	00 0001 iiii iiii	None
IORIA I	Inclusive OR immediate with Acc	1	00 0011 iiii iiii	Z
RETIA I	Return, place immediate in A	2	00 1100 iiii iiii	None
LCALL I	Call subroutine	2	10 0iii iiii iiii	None
LGOTO I	Unconditional branch	2	10 1iii iiii iiii	None
NOP	No operation	1	01 0000 0000 0000	None
MOVAR R	Move Acc to R	1	01 0000 1rrr rrrr	None
COMR R, d	Complement R	1	01 0010 drrr rrrr	Z
MOVR R, d	Move R	1	01 0011 drrr rrrr	Z
RRR R, d	Rotate right R	1	01 1110 drrr rrrr	C
RLR R, d	Rotate left R	1	01 1100 drrr rrrr	C
SWAPR R, d	Swap halves R	1	01 1101 drrr rrrr	None
CLRA	Clear Acc	1	01 0001 0000 0000	Z
CLRR R	Clear R	1	01 0001 1rrr rrrr	Z
INCR R, d	Increment R	1	01 1000 drrr rrrr	Z
INCRSZ R, d	Increment R, Skip if 0	1 or 2(skip)	01 100 1 drrr rrrr	None
DECR R, d	Decrement R	1	01 0110 drrr rrrr	Z

TEL：886-3-5770755 FAX：886-3-5770756 E-mail：sales@jaztek.com.tw Web-site：www.jaztek.com.tw

Mnemonic Operands	Description	Cycles	Instruction Code	Status Affected
DECRSZ R, d	Decrement R, Skip if 0	1 or 2(skip)	01 0111 drrr rrrr	None
SUBAR R, d	Subtract Acc from R	1	01 1010 drrr rrrr	C, DC, Z
XORAR R, d	Exclusive OR Acc with R	1	01 1011 drrr rrrr	Z
ANDAR R, d	AND Acc with R	1	01 0100 drrr rrrr	Z
ADDAR R, d	Add Acc and R	1	01 0101 drrr rrrr	C, DC, Z
IORAR R, d	Inclusive OR Acc with R	1	01 1111 drrr rrrr	Z

Note:

b	: Bit position	WDT	: Watchdog Timer	R	: Register address
i	: Immediate data	Acc	: Accumulator	T0MODE	: T0MODE register
PD	: Power down flag	TO	: Time overflow bit	IOST	: I/O port status register
Z	: Zero flag	C	: Carry flag	DC	: Digital carry flag
I	: (i_7 i_6 i_5 i_4 i_3 i_2 i_1 i_0)	R	: (r_6 r_5 r_4 r_3 r_2 r_1 r_0)		

D ∈ [0,1] Destination:
If d is “0”, the result is stored in the Acc register.
If d is “1”, the result is stored back in register R.

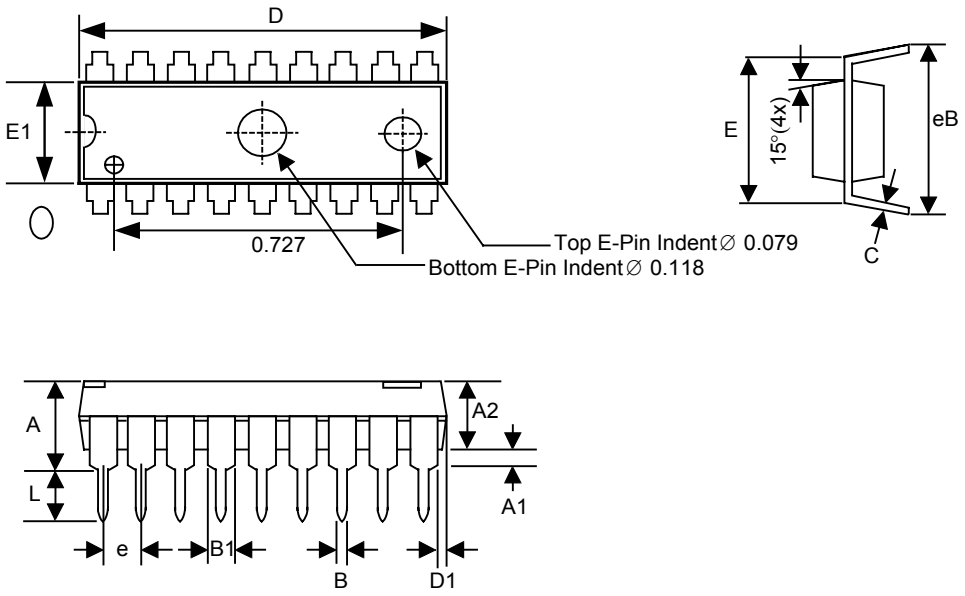
Order Information

Type	300mil PDIP	600mil PDIP	300mil SOP	Die Form
18pins	JA58560N	—	JA58560P	JA58560

TEL：886-3-5770755 FAX：886-3-5770756 E-mail：sales@jaztek.com.tw Web-site：www.jaztek.com.tw

Package Dimension

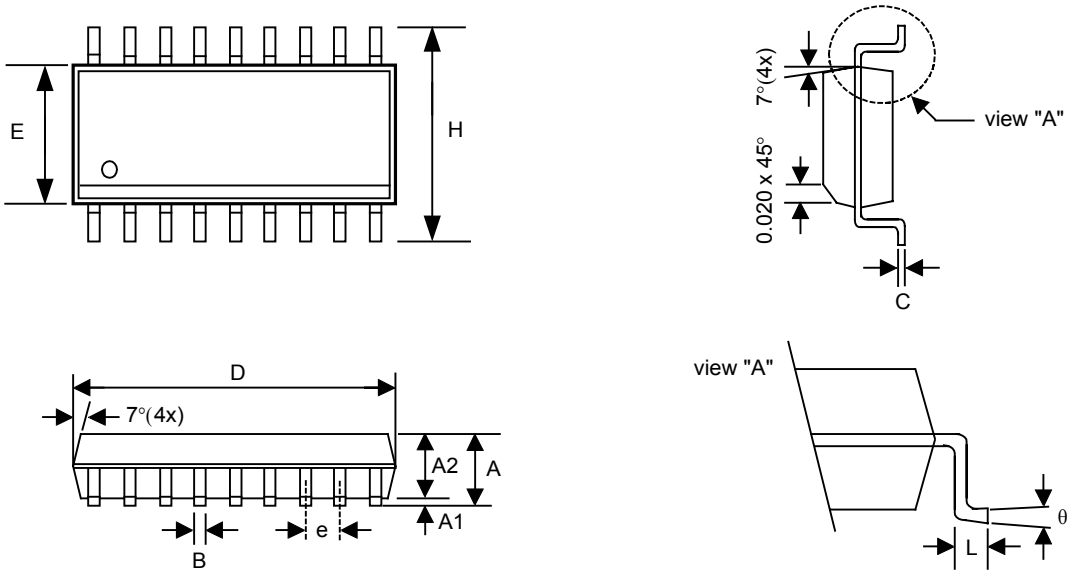
18 Pin PDIP 300mil for JA58560N



Symbol	Dimension in Millimeters			Dimension in Millimeters		
	Min	Nom	Max	Min	Nom	Max
A	—	—	4.57	—	—	0.180
A1	0.13	—	—	0.005	—	—
A2	—	0.30	3.56	—	—	0.140
B	0.36	0.46	0.56	0.014	—	0.022
B1	1.27	1.52	1.78	0.050	—	0.070
C	0.20	0.25	0.33	0.008	—	0.013
D	22.71	22.96	23.11	0.894	—	0.910
D1	0.43	0.56	0.69	0.017	—	0.027
e	7.62	—	8.26	0.300	—	0.325
E1	6.40	6.50	6.65	0.252	—	0.262
E	—	2.54	—	—	—	—
L	3.18	—	—	0.125	—	—
eB	8.38	—	9.65	0.330	—	0.380

TEL：886-3-5770755 FAX：886-3-5770756 E-mail：sales@jaztek.com.tw Web-site：www.jaztek.com.tw

18 Pin SOP for JA58560P



Symbol	Dimension in Millimeters			Dimension in Millimeters		
	Min	Nom	Max	Min	Nom	Max
A	2.36	2.49	2.64	0.093	0.098	0.104
A1	0.10	—	0.30	0.04	—	0.012
A2	—	2.31	—	—	0.091	—
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.18	0.23	0.28	0.007	0.009	0.011
D	11.35	—	11.76	0.447	—	0.463
E	7.39	7.49	7.59	0.291	0.295	0.299
e	—	1.27	—	—	0.050	—
H	10.01	10.31	10.64	0.394	0.406	0.419
L	0.38	0.81	1.27	0.015	0.032	0.050
θ	0°	—	8°	0°	—	8°

TEL：886-3-5770755 FAX：886-3-5770756 E-mail：sales@jaztek.com.tw Web-site：www.jaztek.com.tw