
HD74HC678

16-bit Address Comparator

HITACHI

Description

The HD74HC678 address comparator simplifies addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 16 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A₁ through A₇ must be low and that inputs A₈ through A₁₆ must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low. The HD74HC678 features a transparent latch and a latch enabled input (C). When C is high, the device is in the transparent mode. When C is low, the previous logic state of Y is latched.

Features

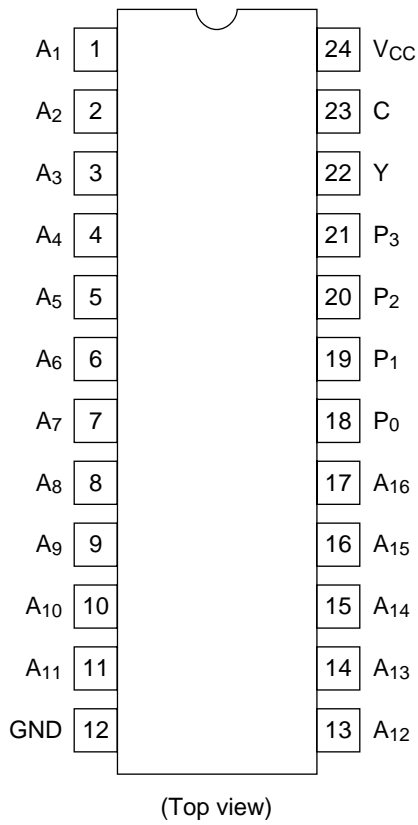
- High Speed Operation
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: $I_{CC}(\text{static}) = 4 \mu\text{A max}$ ($T_a = 25^\circ\text{C}$)

HD74HC678

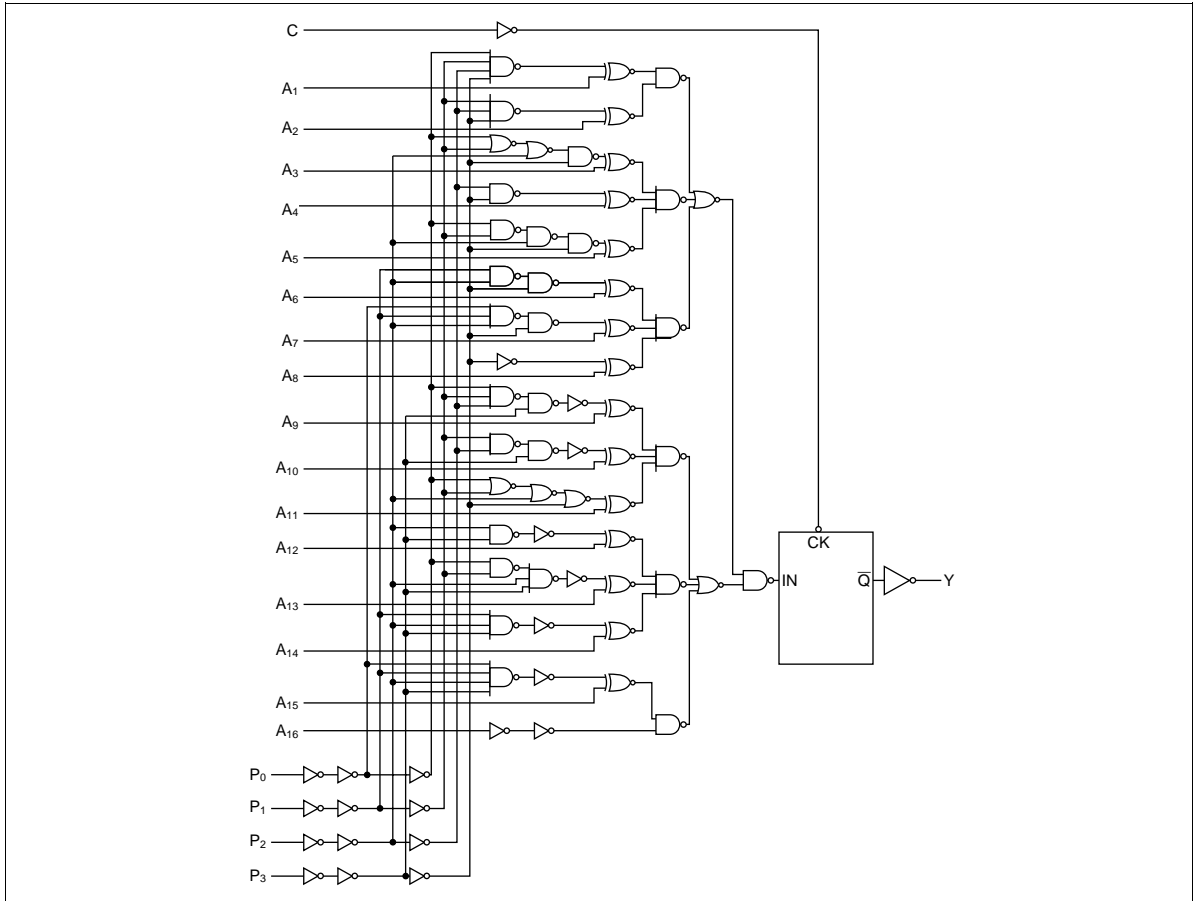
Function Table

Inputs																			Output Y		
C	P ₃	P ₂	P ₁	P ₀	A ₁	A ₂	A ₃	A ₄	A ₅	A ₆	A ₇	A ₈	A ₉	A ₁₀	A ₁₁	A ₁₂	A ₁₃	A ₁₄		A ₁₅	A ₁₆
H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	L
H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
H	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
H	H	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
H	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
H	All other combinations																			H	
L	Any combination																			Latched	

Pin Arrangement



Logic Diagram



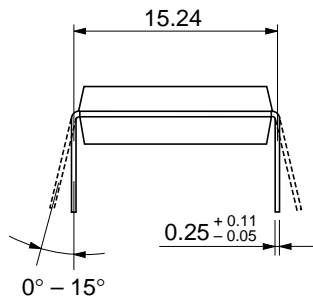
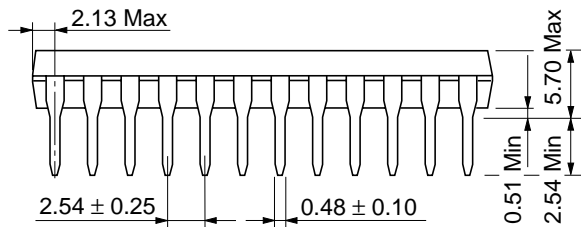
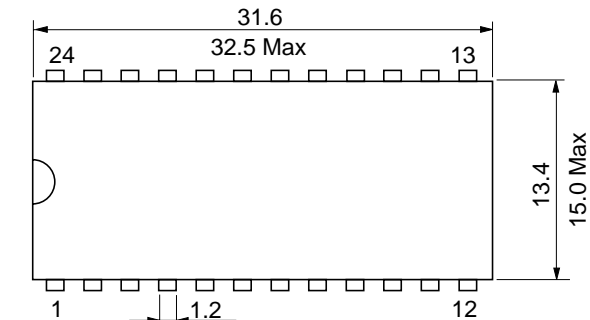
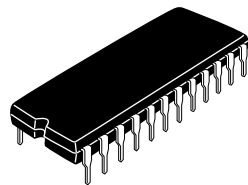
DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I _{OH} = -4 mA
		6.0	5.68	—	—	5.63	—			I _{OH} = -5.2 mA
		6.0	—	0.0	0.1	—	0.1			V
	4.5	—	0.0	0.1	—	0.1				
	6.0	—	0.0	0.1	—	0.1				
	4.5	—	—	0.26	—	0.33	I _{OL} = 4 mA			
	6.0	—	—	0.26	—	0.33	I _{OL} = 5.2 mA			
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND	
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, I _{out} = 0 μA	

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AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$		$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min			Max
Propagation delay time	t_{PLH}	2.0	—	—	330	—	410	ns	P to Y
	t_{PHL}	4.5	—	30	66	—	82		
		6.0	—	—	56	—	70		
	t_{PLH}	2.0	—	—	210	—	265	ns	A to Y
	t_{PHL}	4.5	—	21	42	—	53		
		6.0	—	—	36	—	45		
	t_{PLH}	2.0	—	—	150	—	190	ns	C to Y
	t_{PHL}	4.5	—	13	30	—	38		
		6.0	—	—	26	—	33		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	A to C
		4.5	20	12	—	25	—		
		6.0	17	—	—	21	—		
Output rise/fall time	t_{TLH}	2.0	—	—	75	—	95	ns	
	t_{THL}	4.5	—	—	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C_{in}	—	—	5	10	—	10	pF	



Hitachi Code	DP-24
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	3.1 g

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