

# RF Power Field Effect Transistor

## N-Channel Enhancement-Mode Lateral MOSFETs

Designed for Class A or Class AB base station applications with frequencies up to 1500 MHz. Suitable for analog and digital modulation and multicarrier amplifier applications.

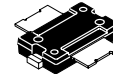
- Typical Two-Tone Performance at 960 MHz:  $V_{DD} = 28$  Volts,  $I_{DQ} = 125$  mA,  $P_{out} = 10$  Watts PEP  
 Power Gain — 18 dB  
 Drain Efficiency — 32%  
 IMD — -37 dBc
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 960 MHz, 10 Watts CW Output Power

### Features

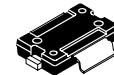
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- On-Chip RF Feedback for Broadband Stability
- Qualified Up to a Maximum of 32  $V_{DD}$  Operation
- Integrated ESD Protection
- 200°C Capable Plastic Package
- N Suffix Indicates Lead-Free Terminations. RoHS Compliant.
- In Tape and Reel. R1 Suffix = 500 Units per 24 mm, 13 inch Reel.

**MW6S010NR1**  
**MW6S010GNR1**

**450 - 1500 MHz, 10 W, 28 V**  
**LATERAL N-CHANNEL**  
**BROADBAND RF POWER MOSFETs**



**CASE 1265-08, STYLE 1**  
**TO-270-2**  
**PLASTIC**  
**MW6S010NR1**



**CASE 1265A-02, STYLE 1**  
**TO-270-2 GULL**  
**PLASTIC**  
**MW6S010GNR1**

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +68	Vdc
Gate-Source Voltage	$V_{GS}$	-0.5, +12	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	$P_D$	61.4 0.35	W W/°C
Storage Temperature Range	$T_{stg}$	- 65 to +175	°C
Operating Junction Temperature	$T_J$	200	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 10 W PEP	$R_{\theta JC}$	2.85	°C/W

1. MTF calculator available at <http://www.freescale.com/rf>. Select Tools/Software/Application Software/Calculators to access the MTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	1A
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	III

**Table 4. Moisture Sensitivity Level**

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	1	260	°C

**Table 5. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Off Characteristics**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 68\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 100\ \mu\text{Adc}$ )	$V_{GS(th)}$	1.5	2.3	3	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28\text{ Vdc}$ , $I_D = 125\text{ mAdc}$ )	$V_{GS(Q)}$	—	3.1	—	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 0.3\text{ Adc}$ )	$V_{DS(on)}$	—	0.27	0.35	Vdc

**Dynamic Characteristics**

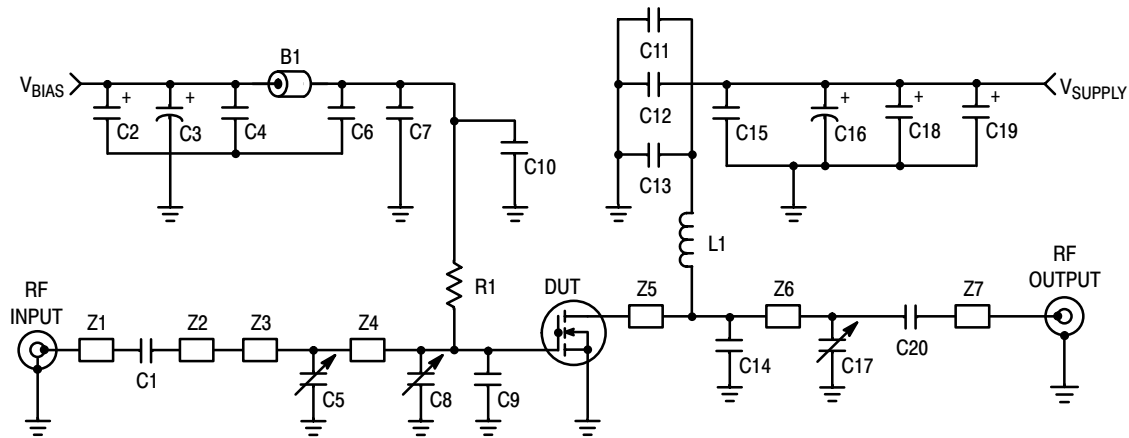
Input Capacitance ( $V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{iss}$	—	23	—	pF
Output Capacitance ( $V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{oss}$	—	10	—	pF
Reverse Transfer Capacitance ( $V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{rss}$	—	0.32	—	pF

**Functional Tests** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ} = 125\text{ mA}$ ,  $P_{out} = 10\text{ W PEP}$ ,  $f = 960\text{ MHz}$ , Two-Tone Test, 100 kHz Tone Spacing

Power Gain	$G_{ps}$	17.5	18	20.5	dB
Drain Efficiency	$\eta_D$	31	32	—	%
Intermodulation Distortion	IMD	—	-37	-33	dBc
Input Return Loss	IRL	—	-18	-10	dB

**Typical Performances** (In Freescale 450 MHz Demo Board, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ} = 150\text{ mA}$ ,  $P_{out} = 10\text{ W PEP}$ , 420-470 MHz, Two-Tone Test, 100 kHz Tone Spacing

Power Gain	$G_{ps}$	—	20	—	dB
Drain Efficiency	$\eta_D$	—	33	—	%
Intermodulation Distortion	IMD	—	-40	—	dBc
Input Return Loss	IRL	—	-10	—	dB



Z1	0.073" x 0.223" Microstrip	Z5	0.313" x 0.902" Microstrip
Z2	0.112" x 0.070" Microstrip	Z6	0.073" x 1.080" Microstrip
Z3	0.213" x 0.500" Microstrip	Z7	0.073" x 0.314" Microstrip
Z4	0.313" x 1.503" Microstrip	PCB	Rogers ULTRALAM 2000, 0.031", $\epsilon_r = 2.55$

**Figure 1. MW6S010NR1(GNR1) Test Circuit Schematic — 900 MHz**

**Table 6. MW6S010NR1(GNR1) Test Circuit Component Designations and Values — 900 MHz**

Part	Description	Part Number	Manufacturer
B1	Ferrite Bead	2743019447	Fair-Rite
C1, C6, C11, C20	47 pF Chip Capacitors	100B470JP500X	ATC
C2, C18, C19	22 $\mu$ F, 35 V Tantalum Capacitors	T491D226K035AS	Kemet
C3, C16	220 $\mu$ F, 63 V Electrolytic Capacitors, Radial	13668221	Phillips
C4, C15	0.1 $\mu$ F Chip Capacitors	CDR33BX104AKWS	Kemet
C5, C8, C17	0.8 - 8.0 pF Variable Capacitors, Gigatrim	272915L	Johanson
C7, C12	24 pF Chip Capacitors	100B240JP500X	ATC
C9, C10, C13	6.8 pF Chip Capacitors	100B6R8JP500X	ATC
C14	7.5 pF Chip Capacitor	100B7R5JP500X	ATC
L1	12.5 nH Inductor	A04T-5	Coilcraft
R1	1 k $\Omega$ Chip Resistor	CRCW12061001F100	Vishay-Dale

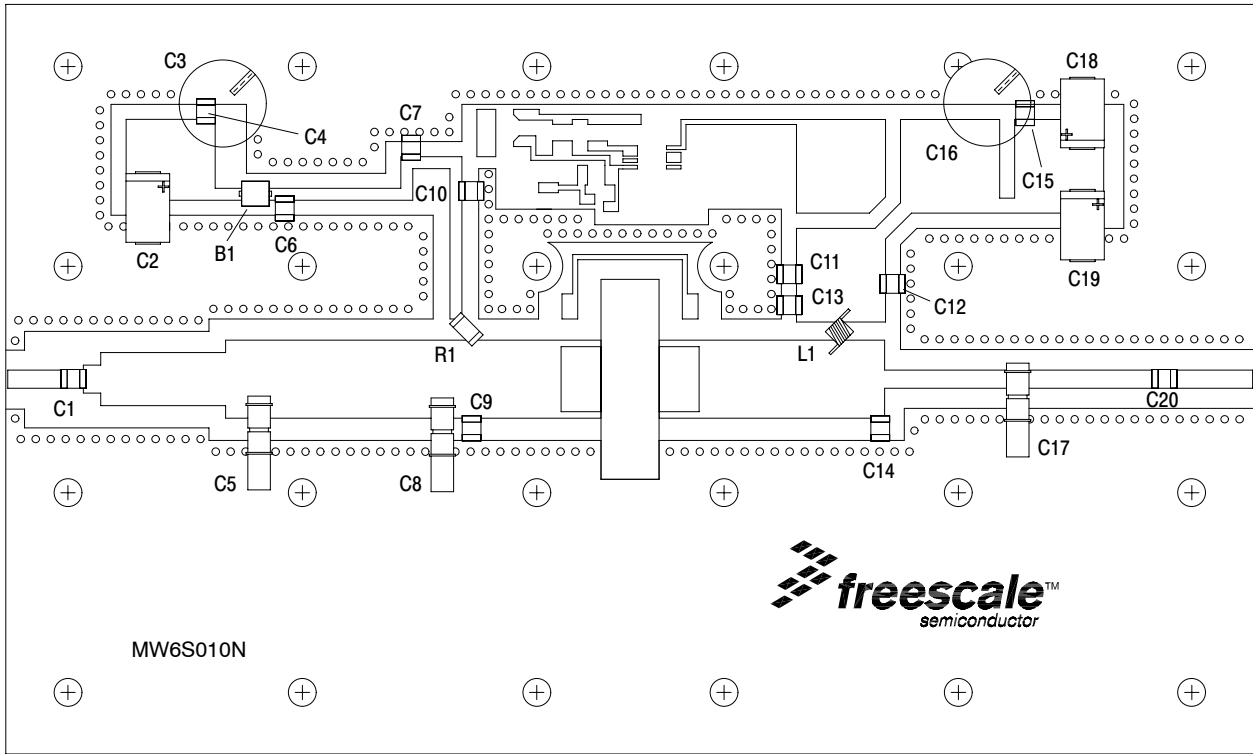
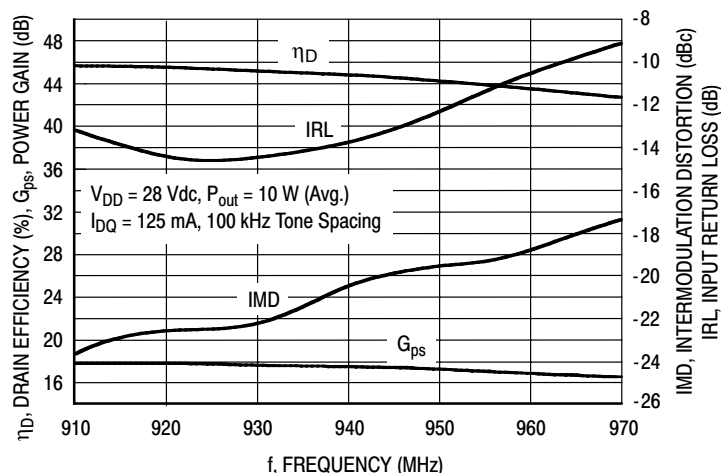
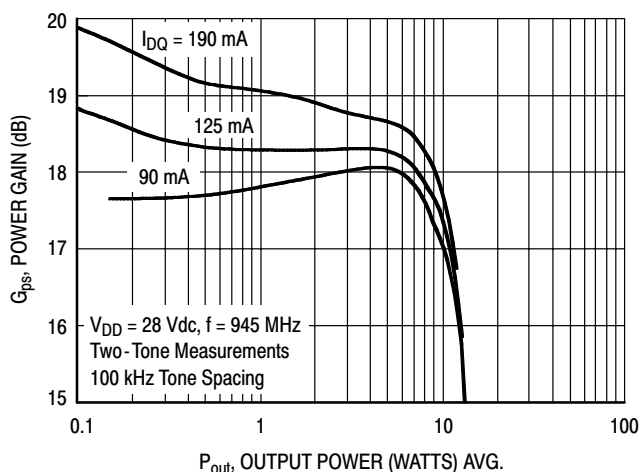


Figure 2. MW6S010NR1(GNR1) Test Circuit Component Layout — 900 MHz

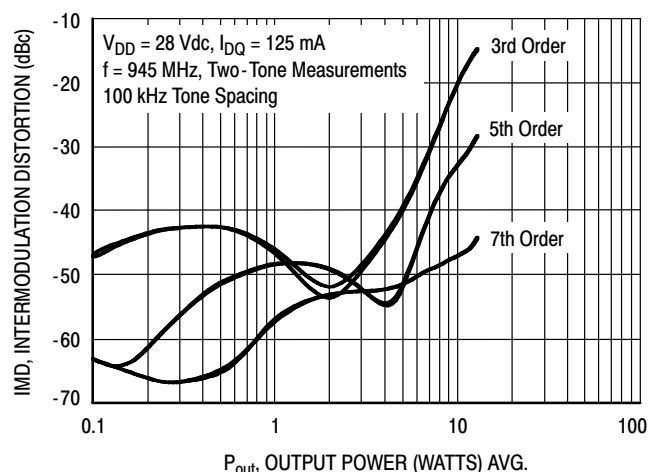
## TYPICAL CHARACTERISTICS — 900 MHz



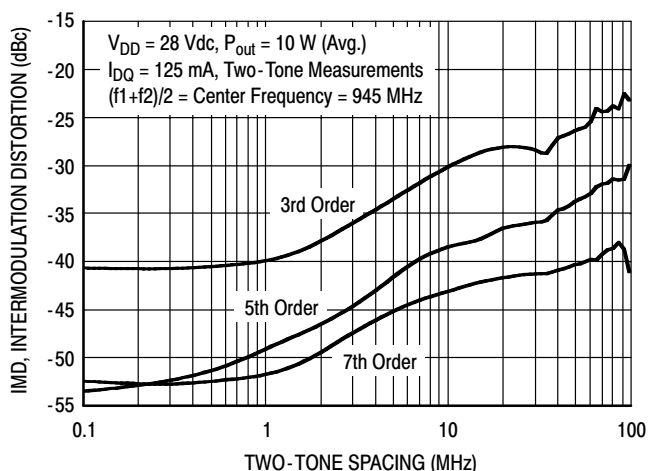
**Figure 3. Two-Tone Wideband Performance @  $P_{out} = 10$  Watts**



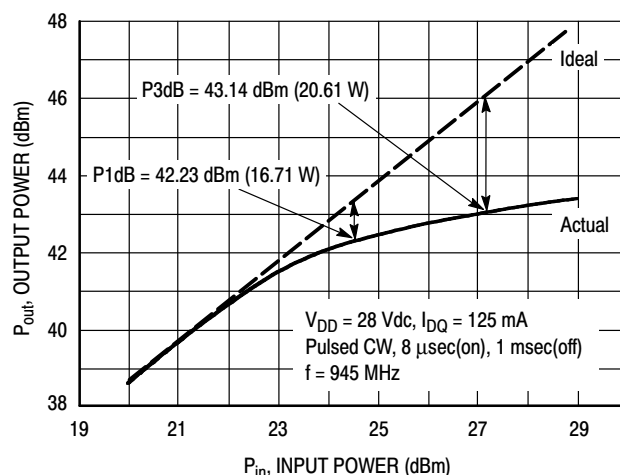
**Figure 4. Two-Tone Power Gain versus Output Power**



**Figure 5. Intermodulation Distortion Products versus Output Power**

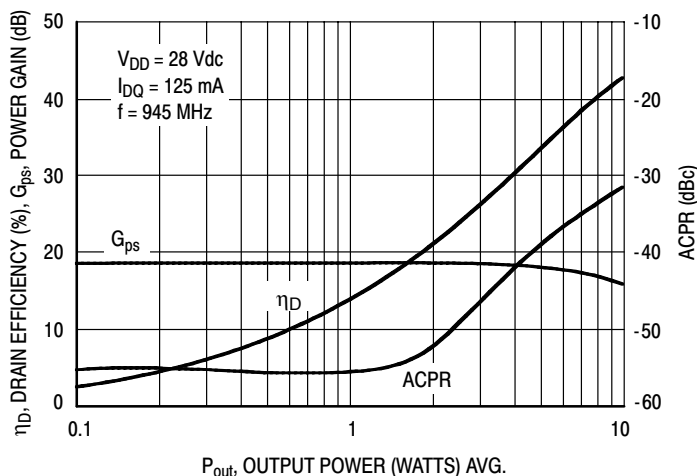


**Figure 6. Intermodulation Distortion Products versus Tone Spacing**

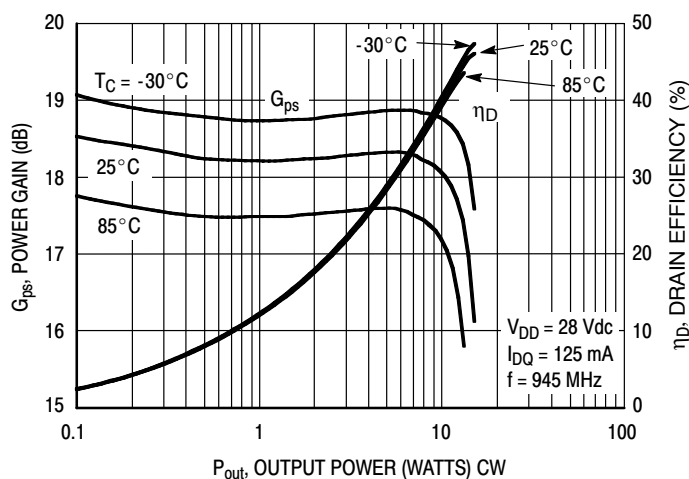


**Figure 7. Pulse CW Output Power versus Input Power**

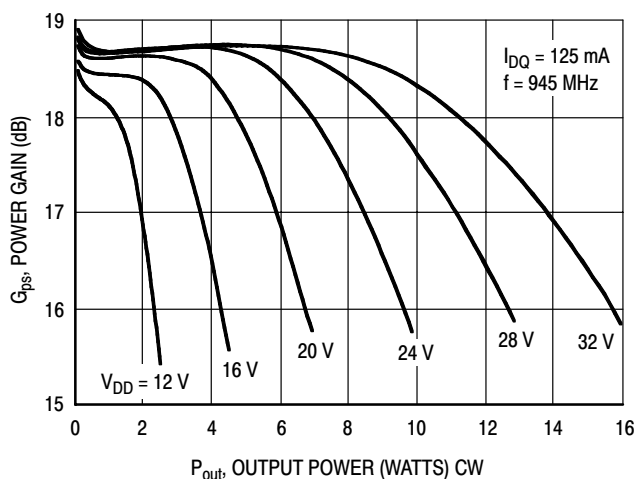
### TYPICAL CHARACTERISTICS — 900 MHz



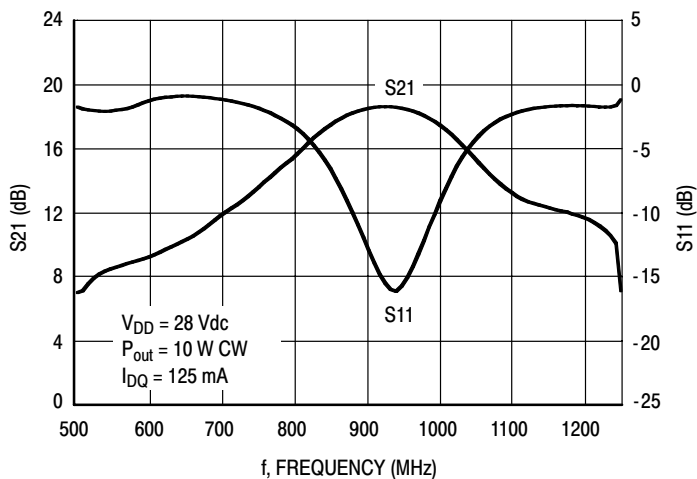
**Figure 8. Single-Carrier CDMA ACPR, Power Gain and Power Added Efficiency versus Output Power**



**Figure 9. Power Gain and Power Added Efficiency versus Output Power**

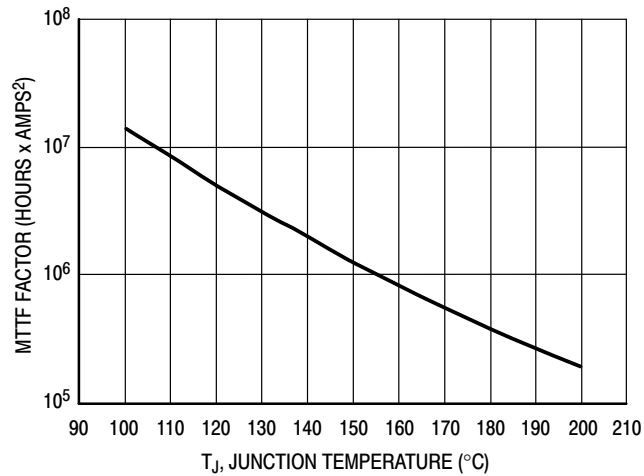


**Figure 10. Power Gain versus Output Power**



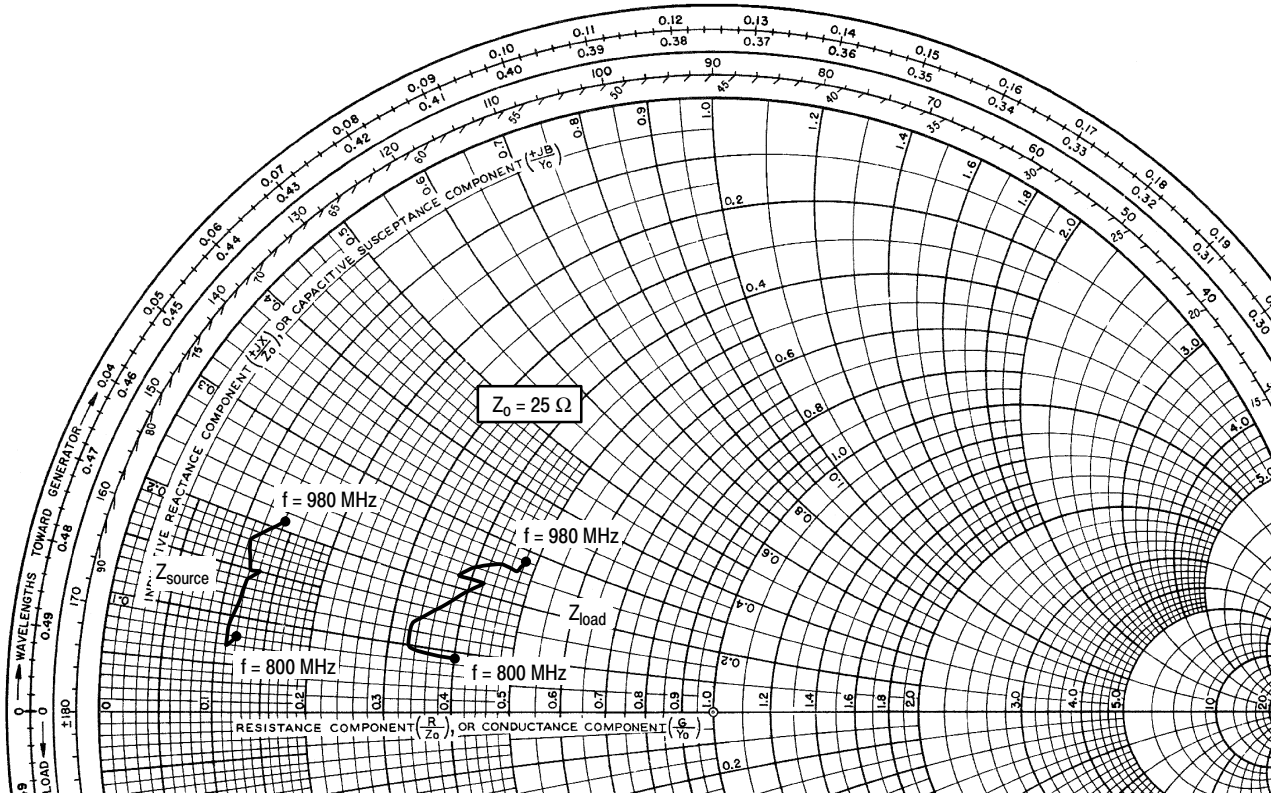
**Figure 11. Broadband Frequency Response**

## TYPICAL CHARACTERISTICS



This above graph displays calculated MTTF in hours x ampere<sup>2</sup> drain current. Life tests at elevated temperatures have correlated to better than  $\pm 10\%$  of the theoretical prediction for metal failure. Divide MTTF factor by  $I_D^2$  for MTTF in a particular application.

**Figure 12. MTTF Factor versus Junction Temperature**



$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 125 \text{ mA}$ ,  $P_{out} = 10 \text{ W PEP}$

f MHz	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
800	$3.1 + j1.9$	$10.1 + j2.3$
820	$2.8 + j1.7$	$8.3 + j2.5$
840	$2.7 + j2.2$	$8.2 + j3.3$
860	$3.1 + j3.4$	$9.8 + j4.8$
880	$3.3 + j3.8$	$10.6 + j5.6$
900	$2.9 + j3.7$	$9.5 + j5.5$
920	$2.8 + j4.4$	$10.1 + j5.9$
940	$3.0 + j4.7$	$11.0 + j6.4$
960	$3.2 + j4.9$	$11.8 + j6.6$
980	$3.6 + j5.2$	$12.1 + j7.1$

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

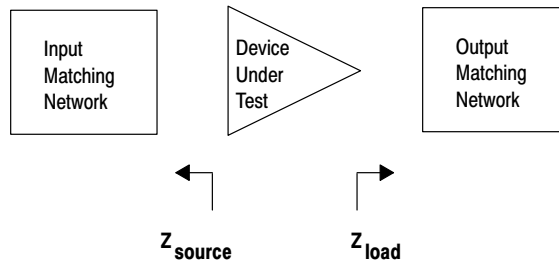
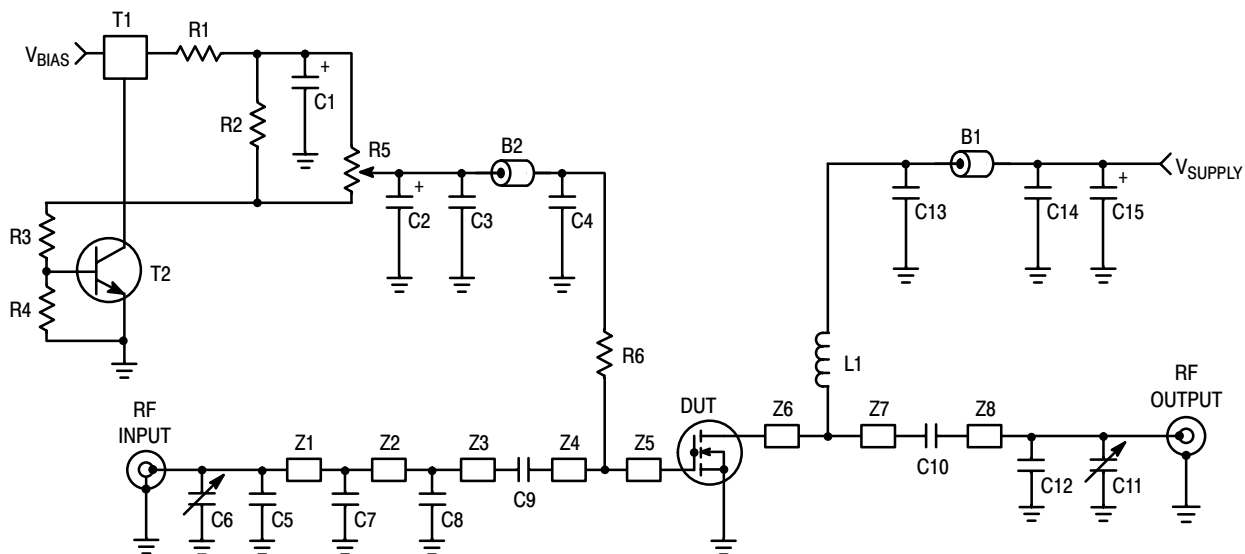


Figure 13. Series Equivalent Source and Load Impedance — 900 MHz





Z1	0.540" x 0.080" Microstrip	Z5	0.475" x 0.330" Microstrip
Z2	0.365" x 0.080" Microstrip	Z6	0.475" x 0.325" Microstrip
Z3	0.225" x 0.080" Microstrip	Z8	1.250" x 0.080" Microstrip
Z4, Z7	0.440" x 0.080" Microstrip	PCB	Rogers ULTRALAM 2000, 0.030", $\epsilon_r = 2.55$

**Figure 14. MW6S010NR1(GNR1) Test Circuit Schematic — 450 MHz**

**Table 7. MW6S010NR1(GNR1) Test Circuit Component Designations and Values — 450 MHz**

Part	Description	Part Number	Manufacturer
B1, B2	Ferrite Bead	2743019447	Fair-Rite
C1	1 $\mu$ F, 35 V Tantalum Capacitor	T491C105K050AS	Kemet
C2, C15	22 $\mu$ F, 35 V Tantalum Capacitors	T491X226K035AS	Kemet
C3, C14	0.1 $\mu$ F Chip Capacitors	C1210C104K5RACTR	Kemet
C4, C9, C10, C13	330 pF Chip Capacitors	700A331JP150X	ATC
C5	4.3 pF Chip Capacitor	100B4R3JP500X	ATC
C6, C11	0.6-8.0 pF Variable Capacitors	27291SL	Johanson
C7, C8, C12	4.7 pF Chip Capacitors	100B4R7JP500X	ATC
L1	39 $\mu$ H Chip Inductor	ISC-1210	Vishay-Dale
R1	10 $\Omega$ Chip Resistor (0805)	CRCW080510R0F100	Vishay-Dale
R2	1 k $\Omega$ Chip Resistor (0805)	CRCW08051001F100	Vishay-Dale
R3	1.2 k $\Omega$ Chip Resistor (0805)	CRCW08051201F100	Vishay-Dale
R4	2.2 k $\Omega$ Chip Resistor (0805)	CRCW08052201F100	Vishay-Dale
R5	5 k $\Omega$ Potentiometer	1224W	Bourns
R6	1 k $\Omega$ Chip Resistor (1206)	CRCW12061001F100	Vishay-Dale
T1	5 Volt Regulator, Micro 8	LP2951	On Semiconductor
T2	NPN Transistor	BC847ALT1	On Semiconductor

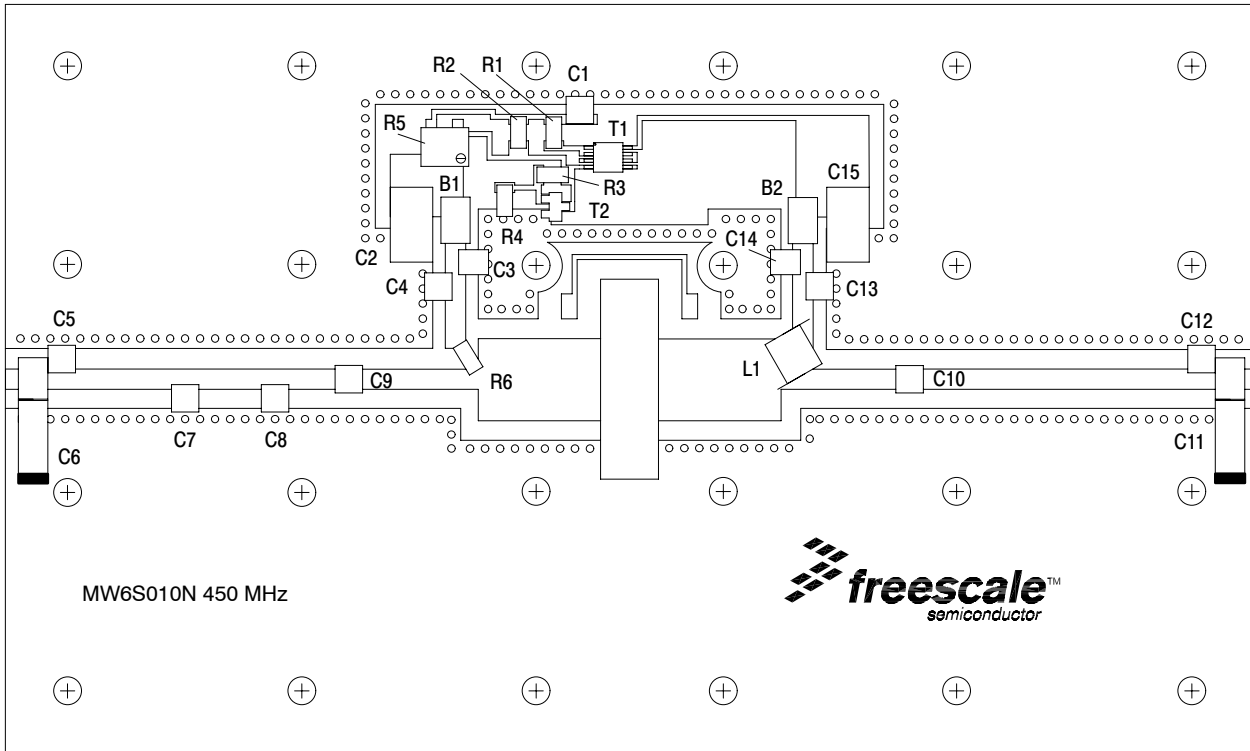


Figure 15. MW6S010NR1(GNR1) Test Circuit Component Layout — 450 MHz

### TYPICAL CHARACTERISTICS — 450 MHz

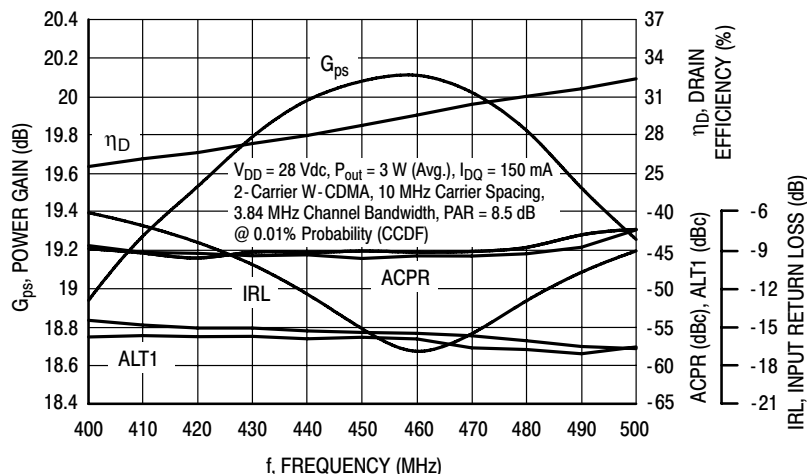


Figure 16. 2-Carrier W-CDMA Broadband Performance @  $P_{out} = 3$  Watts Avg.

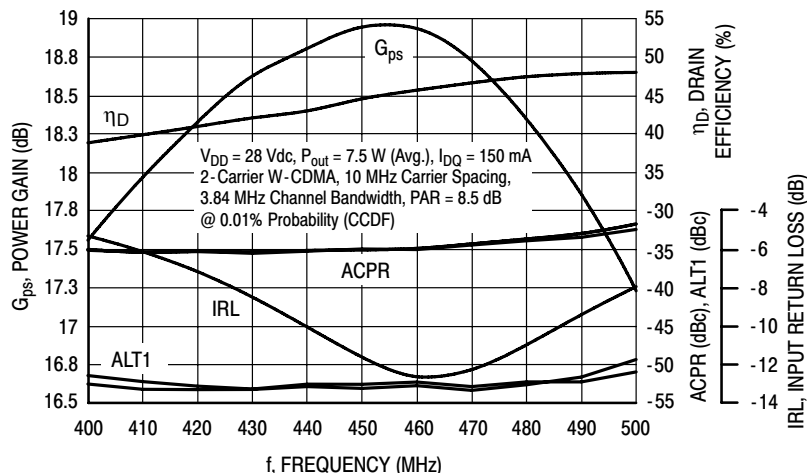


Figure 17. 2-Carrier W-CDMA Broadband Performance @  $P_{out} = 7.5$  Watts Avg.

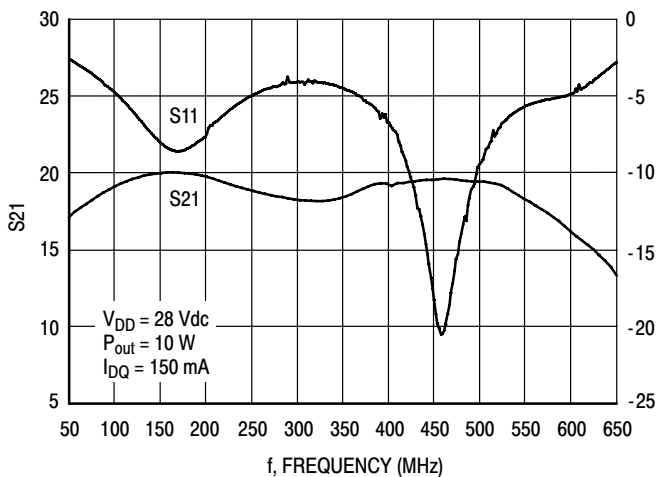


Figure 18. Broadband Frequency Response

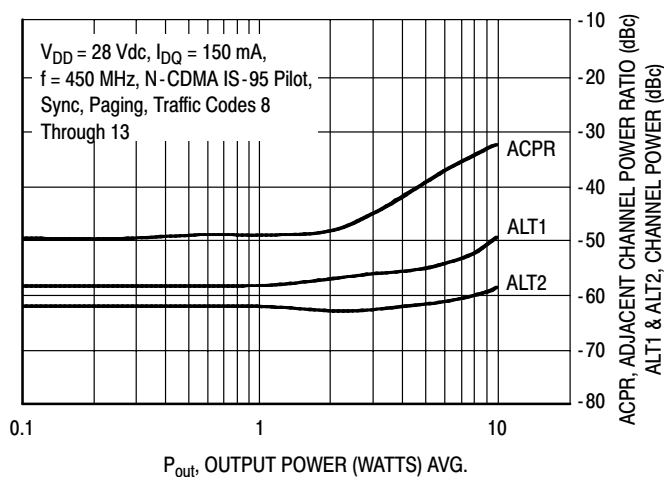
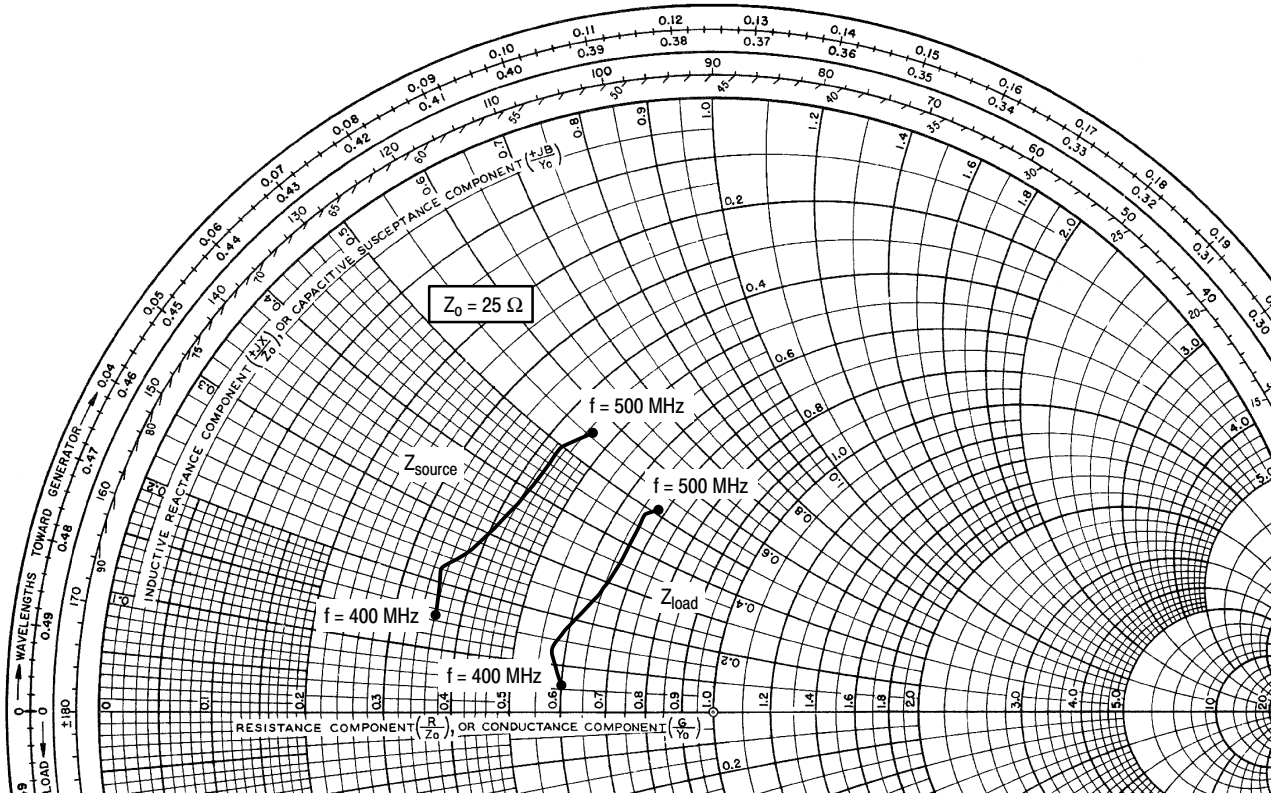


Figure 19. Single-Carrier N-CDMA ACPR, ALT1 and ALT2 versus Output Power



$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 150 \text{ mA}$ ,  $P_{out} = 10 \text{ W PEP}$

f MHz	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
400	$9.0 + j3.8$	$15.0 + j1.4$
420	$8.8 + j5.4$	$14.3 + j3.3$
440	$9.6 + j6.6$	$15.0 + j4.7$
460	$10.6 + j9.5$	$16.3 + j7.3$
480	$10.7 + j12.6$	$16.4 + j11.1$
500	$11.5 + j13.9$	$16.9 + j12.7$

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

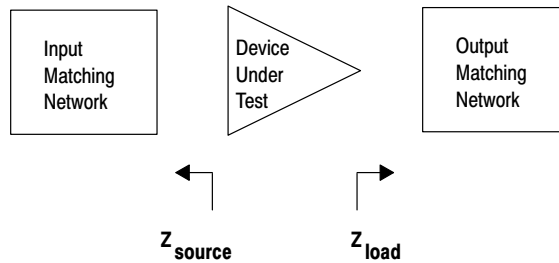


Figure 20. Series Equivalent Source and Load Impedance — 450 MHz



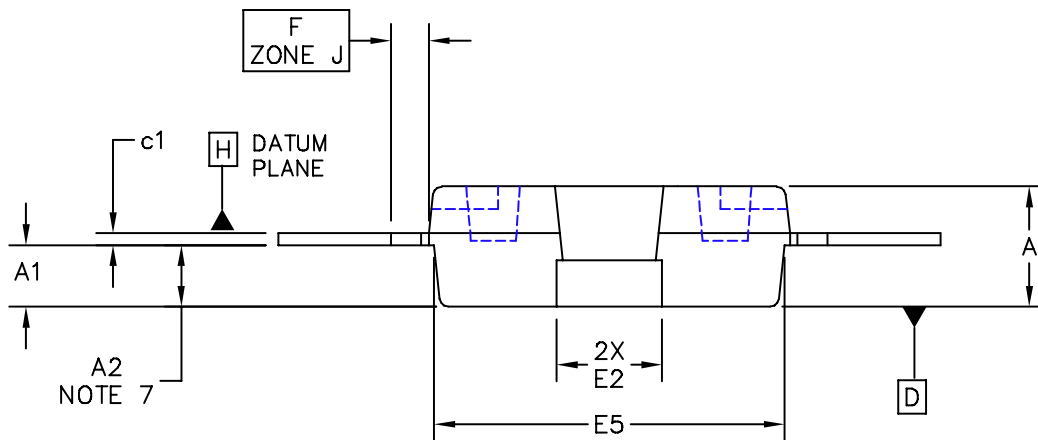
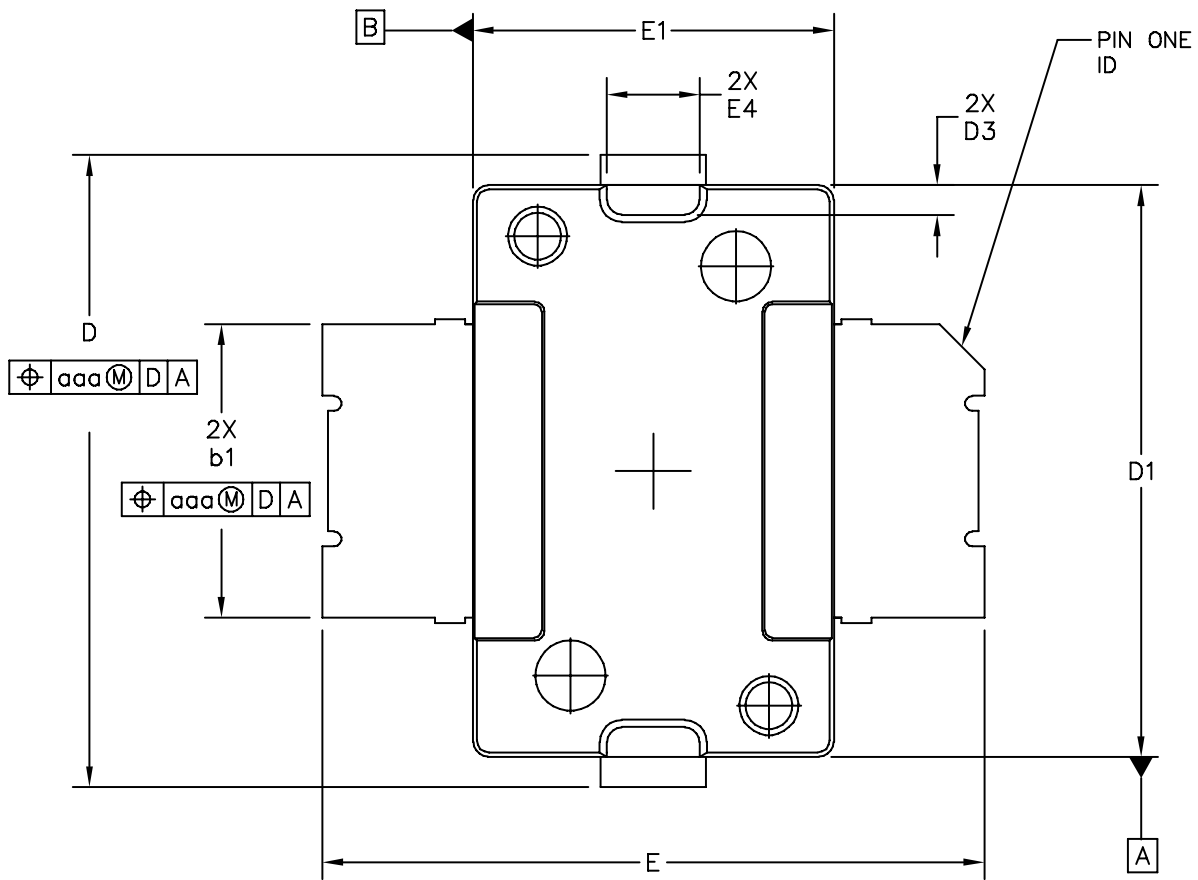
# NOTES

# NOTES



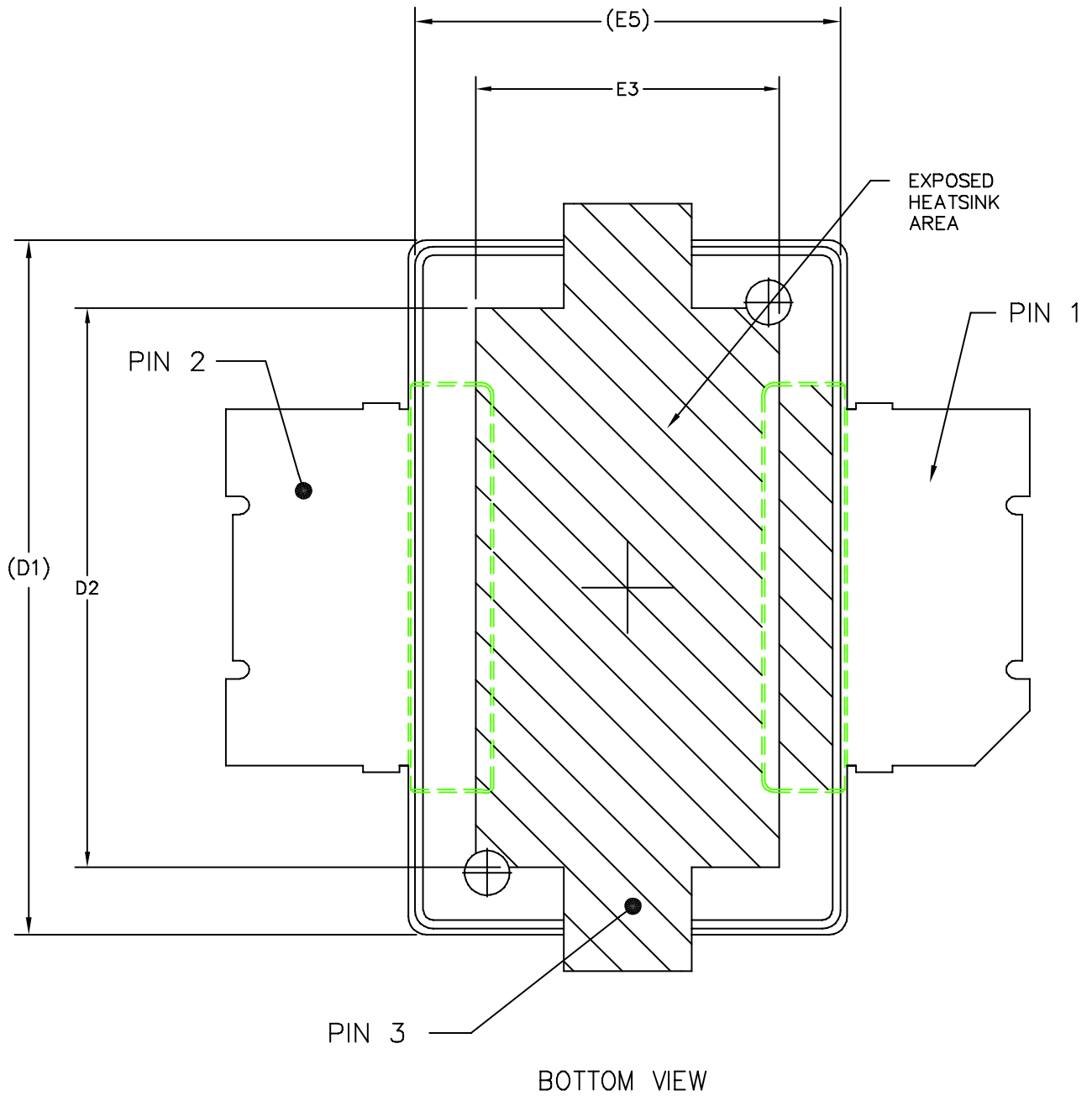
# NOTES

**PACKAGE DIMENSIONS**



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TITLE: <div style="text-align: center;"> <p>TO-270 SURFACE MOUNT</p> </div>	DOCUMENT NO: 98ASH98117A	REV: J	
	CASE NUMBER: 1265-08	01 APR 2005	
	STANDARD: NON-JEDEC		





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TITLE: <div style="text-align: center; padding: 5px;"> <b>TO-270 SURFACE MOUNT</b> </div>	DOCUMENT NO: 98ASH98117A	REV: J	
	CASE NUMBER: 1265-08	01 APR 2005	
	STANDARD: NON-JEDEC		

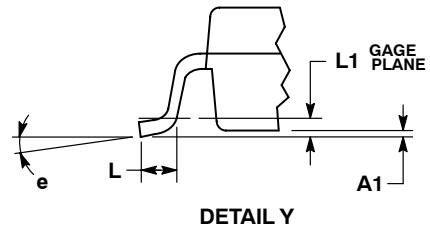
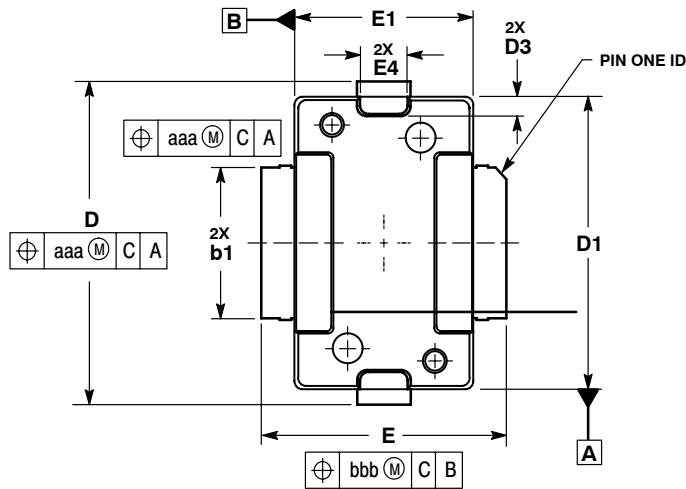
**MW6S010NR1 MW6S010GNR1**

NOTES:

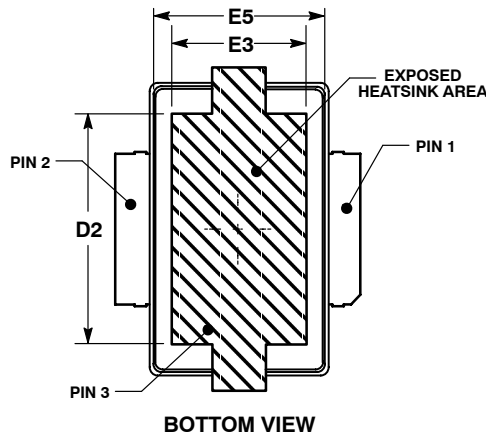
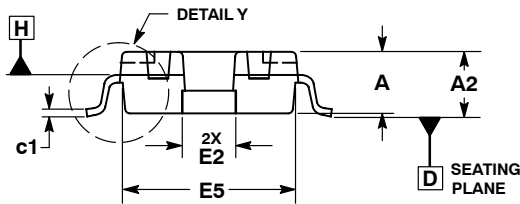
1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D1 AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION "A2" APPLIES WITHIN ZONE "J" ONLY.
8. DIMENSIONS "D" AND "E2" DO NOT INCLUDE MOLD PROTRUSION. OVERALL LENGTH INCLUDING MOLD PROTRUSION SHOULD NOT EXCEED 0.430 INCH FOR DIMENSION "D" AND 0.080 INCH FOR DIMENSION "E2". DIMENSIONS "D" AND "E2" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -D-.

STYLE 1:  
 PIN 1 - DRAIN  
 PIN 2 - GATE  
 PIN 3 - SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.078	.082	1.98	2.08	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b1	.193	.199	4.90	5.06
A2	.040	.042	1.02	1.07	c1	.007	.011	0.18	0.28
D	.416	.424	10.57	10.77	aaa	.004		0.10	
D1	.378	.382	9.60	9.70					
D2	.290	.320	7.37	8.13					
D3	.016	.024	0.41	0.61					
E	.436	.444	11.07	11.28					
E1	.238	.242	6.04	6.15					
E2	.066	.074	1.68	1.88					
E3	.150	.180	3.81	4.57					
E4	.058	.066	1.47	1.68					
E5	.231	.235	5.87	5.97					
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.			<b>MECHANICAL OUTLINE</b>			PRINT VERSION NOT TO SCALE			
TITLE:  TO-270 SURFACE MOUNT					DOCUMENT NO: 98ASH98117A			REV: J	
					CASE NUMBER: 1265-08			01 APR 2005	
					STANDARD: NON-JEDEC				



- NOTES:
1. CONTROLLING DIMENSION: INCH.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
  3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
  4. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D1" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
  5. DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b1 DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
  7. DIMENSIONS "D" AND "E2" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .003 PER SIDE. DIMENSIONS "D" AND "E2" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -D-.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.078	.082	1.98	2.08
A1	.001	.004	0.02	0.10
A2	.077	.088	1.96	2.24
D	.416	.424	10.57	10.77
D1	.378	.382	9.60	9.70
D2	.290	.320	7.37	8.13
D3	.016	.024	0.41	0.61
E	.316	.324	8.03	8.23
E1	.238	.242	6.04	6.15
E2	.066	.074	1.68	1.88
E3	.150	.180	3.81	4.57
E4	.058	.066	1.47	1.68
E5	.231	.235	5.87	5.97
L	.018	.024	4.90	5.06
L1	.01 BSC		0.25 BSC	
b1	.193	.199	4.90	5.06
c1	.007	.011	0.18	0.28
e	2°		8°	
aaa	.004		0.10	

- STYLE 1:  
 PIN 1. DRAIN  
 PIN 2. GATE  
 PIN 3. SOURCE

**CASE 1265A-02  
 ISSUE B  
 TO-270-2 GULL  
 PLASTIC  
 MW6S010GNR1**

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