19-3381; Rev 0; 8/04

2-Wire-Interfaced, 16-Bit, I/O Port Expander with Interrupt and Hot-Insertion Protection

General Description

The MAX7318 2-wire-interfaced expander provides 16-bit parallel input/output (I/O) port expansion for SMBus™ and I^{2}C™ applications. The MAX7318 consists of input port registers, output port registers, polarity inversion registers, configuration registers, a bus timeout register, and an I^{2}C-compatible serial interface logic compatible with SMBus. The system master can invert the MAX7318 input data by writing to the active-high polarity inversion register.

Any of the 16 I/O ports can be configured as an input or output. A power-on reset (POR) initializes the 16 I/Os as inputs. Three address select pins configure one of 64 slave ID addresses.

The MAX7318 supports hot insertion. All port pins, the $\overline{\text{INT}}$ output, SDA, SCL, and the slave address inputs AD0–2 remain high impedance in power-down (V+ = 0V) with up to 6V asserted upon them.

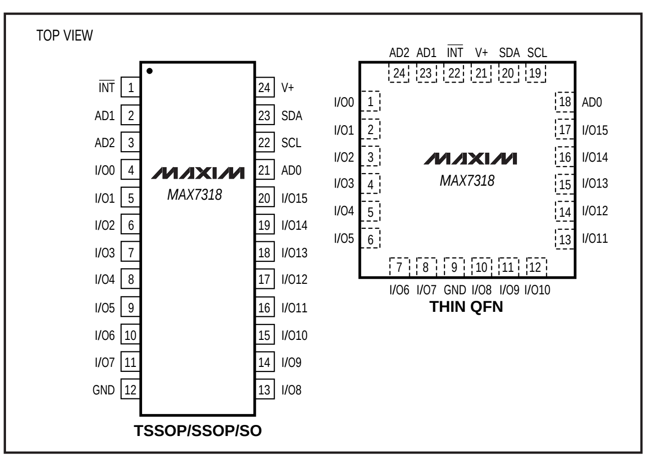
The MAX7318 is available in 24-pin SO, SSOP, TSSOP, and thin QFN packages and is specified over the -40°C to +125°C automotive temperature range.

For applications requiring an SMBus timeout function, refer to the MAX7311 data sheet.

Applications

- Servers
- RAID Systems
- Industrial Control
- Medical Equipment
- PLCs
- Instrumentation and Test Measurement

Pin Configurations



Features

- ♦ **400kbps I^{2}C-Compatible Serial Interface**
- ♦ **2V to 5.5V Operation**
- ♦ **5.5V Overvoltage-Tolerant I/Os**
- ♦ **Supports Hot Insertion**
- ♦ **16 I/O Pins that Default to Inputs on Power-Up**
- ♦ **100kΩ Pullup on Each I/O**
- ♦ **Open-Drain Interrupt Output ($\overline{\text{INT}}$)**
- ♦ **Noise Filter on SCL/SDA Inputs**
- ♦ **64 Slave ID Addresses Available**
- ♦ **Low Standby Current (5.4µA typ)**
- ♦ **Polarity Inversion**
- ♦ **4mm × 4mm, 0.8mm Thin QFN Package**
- ♦ **-40°C to +125°C Operation**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX7318AWG	-40°C to +125°C	24 Wide SO	—
MAX7318AAG	-40°C to +125°C	24 SSOP	—
MAX7318ATG	-40°C to +125°C	24 Thin QFN (4mm × 4mm)	T2444-4
MAX7318AUG	-40°C to +125°C	24 TSSOP	—

ABSOLUTE MAXIMUM RATINGS

V+ to GND ....-0.3V to +6V
I/O0–I/O15 as Inputs ....(GND - 0.3V) to +6V
SCL, SDA, AD0, AD1, AD2, $\overline{\text{INT}}$..................(GND - 0.3V) to +6V
Maximum V+ Current...+250mA
Maximum GND Current ....-250mA
DC Input Current on I/O0–I/O15 ....±20mA
DC Output Current on I/O0–I/O15 ....±80mA

Continuous Power Dissipation (T_A = +70°C)
24-Pin Wide SO (derate 11.8mW/°C above +70°C) 941mW
24-Pin SSOP (derate 8.0mW/°C above +70°C) 640mW
24-Pin TSSOP (derate 12.2mW/°C above +70°C) 976mW
24-Pin Thin QFN (derate 20.8mW/°C above +70°C) .1667mW
Operating Temperature Range ....-40°C to +125°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V+ = 2V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V+			2.0		5.5	V
Supply Current	I^+	All I/Os unloaded, f_{SCL} = 400kHz	V+ = 2V		24	36	µA
			V+ = 3.3V		45	62	
			V+ = 5.5V		83	124	
Standby Current	I_{STBY}	All I/Os unloaded, f_{SCL} = 0	V+ = 2V		4.8	12.1	µA
			V+ = 3.3V		5.4	14.4	
			V+ = 5.5V		6.4	19.4	
Power-On Reset Voltage	V_{POR}				1.4	1.7	V
SCL, SDA							
Input Voltage Low	V_{IL}					0.3 x V+	V
Input Voltage High	V_{IH}			0.7 x V+			V
Low-Level Output Voltage	V_{OL}	I_{SINK} = 6mA				0.4	V
Leakage Current	I_L			-1		+1	µA
Input Capacitance					10		pF
I/O_							
Input Voltage Low	V_{IL}					0.8	V
Input Voltage High	V_{IH}			1.8			V
Input Leakage Current		T_A = -40°C to +85°C; includes internal pullup current, V_{IO} = V+				1	µA
Internal Pullup Current		T_A = -40°C to +85°C, V_{IO} = 0			34	100	µA
Low-Level Output Current	I_{SINK}	V+ = 2V, V_{OL} = 0.5V		8.5	17		mA
		V+ = 3.3V, V_{OL} = 0.5V		17	32		
		V+ = 5V, V_{OL} = 0.5V			43		
High Output Current	I_{SOURCE}	V+ = 3.3V, V_{OH} = 2.4V		29	41		mA
		V+ = 5V, V_{OH} = 4.5V			31		
AD0, AD1, AD2							
Input Voltage Low	V_{IL}					0.3 x V+	V
Input Voltage High	V_{IH}			0.7 x V+			V

DC ELECTRICAL CHARACTERISTICS (continued)

(V+ = 2V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Leakage Current			-1		+1	µA
Input Capacitance				4		pF
$\overline{\text{INT}}$						
Low-Level Output Current	I_{OL}	V_{OL} = 0.4V	6			mA

AC ELECTRICAL CHARACTERISTICS

(V+ = 2V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted.) (Note 1)

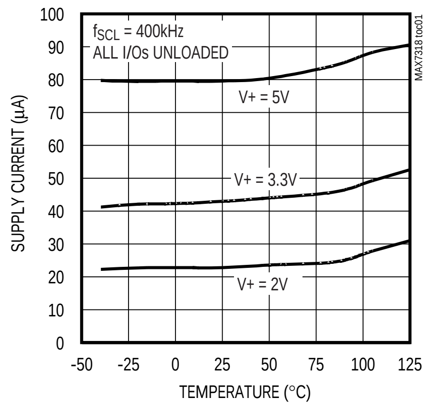
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}					400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}	Figure 2		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$	Figure 2		0.6			µs
Repeated START Condition Setup Time	$t_{SU,STA}$	Figure 2		0.6			µs
STOP Condition Setup Time	$t_{SU,STO}$	Figure 2		0.6			µs
Data Hold Time	$t_{HD,DAT}$	Figure 2 (Note 2)				0.9	µs
Data Setup Time	$t_{SU,DAT}$	Figure 2		100			ns
SCL Low Period	t_{LOW}	Figure 2		1.3			µs
SCL High Period	t_{HIGH}	Figure 2		0.7			µs
SDA Fall Time	t_F	Figure 2 (Notes 3, 4)	V+ < 3.3V			500	ns
			V+ ≥ 3.3V			250	
Pulse Width of Spike Suppressed	t_{SP}	(Note 5)			50		ns
PORT TIMING							
Output Data Valid	t_{PV}	Figure 7				3	µs
Input Data Setup Time				27			µs
Input Data Hold Time				0			µs
INTERRUPT TIMING							
Interrupt Valid	t_{IV}	Figure 9				30.5	µs
Interrupt Reset	t_{IR}	Figure 9				2	µs

Note 1: All parameters are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: A master device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IL} of the SCL signal) to bridge the undefined region SCL's falling edge.
Note 3: C_B = total capacitance of one bus line in pF.
Note 4: The maximum t_F for the SDA and SCL bus lines is specified at 300ns. The maximum fall time for the SDA output stage t_F is specified at 250ns. This allows series protection resistors to be connected between the SDA and SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_F.
Note 5: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

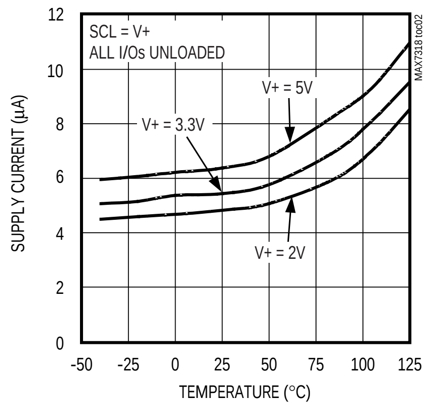
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

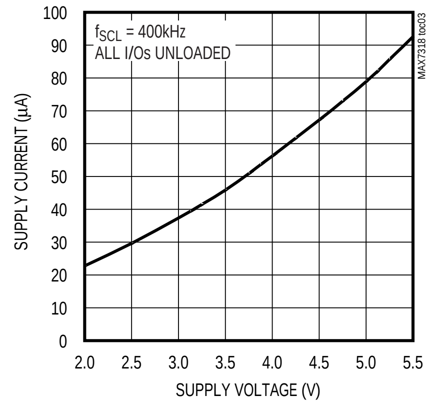
SUPPLY CURRENT vs. TEMPERATURE



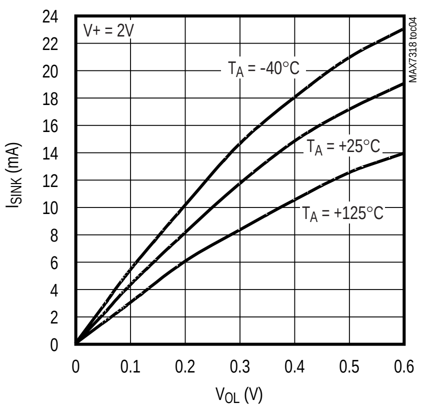
STANDBY SUPPLY CURRENT vs. TEMPERATURE



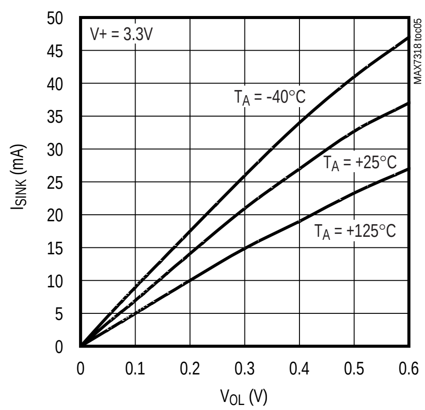
SUPPLY CURRENT vs. SUPPLY VOLTAGE



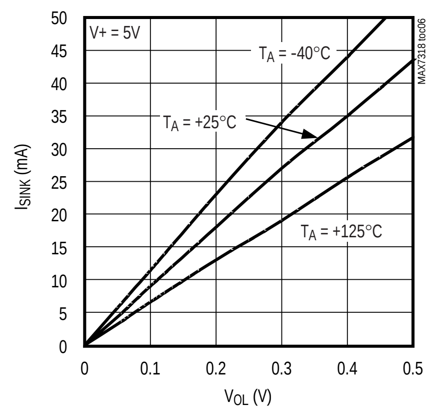
I/O SINK CURRENT vs. OUTPUT LOW VOLTAGE



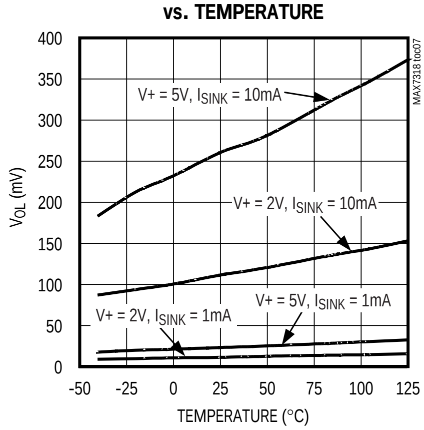
I/O SINK CURRENT vs. OUTPUT LOW VOLTAGE



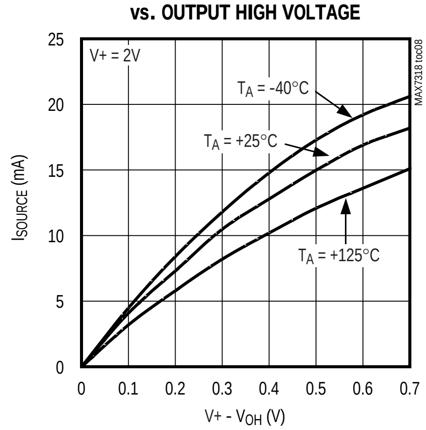
I/O SINK CURRENT vs. OUTPUT LOW VOLTAGE



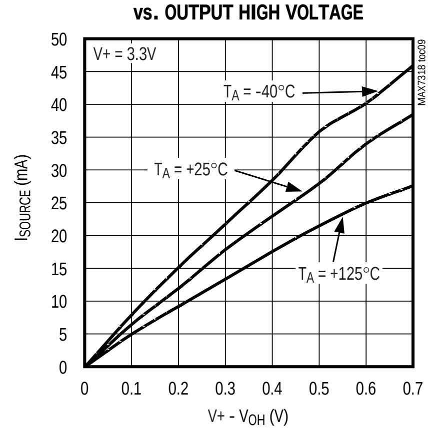
I/O OUTPUT LOW VOLTAGE vs. TEMPERATURE



I/O SOURCE CURRENT vs. OUTPUT HIGH VOLTAGE

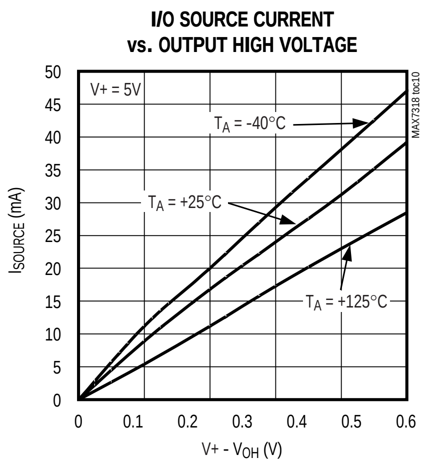


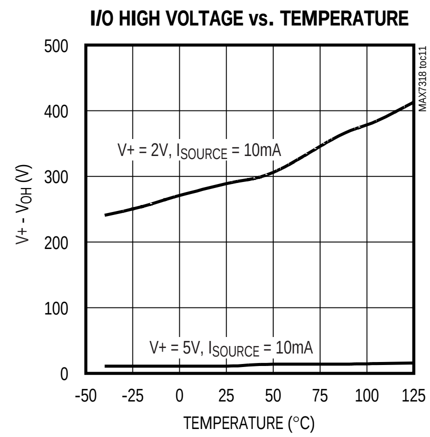
I/O SOURCE CURRENT vs. OUTPUT HIGH VOLTAGE



Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)





Pin Description

PIN		NAME	FUNCTION
TSSOP/SSOP/SO	THIN QFN		
1	22	$\overline{\text{INT}}$	Interrupt Output (Open Drain)
2	23	AD1	Address Input 1
3	24	AD2	Address Input 2
4–11	1–8	I/O0–I/O7	Input/Output Port 1
12	9	GND	Supply Ground
13–20	10–17	I/O8–I/O15	Input/Output Port 2
21	18	AD0	Address Input 0
22	19	SCL	Serial Clock Line
23	20	SDA	Serial Data Line
24	21	V+	Supply Voltage. Bypass with a 0.047µF capacitor to GND.
—	—	EP	Exposed Pad on Package Underside. Connect to GND.

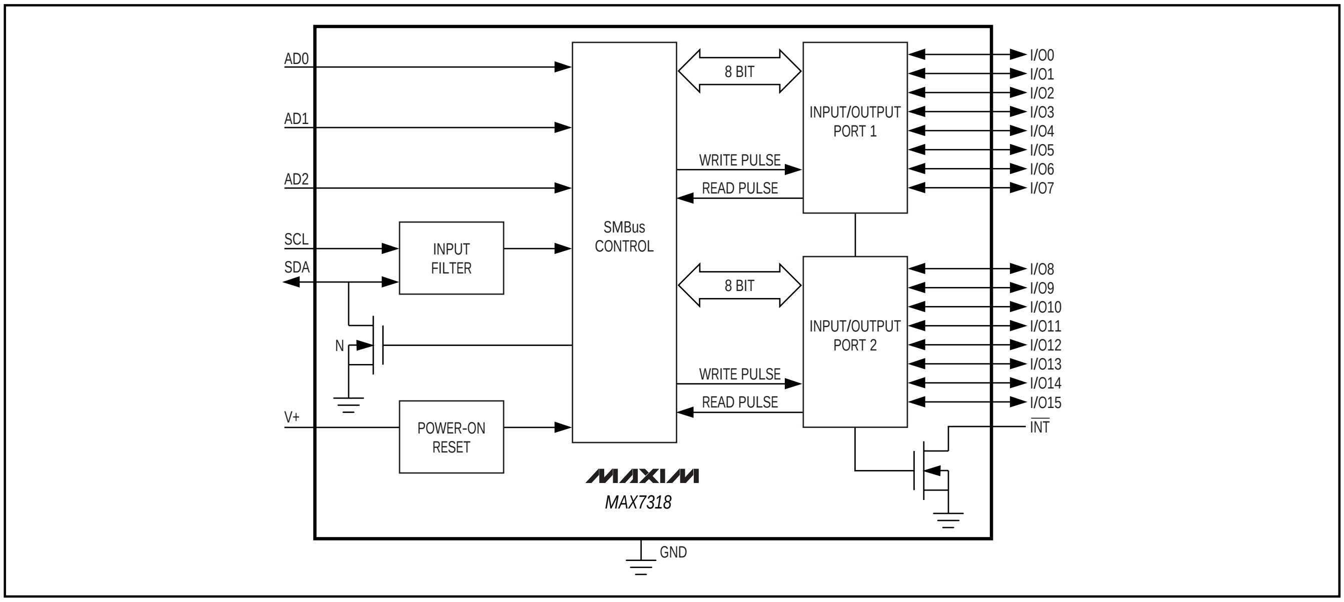


Figure 1. MAX7318 Block Diagram

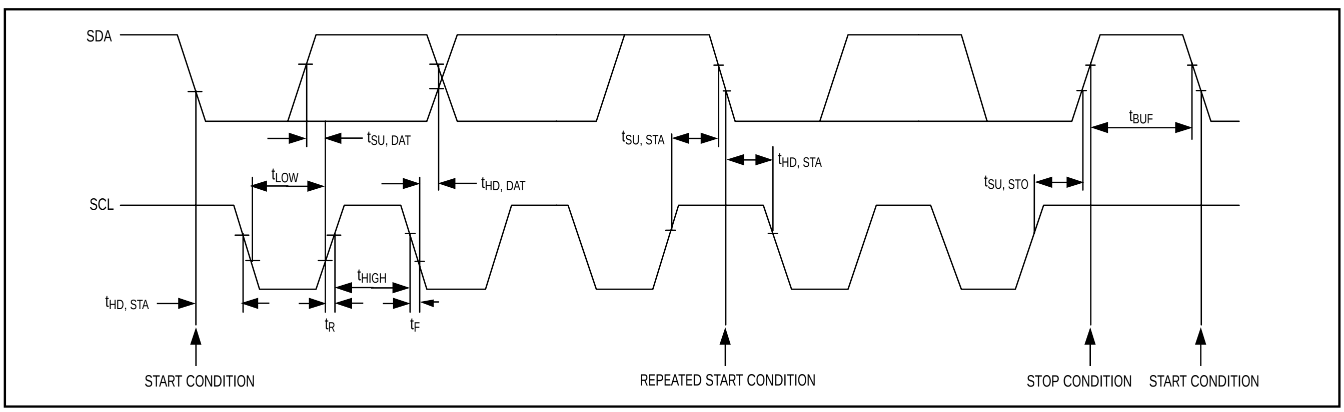


Figure 2. 2-Wire Serial Interface Timing Diagram

Detailed Description

The MAX7318 general-purpose input/output (GPIO) peripheral provides up to 16 I/O ports, controlled through an I^2C-compatible serial interface. The MAX7318 consists of input port registers, output port registers, polarity inversion registers, and configuration registers. Upon power-on, all I/O lines are set as inputs. Three slave ID address select pins, AD0, AD1, and AD2, choose one of 64 slave ID addresses, including the eight addresses supported by the Phillips PCA9555. Table 1 is the register address table. Tables 2–5 show detailed register information.

Serial Interface

Serial Addressing

The MAX7318 operates as a slave that sends and receives data through a 2-wire interface. The interface uses a serial data line (SDA) and a serial clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master, typically a microcontroller, initiates all data transfers to and from the MAX7318, and generates the SCL clock that synchronizes the data transfer (Figure 2).

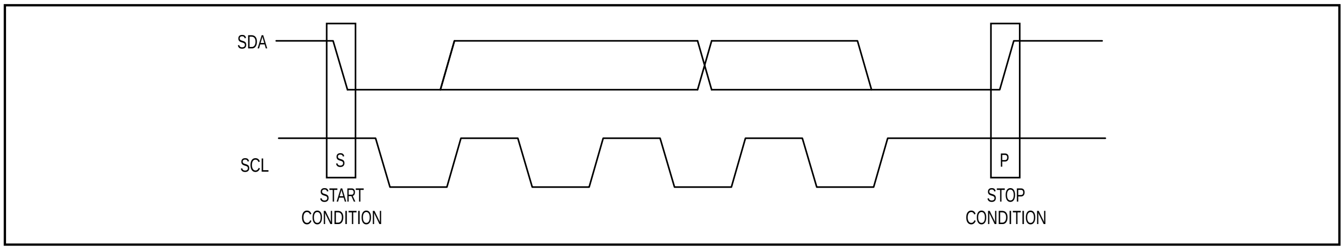


Figure 3. START and STOP Conditions

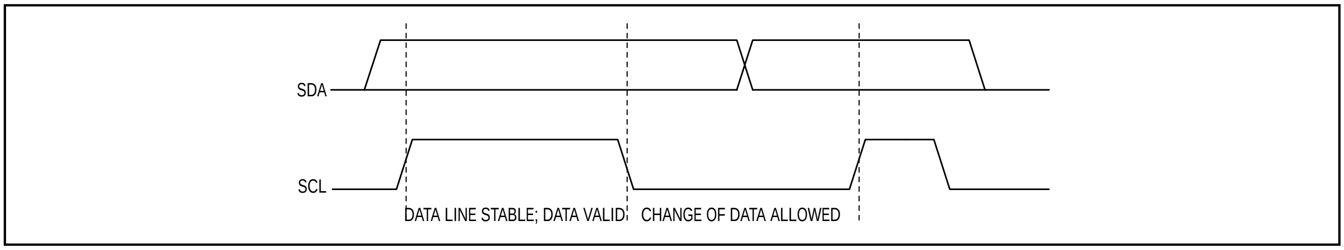


Figure 4. Bit Transfer

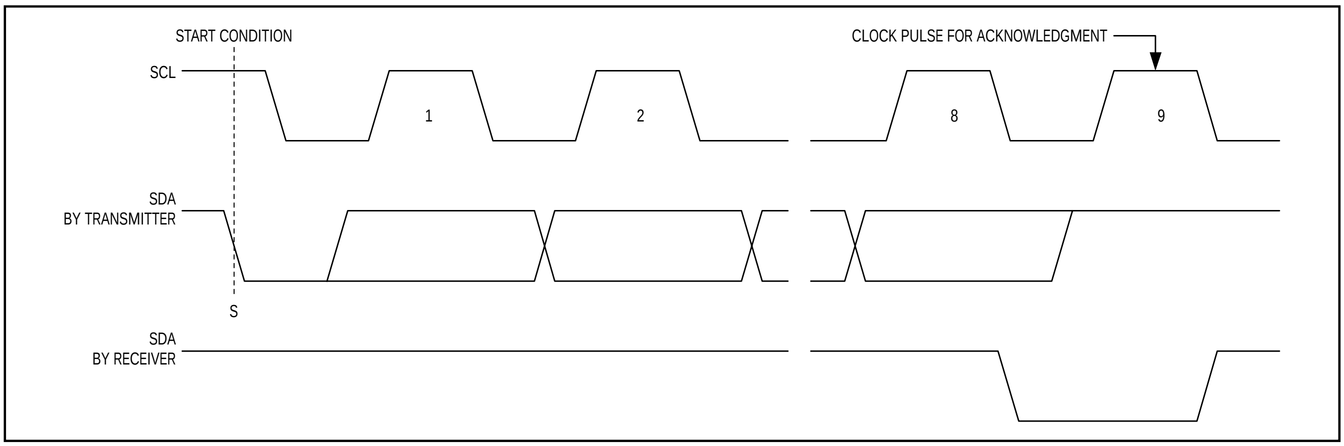


Figure 5. Acknowledge

Each transmission consists of a START condition sent by a master, followed by the MAX7318 7-bit slave address plus R/$\overline{W}$ bit, a register address byte, 1 or more data bytes, and finally a STOP condition (Figure 3).

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 3).

Bit Transfer

One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high (Figure 4).

Acknowledge

The acknowledge bit is a clocked 9th bit, which the recipient uses as a handshake receipt of each byte of data (Figure 5). Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, such that the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX7318, the MAX7318

2-Wire-Interfaced, 16-Bit, I/O Port Expander with Interrupt and Hot-Insertion Protection

generates the acknowledge bit since the MAX7318 is the recipient. When the MAX7318 is transmitting to the master, the master generates the acknowledge bit.

Slave Address

The MAX7318 has a 7-bit-long slave address (Figure 6). The 8th bit following the 7-bit slave address is the R/$\overline{W}$ bit. Set this bit low for a write command and high for a read command.

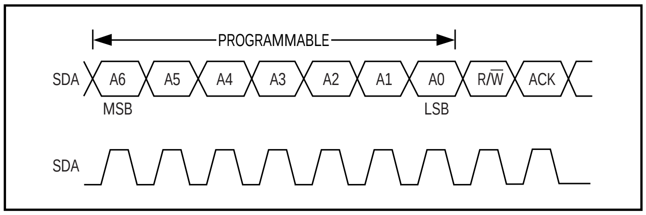


Figure 6. Slave Address

Slave address pins AD2, AD1, and AD0 choose 1 of 64 slave ID addresses (Table 7).

Data Bus Transaction

The command byte is the first byte to follow the 8-bit device slave address during a write transmission (Table 1, Figure 7). The command byte is used to determine which of the following registers are written or read.

Writing to Port Registers

Transmit data to the MAX7318 by sending the device slave address and setting the LSB to a logic zero. The command byte is sent after the address and determines which registers receive the data following the command byte (Figure 7).

Table 1. Command-Byte Register

COMMAND BYTE ADDRESS (hex)	FUNCTION	PROTOCOL	POWER-UP DEFAULT
0x00	Input port 1	Read byte	XXXX XXXX
0x01	Input port 2	Read byte	XXXX XXXX
0x02	Output port 1	Read/write byte	1111 1111
0x03	Output port 2	Read/write byte	1111 1111
0x04	Port 1 polarity inversion	Read/write byte	0000 0000
0x05	Port 2 polarity inversion	Read/write byte	0000 0000
0x06	Port 1 configuration	Read/write byte	1111 1111
0x07	Port 2 configuration	Read/write byte	1111 1111
0xFF	Factory reserved. (Do not write to this register.)	—	—

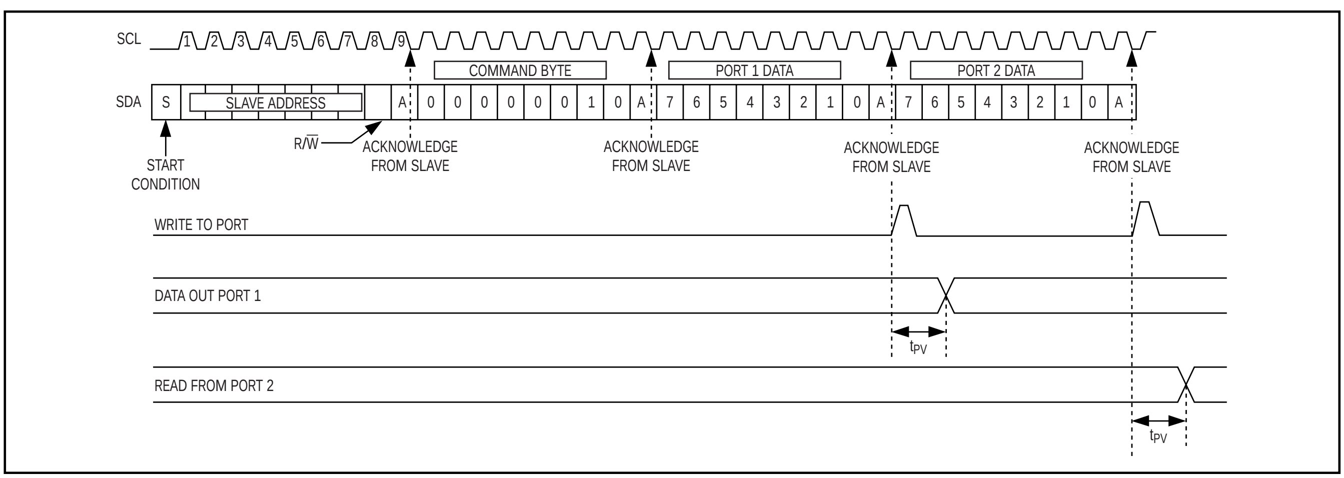


Figure 7. Writes to Output Registers Through Write-Byte Protocol

The MAX7318's eight registers are configured to operate as four register pairs: input ports, output ports, polarity inversion ports, and configuration ports. After sending 1 byte of data to one register, the next byte is sent to the other register in the pair. For example, if the first byte of data is sent to output port 2, then the next byte of data is stored in output port 1. An unlimited number of data bytes can be sent in one write transmission. This allows each 8-bit register to be updated independently of the other registers.

Reading Port Registers

To read the device data, the bus master must first send the MAX7318 address with the R/$\overline{W}$ bit set to zero, followed by the command byte, which determines which register is accessed. After a restart, the bus master must then send the MAX7318 address with the R/$\overline{W}$ bit set to 1. Data from the register defined by the command byte is then sent from the MAX7318 to the master (Figures 8, 9).

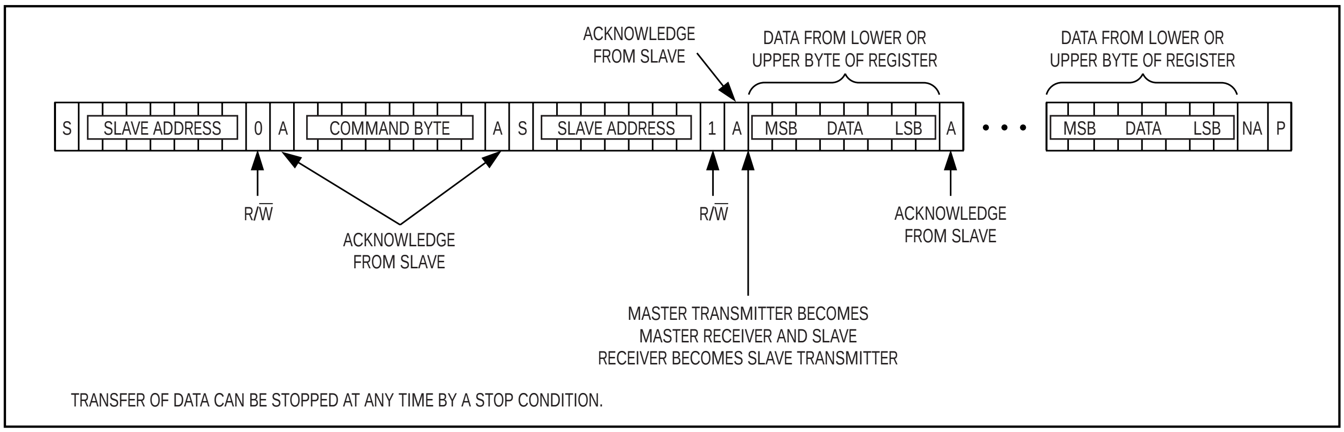


Figure 8. Read from Register

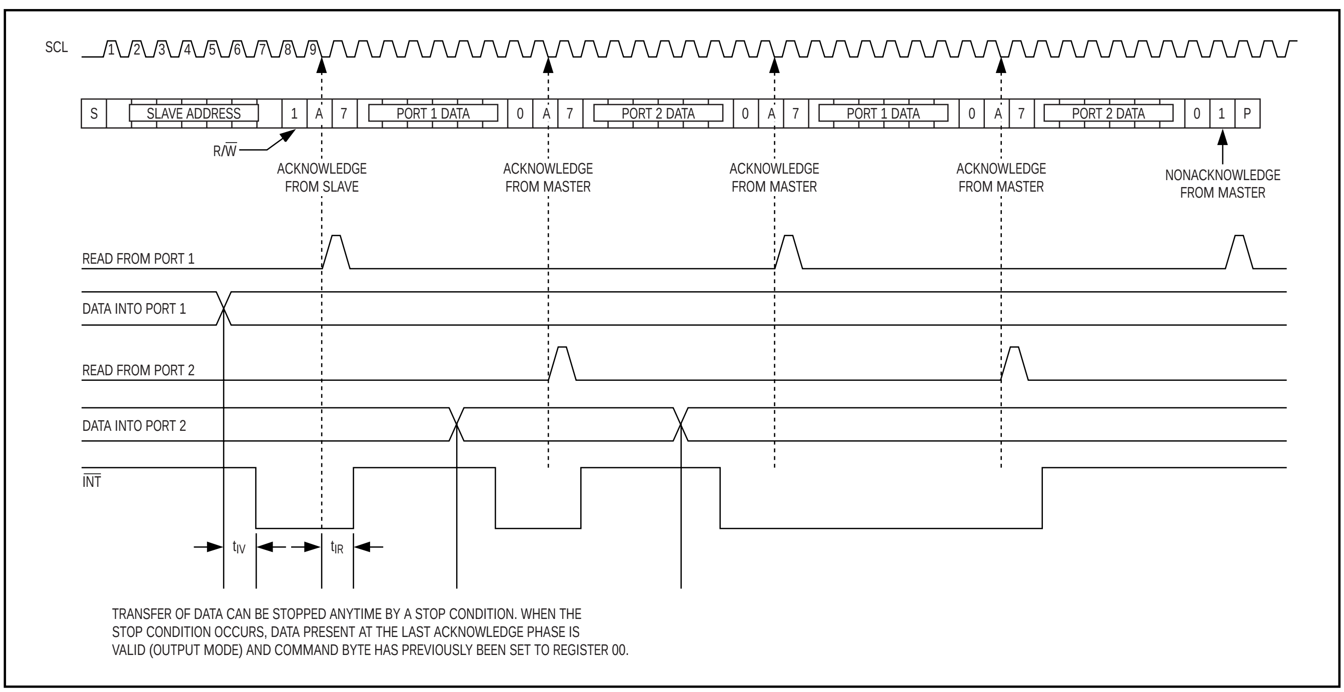


Figure 9. Read from Input Registers

2-Wire-Interfaced, 16-Bit, I/O Port Expander with Interrupt and Hot-Insertion Protection

Data is clocked into a register on the falling edge of the acknowledge clock pulse. After reading the first byte, additional bytes may be read and reflect the content in the other register in the pair. For example, if input port 1 is read, the next byte read is input port 2. An unlimited number of data bytes can be read in one read transmission, but the final byte received must not be acknowledged by the bus master.

Interrupt ($\overline{INT}$)

The open-drain interrupt output, $\overline{INT}$, activates when one of the port pins changes states and only when the pin is configured as an input. The interrupt deactivates when the input returns to its previous state or the input register is read (Figure 9). A pin configured as an output does not cause an interrupt. Each 8-bit port register is read independently; therefore, an interrupt caused by port 1 is not cleared by a read of port 2's register.

Changing an I/O from an output to an input may cause a false interrupt to occur if the state of that I/O does not match the content of the input port register.

Input/Output Port

When an I/O is configured as an input, FETs Q1 and Q2 are off (Figure 10), creating a high-impedance input with a nominal 100kΩ pullup to V+. All inputs are overvoltage protected to 5.5V, independent of supply voltage. When a port is configured as an output, either Q1 or Q2 is on, depending on the state of the output port register. When V+ powers up, an internal power-on reset sets all registers to their respective defaults (Table 1).

Input Port Registers

The input port registers (Table 2) are read-only ports. They reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the respective configuration register. A read of the input port 1 register latches the current value of I/O0–I/O7. A read of the input port 2 register latches the current value of I/O8–I/O15. Writes to the input port registers are ignored.

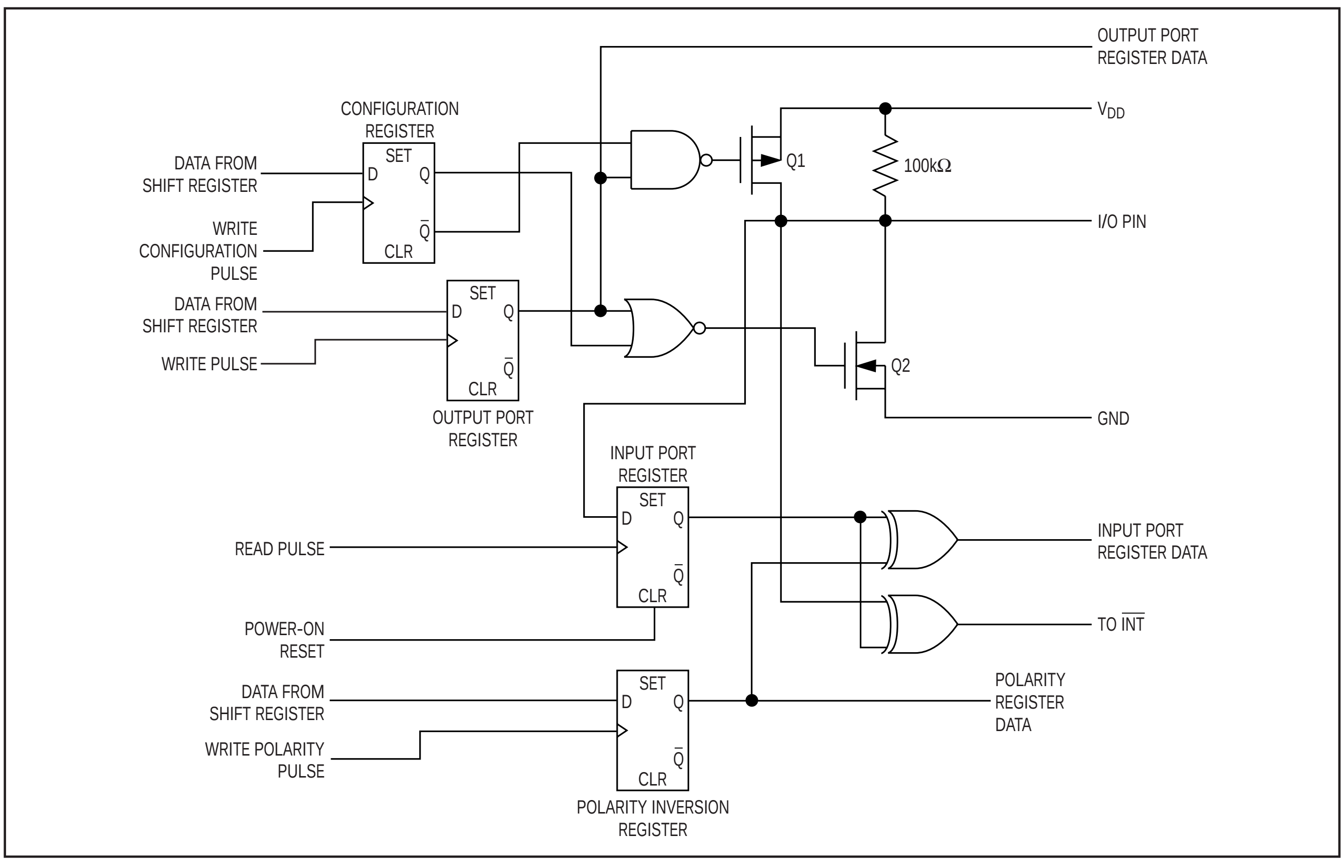


Figure 10. Simplified Schematic of I/Os

Table 2. Registers 0x00, 0x01—Input Port Registers

BIT	I7	I6	I5	I4	I3	I2	I1	I0
	I15	I14	I13	I12	I11	I10	I9	I8

Table 3. Registers 0x02, 0x03—Output Port Registers

BIT	O7	O6	O5	O4	O3	O2	O1	O0
	O15	O14	O13	O12	O11	O10	O9	O8
Power-up default	1	1	1	1	1	1	1	1

Table 4. Registers 0x04, 0x05—Polarity Inversion Registers

BIT	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
	I/O15	I/O14	I/O13	I/O12	I/O11	I/O10	I/O9	I/O8
Power-up default	0	0	0	0	0	0	0	0

Table 5. Registers 0x06, 0x07—Configuration Registers

BIT	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
	I/O15	I/O14	I/O13	I/O12	I/O11	I/O10	I/O9	I/O8
Power-up default	1	1	1	1	1	1	1	1

Output Port Registers

The output port registers (Table 3) set the outgoing logic levels of the I/Os defined as outputs by the respective configuration register. Reads from the output port registers reflect the value that is in the flip-flop controlling the output selection, not the actual I/O value.

Polarity Inversion Registers

The polarity inversion registers (Table 4) enable polarity inversion of pins defined as inputs by the respective port configuration registers. Set the bit in the polarity inversion register to invert the corresponding port pin's polarity. Clear the bit in the polarity inversion register to retain the corresponding port pin's original polarity.

Configuration Registers

The configuration registers (Table 5) configure the directions of the I/O pins. Set the bit in the respective configuration register to enable the corresponding port as an input. Clear the bit in the configuration register to enable the corresponding port as an output.

Standby

The MAX7318 goes into standby when the I^2C bus is idle. Standby supply current is typically 5.4µA.

Applications Information

Hot Insertion

The I/O ports I/O0–I/O15, interrupt output $\overline{INT}$, and serial interface SDA, SCL, AD0–2 remain high impedance with up to 6V asserted on them when the MAX7318 is powered down (V+ = 0V). The MAX7318 can therefore be used in hot-swap applications. Note that each I/O's 100kΩ pullup effectively becomes a 100kΩ pulldown when the MAX7318 is powered down.

Power-Supply Consideration

The MAX7318 operates from a supply voltage of 2V to 5.5V. Bypass the power supply to GND with a 0.047µF capacitor as close to the device as possible. For the QFN version, connect the exposed pad to GND.

Table 6. MAX7318 Address Map

AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	ADDRESS (hex)
GND	**SCL**	**GND**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0x20**
GND	SCL	V+	0	0	1	0	0	0	1	0x22
GND	SDA	GND	0	0	1	0	0	1	0	0x24
GND	SDA	V+	0	0	1	0	0	1	1	0x26
V+	SCL	GND	0	0	1	0	1	0	0	0x28
V+	SCL	V+	0	0	1	0	1	0	1	0x2A
V+	SDA	GND	0	0	1	0	1	1	0	0x2C
V+	SDA	V+	0	0	1	0	1	1	1	0x2E
GND	**SCL**	**SCL**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0x30**
GND	SCL	SDA	0	0	1	1	0	0	1	0x32
GND	SDA	SCL	0	0	1	1	0	1	0	0x34
GND	SDA	SDA	0	0	1	1	0	1	1	0x36
V+	SCL	SCL	0	0	1	1	1	0	0	0x38
V+	SCL	SDA	0	0	1	1	1	0	1	0x3A
V+	SDA	SCL	0	0	1	1	1	1	0	0x3C
V+	SDA	SDA	0	0	1	1	1	1	1	0x3E
GND	**GND**	**GND**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0x40**
GND	GND	V+	0	1	0	0	0	0	1	0x42
GND	V+	GND	0	1	0	0	0	1	0	0x44
GND	V+	V+	0	1	0	0	0	1	1	0x46
V+	GND	GND	0	1	0	0	1	0	0	0x48
V+	GND	V+	0	1	0	0	1	0	1	0x4A
V+	V+	GND	0	1	0	0	1	1	0	0x4C
V+	V+	V+	0	1	0	0	1	1	1	0x4E
GND	**GND**	**SCL**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0x50**
GND	GND	SDA	0	1	0	1	0	0	1	0x52
GND	V+	SCL	0	1	0	1	0	1	0	0x54
GND	V+	SDA	0	1	0	1	0	1	1	0x56
V+	GND	SCL	0	1	0	1	1	0	0	0x58
V+	GND	SDA	0	1	0	1	1	0	1	0x5A
V+	V+	SCL	0	1	0	1	1	1	0	0x5C
V+	V+	SDA	0	1	0	1	1	1	1	0x5E

Table 6. MAX7318 Address Map (continued)

AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	ADDRESS (hex)
SCL	**SCL**	**GND**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0xA0**
SCL	SCL	V+	1	0	1	0	0	0	1	0xA2
SCL	SDA	GND	1	0	1	0	0	1	0	0xA4
SCL	SDA	V+	1	0	1	0	0	1	1	0xA6
SDA	SCL	GND	1	0	1	0	1	0	0	0xA8
SDA	SCL	V+	1	0	1	0	1	0	1	0xAA
SDA	SDA	GND	1	0	1	0	1	1	0	0xAC
SDA	SDA	V+	1	0	1	0	1	1	1	0xAE
SCL	**SCL**	**SCL**	**1**	**0**	**1**	**1**	**0**	**0**	**0**	**0xB0**
SCL	SCL	SDA	1	0	1	1	0	0	1	0xB2
SCL	SDA	SCL	1	0	1	1	0	1	0	0xB4
SCL	SDA	SDA	1	0	1	1	0	1	1	0xB6
SDA	SCL	SCL	1	0	1	1	1	0	0	0xB8
SDA	SCL	SDA	1	0	1	1	1	0	1	0xBA
SDA	SDA	SCL	1	0	1	1	1	1	0	0xBC
SDA	SDA	SDA	1	0	1	1	1	1	1	0xBE
SCL	**GND**	**GND**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0xC0**
SCL	GND	V+	1	1	0	0	0	0	1	0xC2
SCL	V+	GND	1	1	0	0	0	1	0	0xC4
SCL	V+	V+	1	1	0	0	0	1	1	0xC6
SDA	GND	GND	1	1	0	0	1	0	0	0xC8
SDA	GND	V+	1	1	0	0	1	0	1	0xCA
SDA	V+	GND	1	1	0	0	1	1	0	0xCC
SDA	V+	V+	1	1	0	0	1	1	1	0xCE
SCL	**GND**	**SCL**	**1**	**1**	**0**	**1**	**0**	**0**	**0**	**0xD0**
SCL	GND	SDA	1	1	0	1	0	0	1	0xD2
SCL	V+	SCL	1	1	0	1	0	1	0	0xD4
SCL	V+	SDA	1	1	0	1	0	1	1	0xD6
SDA	GND	SCL	1	1	0	1	1	**0**	**0**	0xD8
SDA	GND	SDA	1	1	0	1	1	0	1	0xDA
SDA	V+	SCL	1	1	0	1	1	1	0	0xDC
SDA	V+	SDA	1	1	0	1	1	1	1	0xDE

Chip Information

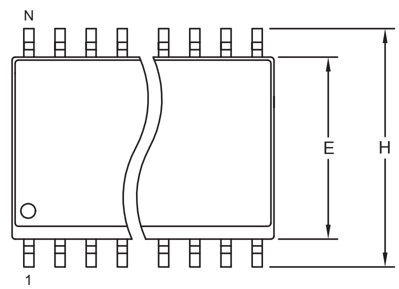
TRANSISTOR COUNT: 12,994

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOICW.EPS

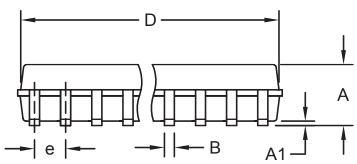


TOP VIEW

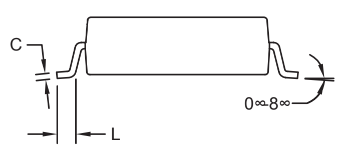
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
e	0.050		1.27	
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS013
D	0.398	0.413	10.10	10.50	16	AA
D	0.447	0.463	11.35	11.75	18	AB
D	0.496	0.512	12.60	13.00	20	AC
D	0.598	0.614	15.20	15.60	24	AD
D	0.697	0.713	17.70	18.10	28	AE



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS013.
6. N = NUMBER OF PINS.

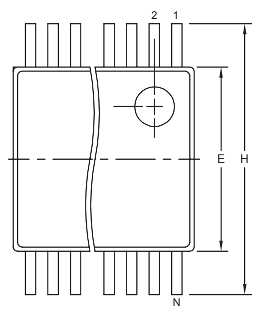
DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, .300" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0042	B	1/1

Package Information (continued)

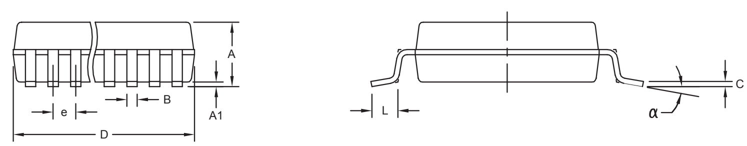
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.212	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0∞	8∞	0∞	8∞

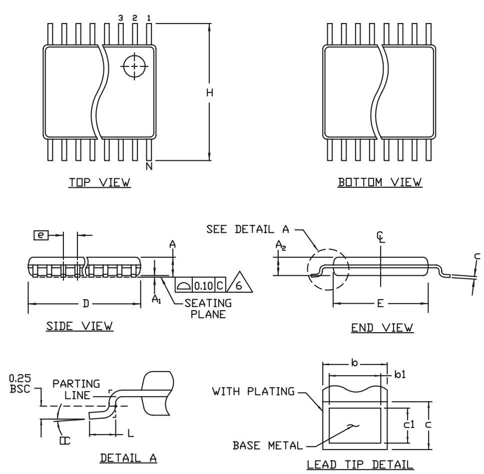
	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	N
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L



NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO150.
5. LEADS TO BE COPLANAR WITHIN 0.10 MM.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, SSOP, 5.3 MM
APPROVAL | DOCUMENT CONTROL NO. 21-0056 | REV. C | 1/1

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC MO-153	N		VARIATIONS MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

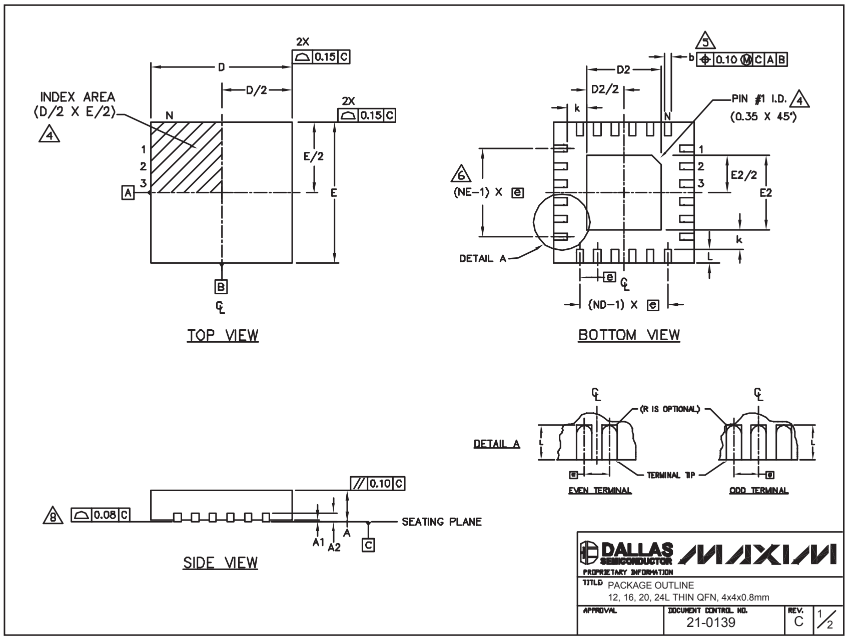
NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. 'N' REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY
APPROVAL | DOCUMENT CONTROL NO. 21-0066 | REV. F | 1/1

2-Wire-Interfaced, 16-Bit, I/O Port Expander with Interrupt and Hot-Insertion Protection

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



24L QFN THIN.EPS

COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16			20			24		
ND	3			4			5			6		
NE	3			4			5			6		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1, T2444-3 AND T2444-4.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE
12, 16, 20, 24L THIN QFN, 4x4x0.8mm
APPROVAL | DOCUMENT CONTROL NO. 21-0139 | REV. C | 2/2

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