

File Number 1563

IRFF120, IRFF121, IRFF122, IRFF123

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

5.0A and 6.0A, 60V-100V
 $r_{DS(on)} = 0.30 \Omega$ and 0.40Ω

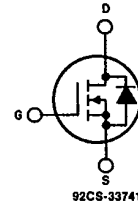
Features:

- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance
- Majority carrier device

The IRFF120, IRFF121, IRFF122 and IRFF123 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

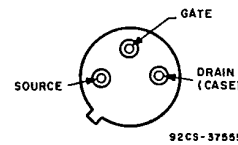
The IRFF-types are supplied in the JEDEC TO-205AF (LOW-PROFILE TO-39) metal package.

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-205AF

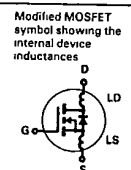
Absolute Maximum Ratings

Parameter	IRFF120	IRFF121	IRFF122	IRFF123	Units
V_{DS} Drain - Source Voltage (1)	100	60	100	60	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 20 \text{ k}\Omega$) (1)	100	60	100	60	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM} Pulsed Drain Current (2)	24	24	20	20	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	20 (See Fig. 14)				W
Linear Derating Factor	0.16 (See Fig. 14)				W/ $^\circ\text{C}$
I_{LM} Inductive Current, Clamped	24	24	20	20	A
T_J Operating Junction and Storage Temperature Range	-55 to 150				$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

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Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter	Type	Min	Typ	Max	Units	Test Conditions
BV _{DSS} Drain - Source Breakdown Voltage	IRFF120	100	—	—	V	V _{GS} = 0V I _D = 250μA
	IRFF122	—	—	—	—	
	IRFF121 IRFF123	60	—	—	V	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	V _{GS} = 20V
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V _{GS} = -20V
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C
I _{D(on)} On-State Drain Current ②	IRFF120	6.0	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V
	IRFF122	5.0	—	—	A	
	IRFF121 IRFF123	—	—	—	—	
R _{DS(on)} Static Drain-Source On-State Resistance ②	IRFF120	—	0.25	0.30	Ω	V _{GS} = 10V, I _D = 3.0A
	IRFF122	—	—	—	—	
	IRFF121 IRFF123	—	0.30	0.40	Ω	
B _f Forward Transconductance ②	ALL	1.5	2.9	—	S (Ω)	V _{DS} > I _{D(on)} × R _{DS(on)} max., I _D = 3.0A
C _{iss} Input Capacitance	ALL	—	450	600	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz
C _{oss} Output Capacitance	ALL	—	200	400	pF	See Fig. 10
C _{rss} Reverse Transfer Capacitance	ALL	—	50	100	pF	See Fig. 10
t _{d(on)} Turn-On Delay Time	ALL	—	20	40	ns	V _{DD} = 0.5 BV _{DSS} , I _D = 3.0A, Z _θ = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t _r Rise Time	ALL	—	37	70	ns	
t _{d(off)} Turn-Off Delay Time	ALL	—	50	100	ns	
t _f Fall Time	ALL	—	35	70	ns	
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	10	15	nC	V _{GS} = 10V, I _D = 10A, V _{DS} = 0.8 Max. Rating See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q _{gs} Gate-Source Charge	ALL	—	6.0	—	nC	
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	4.0	—	nC	
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die
L _S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad



Thermal Resistance

R _{thJC} Junction-to-Case	ALL	—	—	6.25	°C/W	
R _{thJA} Junction-to-Ambient	ALL	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I _S Continuous Source Current (Body Diode)	IRFF120	—	—	6.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier
	IRFF122	—	—	5.0	A	
	IRFF121 IRFF123	—	—	2.0	A	
I _{SM} Pulse Source Current (Body Diode) ③	IRFF120	—	—	24	A	
	IRFF122	—	—	20	A	
	IRFF121 IRFF123	—	—	—	—	
V _{SD} Diode Forward Voltage ②	IRFF120 IRFF121	—	—	2.5	V	T _C = 25°C, I _S = 6.0A, V _{GS} = 0V
	IRFF122 IRFF123	—	—	2.3	V	T _C = 25°C, I _S = 5.0A, V _{GS} = 0V
t _{rr} Reverse Recovery Time	ALL	—	230	—	ns	T _J = 150°C, I _F = 6.0A, dI _F /dt = 100A/μs
Q _{RR} Reverse Recovered Charge	ALL	—	1.2	—	μC	T _J = 150°C, I _F = 6.0A, dI _F /dt = 100A/μs
t _{on} Forward Turn on Time	ALL	Intrinsic turn on time is negligible. Turn on speed is substantially controlled by L _S + L _D				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width < 300μs. Duty Cycle < 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

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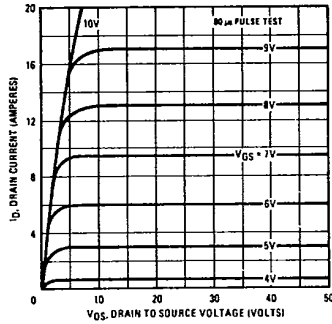


Fig. 1 - Typical Output Characteristics

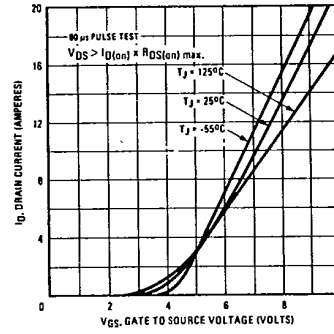


Fig. 2 - Typical Transfer Characteristics

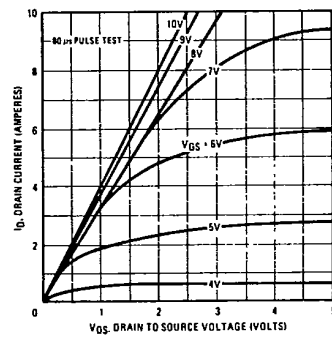


Fig. 3 - Typical Saturation Characteristics

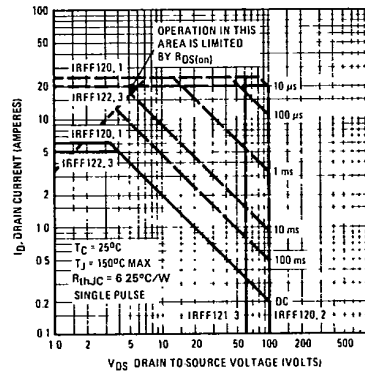


Fig. 4 - Maximum Safe Operating Area

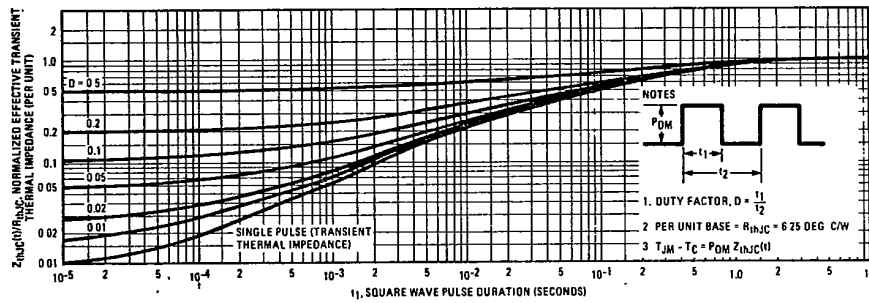


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

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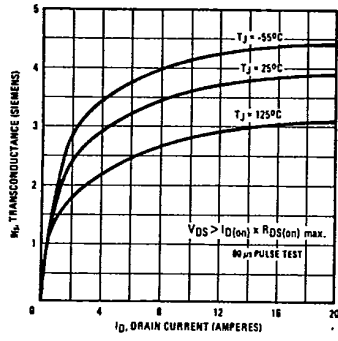


Fig. 6 - Typical Transconductance Vs. Drain Current

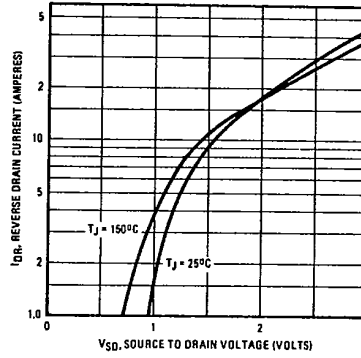


Fig. 7 - Typical Source-Drain Diode Forward Voltage

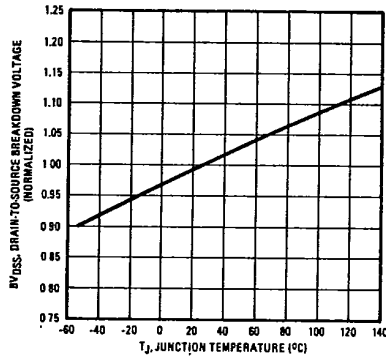


Fig. 8 - Breakdown Voltage Vs. Temperature

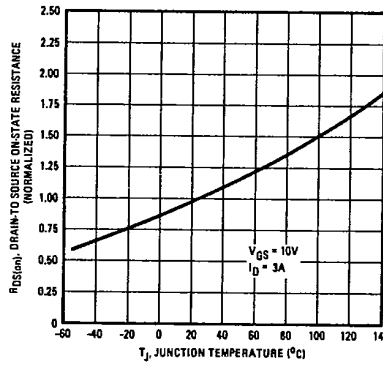


Fig. 9 - Normalized On-Resistance Vs. Temperature

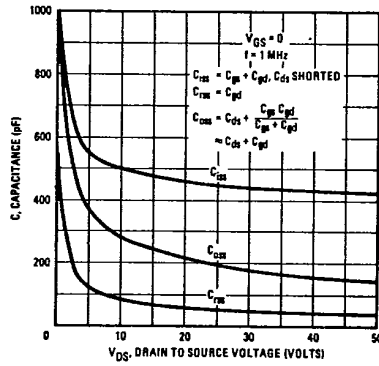


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

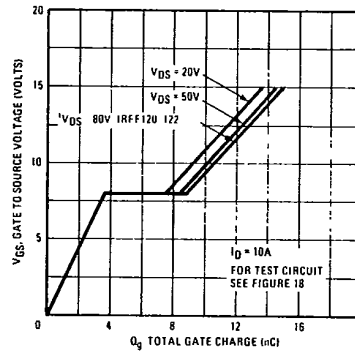


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

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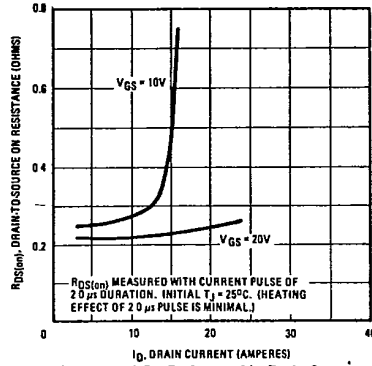


Fig. 12 - Typical On-Resistance Vs. Drain Current

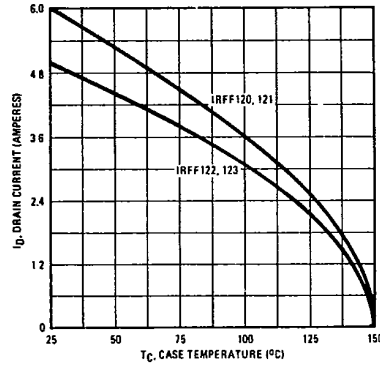


Fig. 13 - Maximum Drain Current Vs. Case Temperature

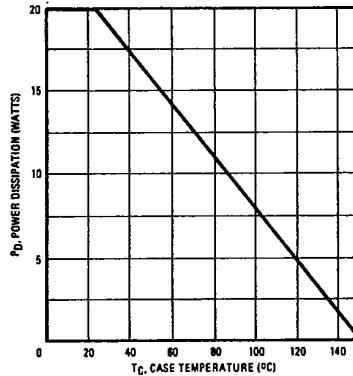


Fig. 14 - Power Vs. Temperature Derating Curve

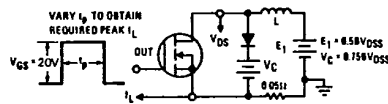


Fig. 15 - Clamped Inductive Test Circuit



Fig. 16 - Clamped Inductive Waveforms

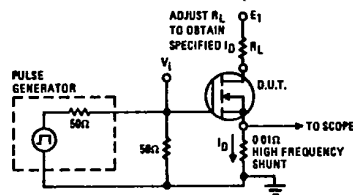


Fig. 17 - Switching Time Test Circuit

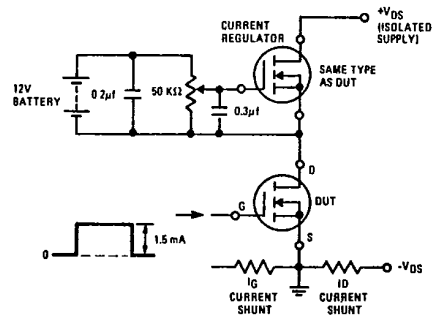


Fig. 18 - Gate Charge Test Circuit