Integrated Device Technology, Inc.

128K X 8 CMOS STATIC RAM MODULE

IDT8M824S

FEATURES:

- High-density 1 megabit (128K x 8)CMOS static RAM module
- High-speed
  - — Military: 35ns (max.)
  - — Commercial: 25ns (max.)
- Low power consumption
  - — Active: less than 550mW (typ.)
  - — Standby: less than 20mW (typ.)
- Offered in the JEDEC standard 32-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

The IDT8M824S is a 128K x 8 high-speed CMOS static RAM constructed on a co-fired ceramic substrate using four 32K x 8 static RAMs and a FCT139 decoder in leadless chip carriers. Functional equivalence to monolithic one megabit static RAMs is achieved by utilization of an on board decoder that interprets the higher order address A_{15} and A_{16} to select one of the four 32K x 8 RAMs. Extremely fast speeds can be achieved with this technique due to use of 256K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability CEMOS technology.

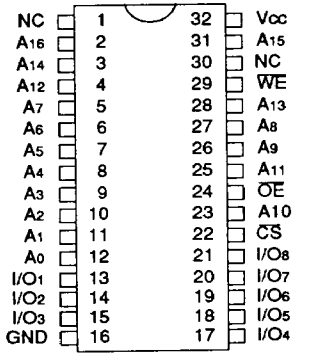
The IDT8M824S is available with maximum access times as fast as 25ns for commercial temperature range, with maximum power consumption of 2.5 watts. The module offers a full standby mode of 440mW (max.).

The IDT8M824S is offered in a 32-pin, 600 mil center sidebraze DIP, adhering to JEDEC standards for one megabit monolithic pinouts.

All inputs and outputs of the IDT8M824S are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

All IDT military module semiconductor components are manufactured in compliance to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION (1)



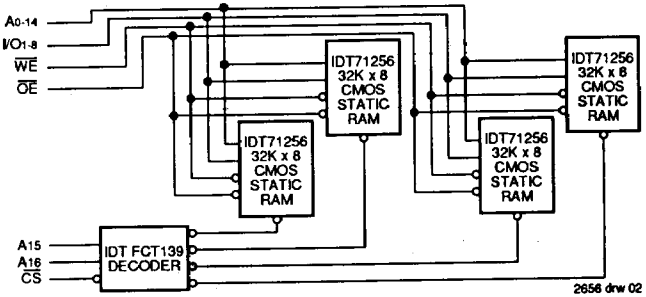
DIP
TOP VIEW

2656 drw 01

2656 drw 01

NOTE:
1. For module dimensions, please refer to module drawing M6 and M7 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



2656 drw 02

PIN NAMES

A_{0-16}	Addresses
I/O_{1-8}	Data Input/Output
$\overline{CS}$	Chip Select
Vcc	Power
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground

2656 tbl 01

8

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2656 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2656 tbl 03

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2656 tbl 04

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to + 125°C and 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	IDT8M824S Typ.(1)	IDT8M824S Max.(2)	IDT8M824S Max.(3)	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	—	20	40	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	—	20	40	uA
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ = V_{IL}, f = f_{MAX}, Output Open	—	150	450	265	mA
I_{SB}	Standby Supply Current	V_{CC} = MAX. $\overline{CS}$ = V_{IH} f = fmax, Outputs open	—	10	280	85	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} -0.2V V_{IN} > V_{CC} -0.2V or < 0.2V	—	10	80	80	mA
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 8mA	—	—	0.4	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min. I_{OH} = -4mA	2.4	—	—	—	V

2656 tbl 05

NOTES:
1. V_{CC} = 5V, T_A = +25°C.
2. tAA = 25ns.
3. tAA = 30, 35, 40, 45, 50, 60, 70, 85, 100ns.

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2656 tbl 06

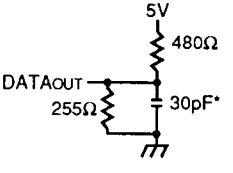
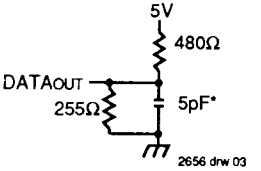


Figure 1. Output Load



2656 drw 03

Figure 2. Output Load
(for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(VCC = 5V ± 10%, TA = -55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	8M824S25 (Com'l. Only) Min.	Max.	8M824S30 (Com'l. Only) Min.	Max.	8M824S35 Min.	Max.	8M824S40 Min.	Max.	8M824S45 Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
tAA	Address Access Time	—	25	—	30	—	35	—	40	—	45	ns
tACS	Chip Select Access Time	—	25	—	30	—	35	—	40	—	45	ns
tCLZ1,2[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	10	—	11	—	13	—	25	—	25	ns
tOLZ[1]	Output Enable to Output in Low Z	2	—	2	—	2	—	5	—	5	—	ns
tCHZ[1]	Chip Select to Output in High Z	—	15	—	16	—	20	—	20	—	20	ns
tOHZ[1]	Output Disable to Output in High Z	—	8	—	10	—	15	—	20	—	20	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
tPU[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD[1]	Chip Deselect to Power-Down Time	—	25	—	30	—	35	—	40	—	45	ns
Write Cycle												
tWC	Write Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
tCW	Chip Select to End of Write	20	—	25	—	30	—	35	—	40	—	ns
tAW	Address Valid to End of Write	20	—	25	—	30	—	35	—	40	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	5	—	5	—	ns
tWP	Write Pulse Width	15	—	20	—	23	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	2	—	5	—	5	—	ns
tWHZ[1]	Write Enable to Output in High Z	—	10	—	11	—	15	—	15	—	15	ns
tDW	Data to Write Time Overlap	11	—	13	—	14	—	15	—	20	—	ns
tDH	Data Hold from Write Time	3	—	3	—	3	—	3	—	5	—	ns
tOW[1]	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

2656 tbl 07

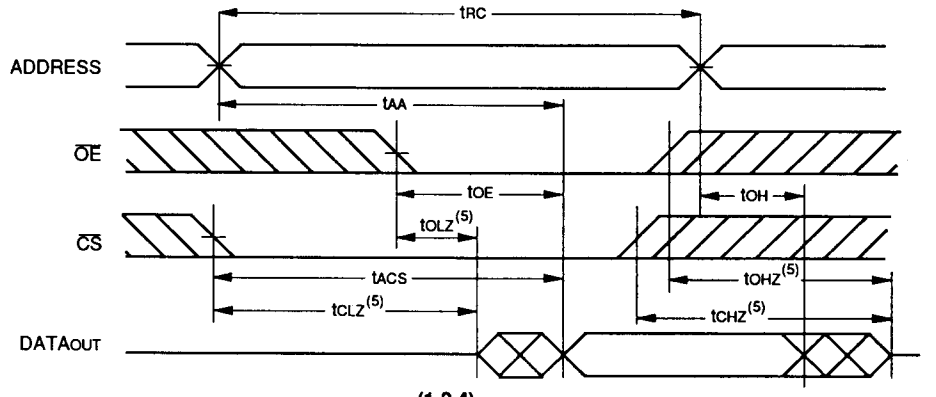
Symbol	Parameter	8M824S50 Min.	Max.	8M824S60 (Mil. Only) Min.	Max.	8M824S70 (Mil. Only) Min.	Max.	8M824S85 (Mil. Only) Min.	Max.	8M824S100 (Mil. Only) Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	50	—	60	—	70	—	85	—	100	—	ns
tAA	Address Access Time	—	50	—	60	—	70	—	85	—	100	ns
tACS	Chip Select Access Time	—	50	—	60	—	70	—	85	—	100	ns
tCLZ1,2[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	30	—	35	—	40	—	50	—	60	ns
tOLZ[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tCHZ[1]	Chip Select to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
tOHZ[1]	Output Disable to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
tPU[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD[1]	Chip Deselect to Power-Down Time	—	50	—	60	—	70	—	85	—	100	ns
Write Cycle												
tWC	Write Cycle Time	50	—	60	—	70	—	85	—	100	—	ns
tCW	Chip Select to End of Write	45	—	55	—	65	—	75	—	90	—	ns
tAW	Address Valid to End of Write	45	—	55	—	65	—	75	—	90	—	ns
tAS	Address Set-up Time	5	—	5	—	5	—	5	—	5	—	ns
tWP	Write Pulse Width	40	—	50	—	60	—	70	—	80	—	ns
tWR	Write Recovery Time	5	—	5	—	5	—	10	—	10	—	ns
tWHZ[1]	Write Enable to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
tDW	Data to Write Time Overlap	20	—	25	—	30	—	35	—	40	—	ns
tDH	Data Hold from Write Time	5	—	5	—	5	—	5	—	5	—	ns
tOW[1]	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

2656 tbl 08

NOTE:
1. This parameter guaranteed by design but not tested.

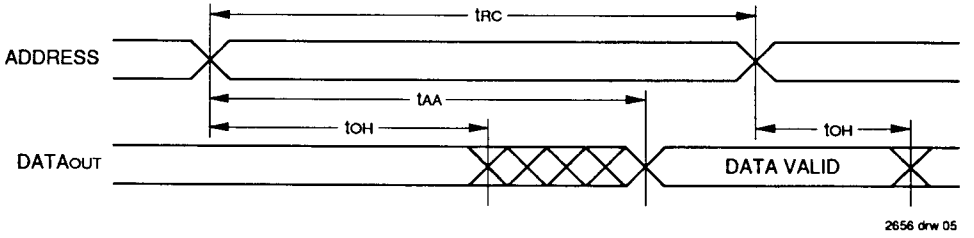
8

TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



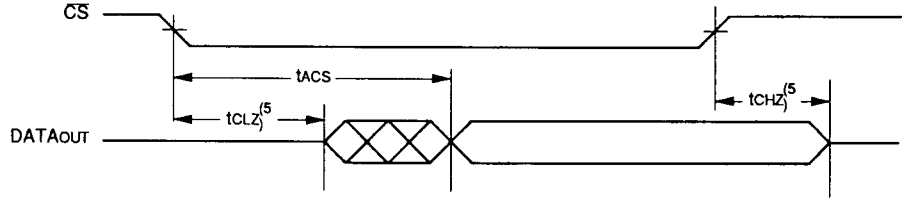
TIMING WAVEFORM OF READ CYCLE NO. 2 (1,2,4)

2656 drw 04



2656 drw 05

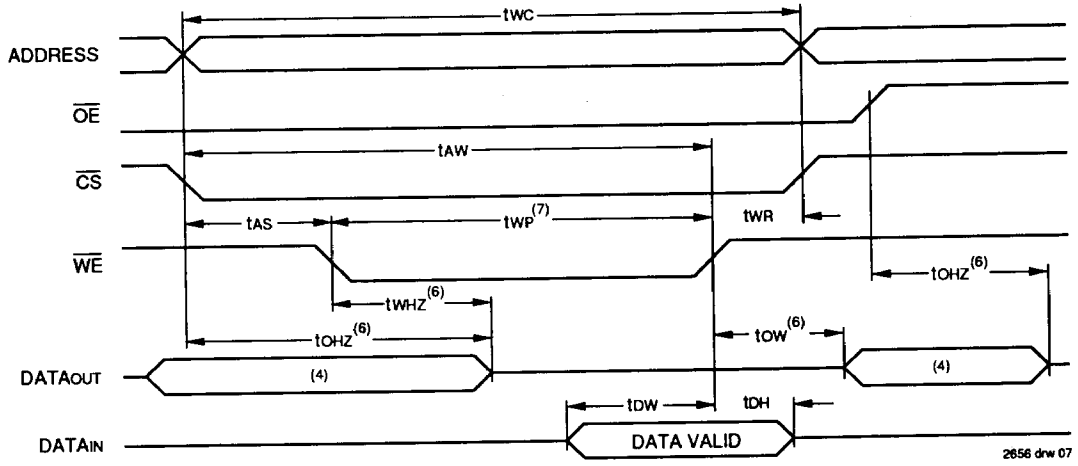
TIMING WAVEFORM OF READ CYCLE NO. 3 (1,3,4)



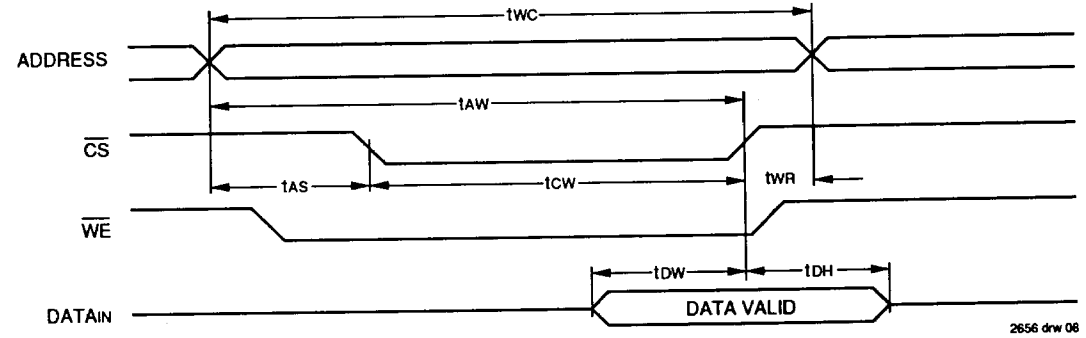
2656 drw 06

NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,3,7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,3,5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (tWP > tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

8

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High Z	Active
Write	L	X	L	DIN	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
$C_{IN(D)}$	Input Capacitance (data)	V_{IN} = 0V	35	50	pF
$C_{IN(AC1)}$	Input Capacitance (A_{0-14}, $\overline{OE}$, $\overline{WE}$)	V_{IN} = 0V	35	50	pF
$C_{IN(AC2)}$	Input Capacitance (A_{15-16}, $\overline{CS}$)	V_{OUT} = 0V	—	14	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	35	50	pF

NOTE:
1. This parameter is guaranteed by design but not tested.

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Semiconductor Components Compliant to MIL-STD-883, Class B
C	LCCs on a Sidebraze DIP (Dual In-line Package)
N	SOICs on a Sidebraze DIP (Dual In-line Package)
25	(Commercial Only) — Speed in Nanoseconds
30	(Commercial Only) — Speed in Nanoseconds
35	Speed in Nanoseconds
40	Speed in Nanoseconds
45	Speed in Nanoseconds
50	Speed in Nanoseconds
60	(Military Only) — Speed in Nanoseconds
70	(Military Only) — Speed in Nanoseconds
85	(Military Only) — Speed in Nanoseconds
100	(Military Only) — Speed in Nanoseconds
S	Standard Power
8M824	128K x 8 CMOS Static RAM Module

2656 Drw 09