

150-mA Ultra Low-Noise LDO Regulator With Error Flag and Discharge Option

FEATURES

- Ultra Low Dropout—130 mV at 150-mA Load
- Ultra Low Noise—30 $\mu\text{V}_{(\text{rms})}$ (10-Hz to 100-kHz Bandwidth)
- Out-of-Regulation Error Flag (power good)
- Shutdown Control
- Only 110- μA Ground Current at 150-mA Load
- Fast Start-Up (50 μs)
- 1.5% Guaranteed Output Voltage Accuracy
- 300-mA Peak Output Current Capability
- Uses Low ESR Ceramic Capacitors
- Fast Line and Load Transient Response ($\leq 30 \mu\text{s}$)
- 1- μA Maximum Shutdown Current
- Output Current Limit

- Si91845: Output, Auto-Discharge in Shutdown Mode
- Si91846: Output, No-Discharge in Shutdown Mode
- Fixed 1.8, 2.0, 2.2, 2.5, 2.6, 2.7, 2.8, 2.85, 2.9, 3.0, 3.3, 3.5, 3.6, 5.0-V Output Voltage Options
- Built-in Short Circuit and Thermal Protection
- Reverse Battery Protection
- Thin SOT23-6 Package

APPLICATIONS

- Cellular Phones, Wireless Handsets
- Noise-Sensitive Electronic Systems, Laptop and Palmtop Computers
- PDAs
- Digital Cameras
- Pagers
- MP3 Players
- Wireless Modems

DESCRIPTION

The Si91845/6 is a 150-mA CMOS LDO (low dropout) voltage regulator. It is the perfect choice for low voltage, low power applications. An ultra low ground current and ultra fast turn-on make this part attractive for battery operated power systems. The Si91845/6 also offers ultra low dropout voltage to prolong battery life in portable electronics. Systems requiring a quiet voltage source will benefit from the Si91845/6's low output noise. The Si91845/6 is designed to maintain regulation while delivering 300-mA peak current, making it ideal for systems that have a high surge current upon turn-on.

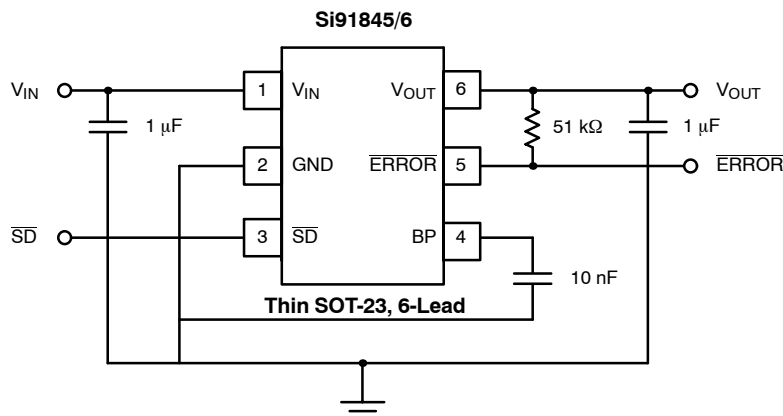
pull-down circuit is built into the Si91845/6 to clamp the output voltage when it rises beyond normal regulation. The Si91845 automatically discharges the output voltage by connecting the output to ground through a 100- Ω n-channel MOSFET when the device is put in shutdown mode.

The Si91845/6 features reverse battery protection to limit reverse current flow to approximately 1- μA in the event reversed battery is applied at the input, thus preventing damage to the IC.

For better transient response and regulation, an active

The Si91845/6 is available in both standard and lead (Pb)-free packages.

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings	
Input Voltage, V_{IN} to GND	-6.0 to 6.5 V
ERROR, V_{SD} (See Detailed Description)	-0.3 V to V_{IN}
Output Current, I_{OUT}	Short Circuit Protected
Output Voltage, V_{OUT}	-0.3 V to $V_{IN} + 0.3$ V
Package Power Dissipation, $(P_d)^b$	440 mW

Package Thermal Resistance, $(\theta_{JA})^a$	180°C/W
Maximum Junction Temperature, $T_{J(max)}$	150°C
Storage Temperature, T_{STG}	-65°C to 150°C

Notes

- Device mounted with all leads soldered or welded to PC board.
- Derate 5.5 mW/°C above $T_A = 70^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Input Voltage, V_{IN}	2 V to 6 V	Operating Ambient Temperature, T_A	-40°C to 85°C
Input Voltage, V_{SD}	0 V to V_{IN}		
$C_{IN} = C_{OUT} = 1 \mu\text{F}$ (ceramic)			
Maximum ESR of C_{OUT} : 0.4 Ω			

SPECIFICATIONS							
Parameter	Symbol	Test Conditions Unless Specified $T_A = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 1$ V, $I_{OUT} = 1$ mA, $C_{IN} = 1 \mu\text{F}$, $C_{OUT} = 1.0 \mu\text{F}$, $V_{SD} = 1.5$ V	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Input Voltage Range	V_{IN}		Full	2		6	V
Output Voltage Accuracy		$1 \text{ mA} \leq I_{OUT} \leq 150 \text{ mA}$	Room	-1.5	1	1.5	%
			Full	-2.5	1	2.5	
Line Regulation ($V_{OUT} \leq 3$ V)	$\frac{\Delta V_{OUT} \times 100}{\Delta V_{IN} \times V_{OUT(nom)}}$	From $V_{IN} = V_{OUT(nom)} + 1$ V to $V_{OUT(nom)} + 2$ V	Full	-0.06		0.18	%V
Line Regulation (3.0 V < $V_{OUT} \leq 3.6$ V)			Full	0		0.3	
Line Regulation (5-V Version)			Full	0		0.4	
Dropout Voltage ^{d, g} ($V_{OUT(nom)} \geq 2.6$ V)	$V_{IN} - V_{OUT}$	$I_{OUT} = 1$ mA	Room		1		mV
			Room		45	80	
				Full		50	
			Full		130	180	
	220						
Dropout Voltage ^{d, g} ($V_{OUT(nom)} < 2.6$ V, $V_{IN} \geq 2$ V)	$V_{IN} - V_{OUT}$	$I_{OUT} = 50$ mA	Room		65	100	mV
			Full			120	
		Room		190	250		
			Full		300		
Ground Pin Current ^{e, g} ($V_{OUT(nom)} \leq 3$ V)	I_{GND}	$I_{OUT} = 0$ mA	Room		100	150	μA
			Full			180	
		Room		110	200		
			Full		230		
Ground Pin Current ^{e, g} ($V_{OUT(nom)} > 3$ V)	I_{GND}	$I_{OUT} = 0$ mA	Room		110	170	μA
			Full			200	
		Room		120	200		
			Full		230		
Peak Output current	$I_{O(peak)}$	$V_{OUT} \geq 0.95 \times V_{OUT(nom)}$, $t_{PW} = 2$ ms	Full	300			mA
Output Noise Voltage	e_N	$V_{NOM} = 2.6$ V, BW = 10 Hz to 100 kHz, $0 \text{ mA} < I_{OUT} < 150 \text{ mA}$	Room		30		$\mu\text{V(rms)}$
Ripple Rejection	$\Delta V_{OUT}/\Delta V_{IN}$	$I_{OUT} = 150$ mA	f = 1 kHz	Room		60	dB
			f = 10 kHz	Room		40	
			f = 100 kHz	Room		30	



SPECIFICATIONS							
Parameter	Symbol	Test Conditions Unless Specified $T_A = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT} = 1.0\ \mu\text{F}$, $V_{SD} = 1.5\text{ V}$	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Dynamic Line Regulation	$\Delta V_{O(\text{line})}$	$V_{IN} : V_{OUT(nom)} + 1\text{ V to } V_{OUT(nom)} + 2\text{ V}$ $t_r/t_f = 2\ \mu\text{s}$, $I_{OUT} = 150\text{ mA}$	Room		20		mV
Dynamic Load Regulation	$\Delta V_{O(\text{load})}$	$I_{OUT} : 1\text{ mA to } 150\text{ mA}$, $t_r/t_f = 2\ \mu\text{s}$	Room		25		
Thermal Shutdown Junction Temperature	$T_{J(S/D)}$		Room		150		°C
Thermal Hysteresis	T_{HYST}		Room		20		
Reverse current	I_R	$V_{IN} = -6.0\text{ V}$	Room		1		μA
Short Circuit Current	I_{SC}	$V_{OUT} = 0\text{ V}$	Room		700		mA
Shutdown							
Shutdown Supply Current	$I_{CC(\text{off})}$	$V_{SD} = 0\text{ V}$	Room		0.1	1	μA
SD Pin Input Voltage	V_{SD}	High = Regulator ON (Rising)	Full	1.5		V_{IN}	V
		Low = Regulator OFF (Falling)	Full			0.4	
Auto Discharge Resistance	R_{DIS}	Si91845 Only	Room		100		Ω
SD Pin Input Current ^f	$I_{IN(SD)}$	$V_{SD} = 1.5\text{ V}$, $V_{IN} = 6\text{ V}$	Room		0.7		μA
SD Hysteresis	$V_{HYST(SD)}$		Full		150		mV
V_{OUT} Turn-On Time	t_{ON}	V_{SD} (See Figure 1), $I_{LOAD} = 100\text{ mA}$	Room		50		μS
ERROR Output							
ERROR High Leakage	I_{OFF}	$\overline{\text{ERROR}} \leq V_{IN}$, V_{OUT} in Regulation	Full			1	μA
ERROR Low Voltage	V_{OL}	$I_{SINK} = 0.5\text{ mA}$	Full			0.4	V
ERROR Voltage Threshold	V_{ERROR}	V_{OUT} Below $V_{OUT(nom)}^g$ V_{OUT} Falling, $I_{OUT} = 1\text{ mA}$, $V_{OUT(nom)} > 2\text{ V}$	Full	-2	-4	-6	%
ERROR Voltage Threshold Hysteresis	$V_{HYST(\text{ERROR})}$	$V_{OUT} > 2\text{ V}$	Room		1.5		
ERROR Voltage Threshold	V_{ERROR}	V_{OUT} Below $V_{OUT(nom)}^g$ V_{OUT} Falling, $I_{OUT} = 1\text{ mA}$, $V_{OUT(nom)} < 2\text{ V}$	Room		-10		
ERROR Voltage Threshold Hysteresis	$V_{HYST(\text{ERROR})}$	$V_{OUT} < 2\text{ V}$	Room		4		

Notes

- a. Room = 25°C, Full = -40 to 85°C.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. Dropout voltage is defined as the input to output differential voltage at which the output voltage drops 2% below the output voltage measured with a 1-V differential, provided that V_{IN} does not drop below 2.0 V.
- e. Ground current is specified for normal operation as well as “drop-out” operation.
- f. The device’s shutdown pin includes a typical 2-MΩ internal pull-down resistor connected to ground.
- g. $V_{OUT(nom)}$ is V_{OUT} when measured with a 1-V differential to V_{IN} .

TIMING WAVEFORMS

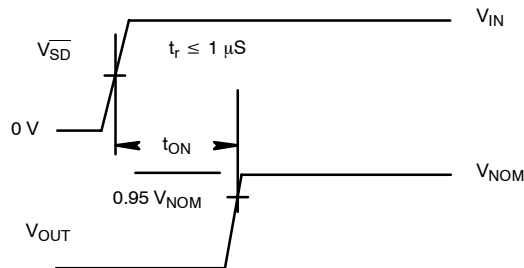
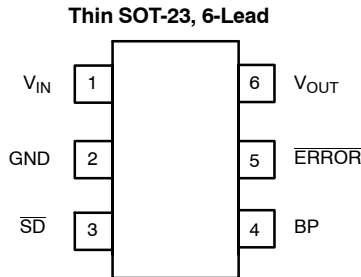


FIGURE 1. Timing Diagram for Power-Up

PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Name	Function
1	V _{IN}	Input supply pin. Bypass this pin with a 1- μ F ceramic or tantalum capacitor to ground
2	GND	Ground pin. For better thermal capability, directly connected to large ground plane
3	SD	By applying less than 0.4 V to this pin, the device will be turned off. Connect this pin to V _{IN} if unused
4	BP	Noise bypass pin. For low noise applications, a 0.01 μ F ceramic capacitor should be connected from this pin to ground.
5	ERROR	The open drain output is an error flag output which goes low when V _{OUT} drops 4% below its nominal voltage.
6	V _{OUT}	Output voltage. Connect C _{OUT} between this pin and ground.

ORDERING INFORMATION—Si91845

Part Number	Lead (Pb)-Free Part Number	Marking	Voltage	Temperature Range	Package
Si91845DT-18-T1	Si91845DT-18-T1—E3	G0LL	1.8	-40 to 85°C	Thin SOT23-6
Si91845DT-20-T1	Si91845DT-20-T1—E3	H1LL	2.0		
Si91845DT-22-T1	Si91845DT-22-T1—E3	H2LL	2.2		
Si91845DT-25-T1	Si91845DT-25-T1—E3	H3LL	2.5		
Si91845DT-26-T1	Si91845DT-26-T1—E3	H4LL	2.6		
Si91845DT-27-T1	Si91845DT-27-T1—E3	H5LL	2.7		
Si91845DT-28-T1	Si91845DT-28-T1—E3	H6LL	2.8		
Si91845DT-285-T1	Si91845DT-285—E3	H7LL	2.85		
Si91845DT-29-T1	Si91845DT-29-T1—E3	H8LL	2.9		
Si91845DT-30-T1	Si91845DT-30-T1—E3	H9LL	3.0		
Si91845DT-33-T1	Si91845DT-33-T1—E3	H0LL	3.3		
Si91845DT-35-T1	Si91845DT-35-T1—E3	I1LL	3.5		
Si91845DT-36-T1	Si91845DT-36-T1—E3	I2LL	3.6		
Si91845DT-50-T1	Si91845DT-50-T1—E3	I3LL	5.0		

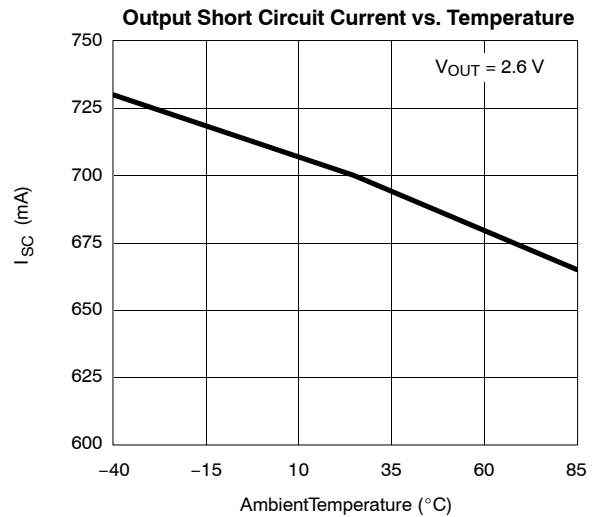
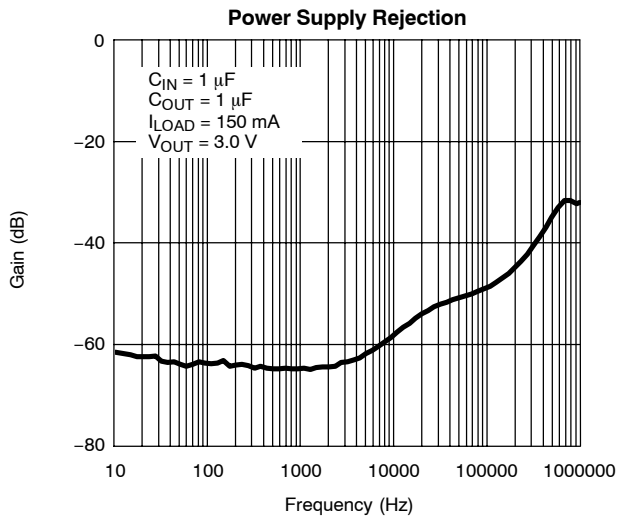
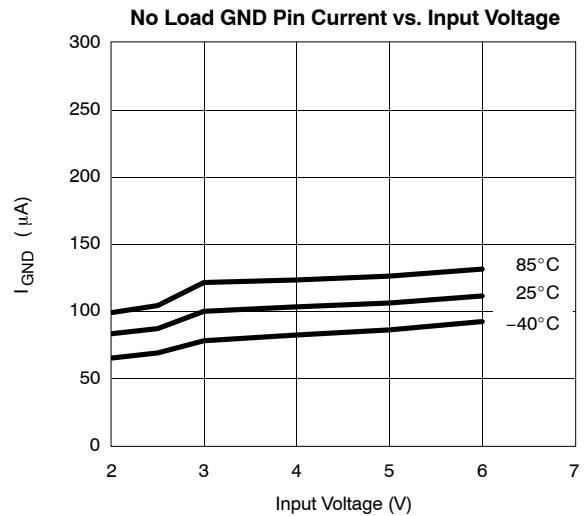
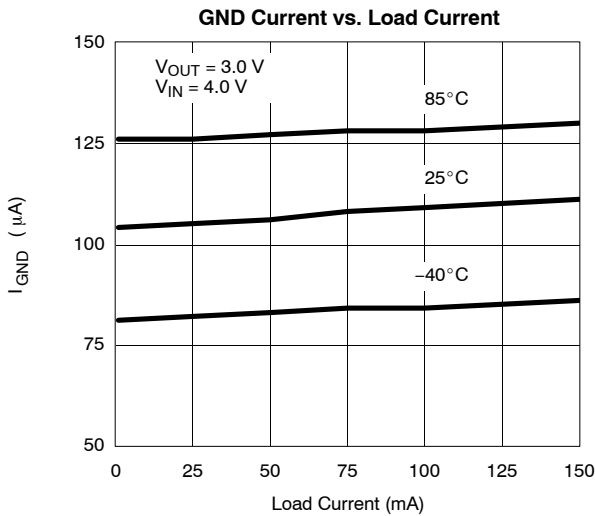
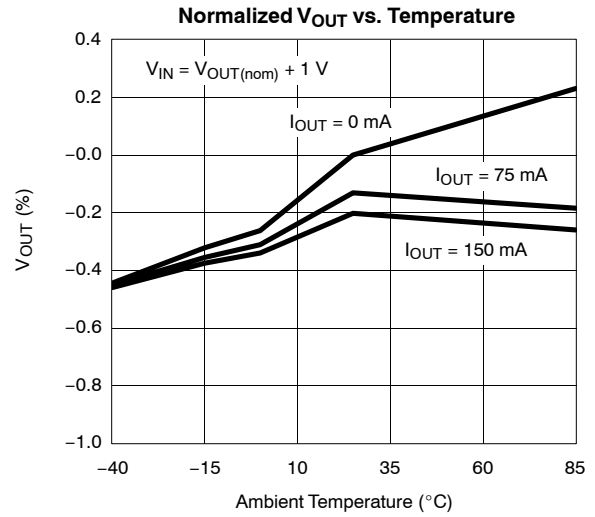
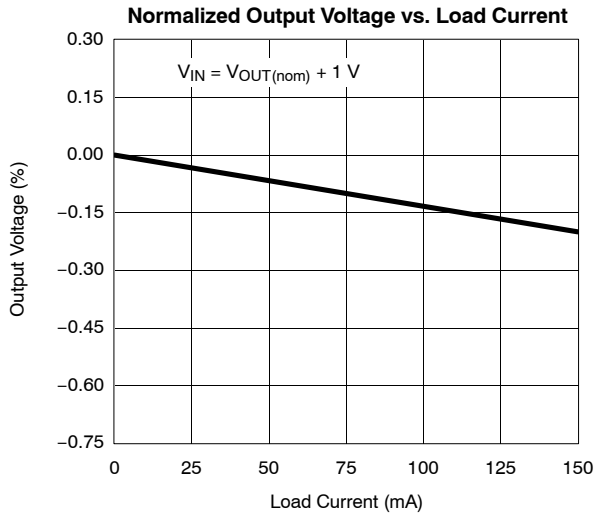
Note: LL = Lot Code

ORDERING INFORMATION—Si91846

Part Number	Lead (Pb)-Free Part Number	Marking	Voltage	Temperature Range	Package
Si91846DT-18-T1	Si91846DT-18-T1—E3	I4LL	1.8	-40 to 85°C	Thin SOT23-6
Si91846DT-20-T1	Si91846DT-20-T1—E3	I5LL	2.0		
Si91846DT-22-T1	Si91846DT-22-T1—E3	I6LL	2.2		
Si91846DT-25-T1	Si91846DT-25-T1—E3	I7LL	2.5		
Si91846DT-26-T1	Si91846DT-26-T1—E3	I8LL	2.6		
Si91846DT-27-T1	Si91846DT-27-T1—E3	I9LL	2.7		
Si91846DT-28-T1	Si91846DT-28-T1—E3	I0LL	2.8		
Si91846DT-285-T1	Si91846DT-285—E3	J1LL	2.85		
Si91846DT-29-T1	Si91846DT-29-T1—E3	J2LL	2.9		
Si91846DT-30-T1	Si91846DT-30-T1—E3	J3LL	3.0		
Si91846DT-33-T1	Si91846DT-33-T1—E3	J4LL	3.3		
Si91846DT-35-T1	Si91846DT-35-T1—E3	J5LL	3.5		
Si91846DT-36-T1	Si91846DT-36-T1—E3	J6LL	3.6		
Si91846DT-50-T1	Si91846DT-50-T1—E3	J7LL	5.0		

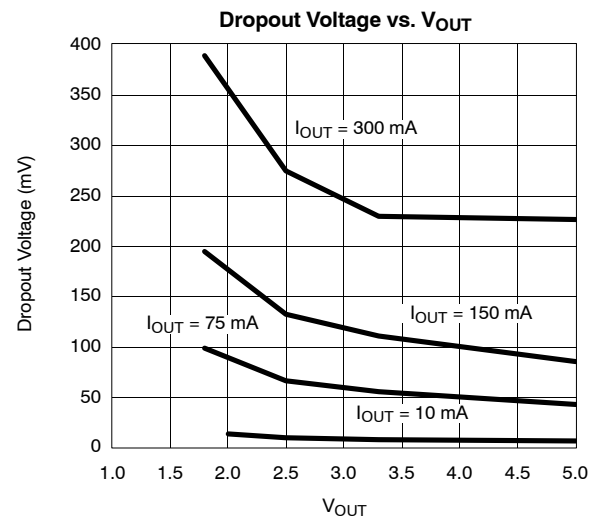
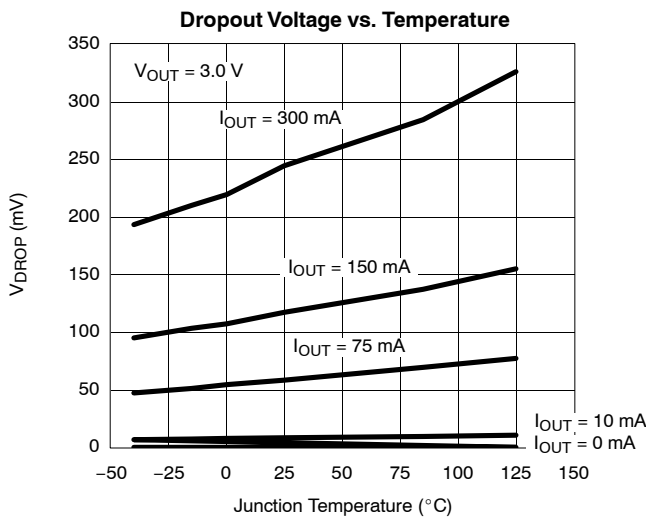
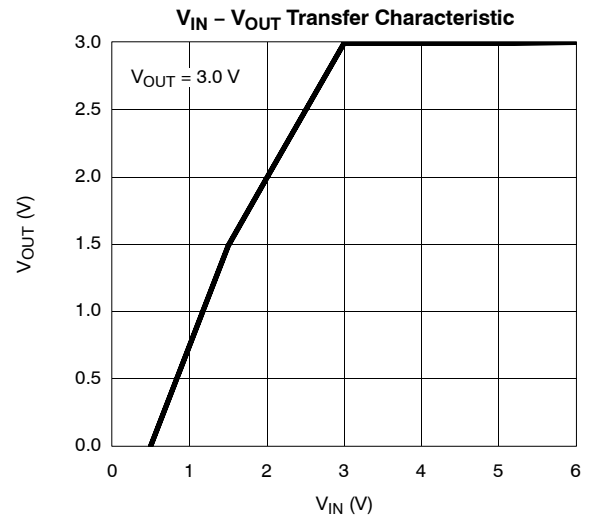
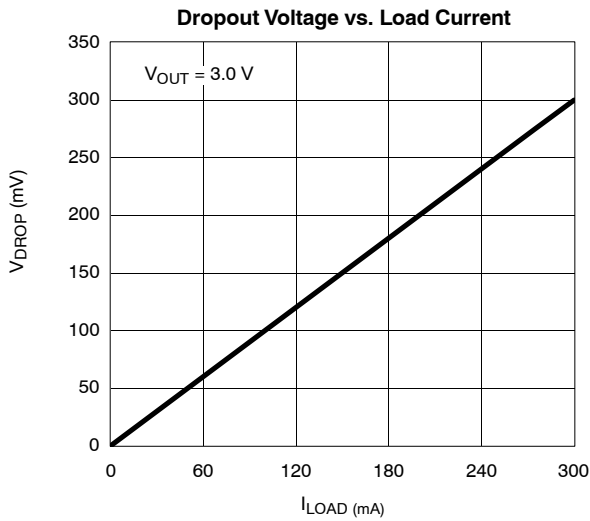
Note: LL = Lot Code

TYPICAL CHARACTERISTICS (INTERNALLY REGULATED, 25°C UNLESS NOTED)



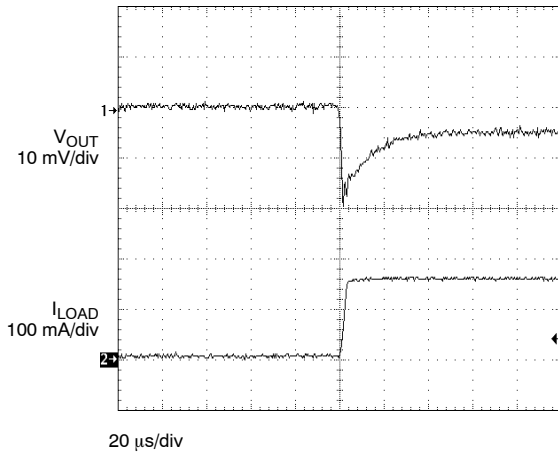


TYPICAL CHARACTERISTICS (INTERNALLY REGULATED, 25°C UNLESS NOTED)



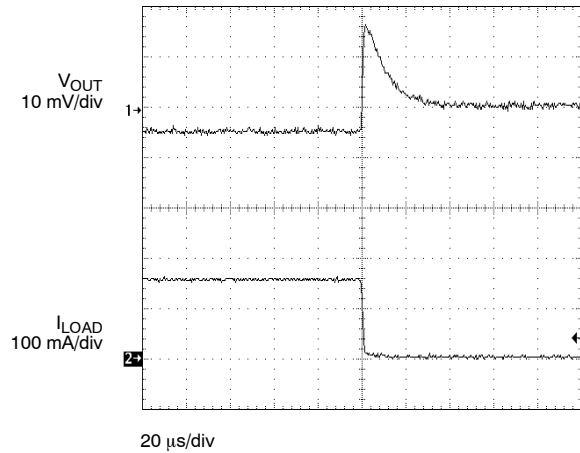
TYPICAL WAVEFORMS

Load Transient Response-1



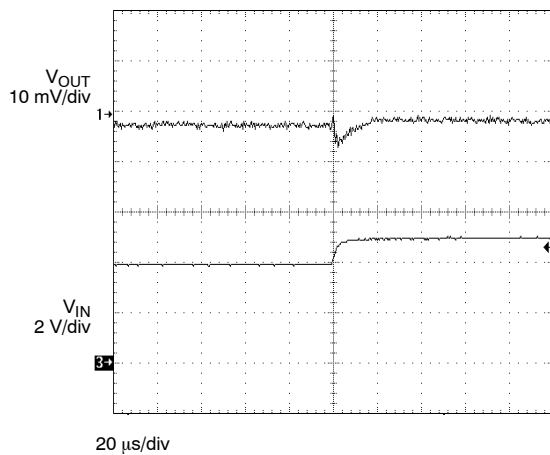
$V_{OUT} = 3.0\text{ V}$
 $C_{OUT} = 1\ \mu\text{F}$
 $I_{LOAD} = 1\ \text{to}\ 150\ \text{mA}$
 $t_{rise} = 2\ \mu\text{sec}$

Load Transient Response-2



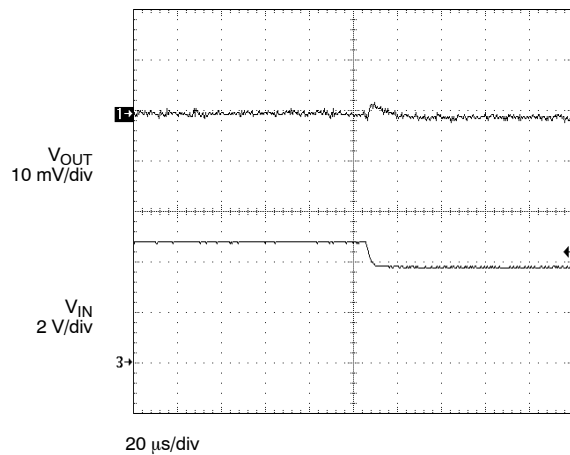
$V_{OUT} = 3.0\text{ V}$
 $C_{OUT} = 1\ \mu\text{F}$
 $I_{LOAD} = 150\ \text{to}\ 1\ \text{mA}$
 $t_{fall} = 2\ \mu\text{sec}$

Line Transient Response-1



$V_{INSTEP} = 4\ \text{to}\ 5\ \text{V}$
 $V_{OUT} = 3\ \text{V}$
 $C_{OUT} = 1\ \mu\text{F}$
 $C_{IN} = 1\ \mu\text{F}$
 $I_{LOAD} = 150\ \text{mA}$
 $t_{rise} = 5\ \mu\text{sec}$

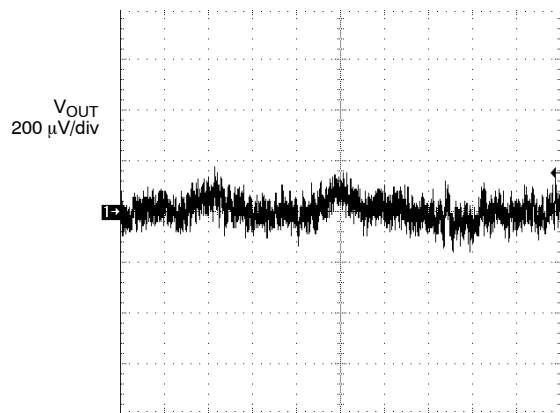
Line Transient Response-2



$V_{INSTEP} = 5\ \text{to}\ 4\ \text{V}$
 $V_{OUT} = 3\ \text{V}$
 $C_{OUT} = 1\ \mu\text{F}$
 $C_{IN} = 1\ \mu\text{F}$
 $I_{LOAD} = 150\ \text{mA}$
 $t_{fall} = 5\ \mu\text{sec}$

TYPICAL WAVEFORMS

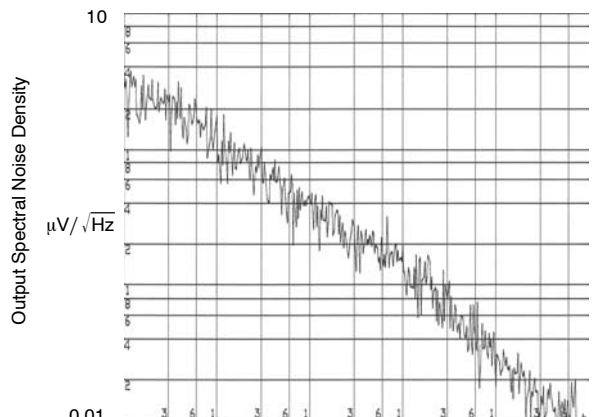
Output Noise



4 ms/div

$V_{IN} = 4\text{ V}$
 $V_{OUT} = 3\text{ V}$
 $I_{OUT} = 150\text{ mA}$
 $C_{NOISE} = 0.01\text{ }\mu\text{F}$
 $BW = 10\text{ Hz to }100\text{ kHz}$

Noise Spectrum

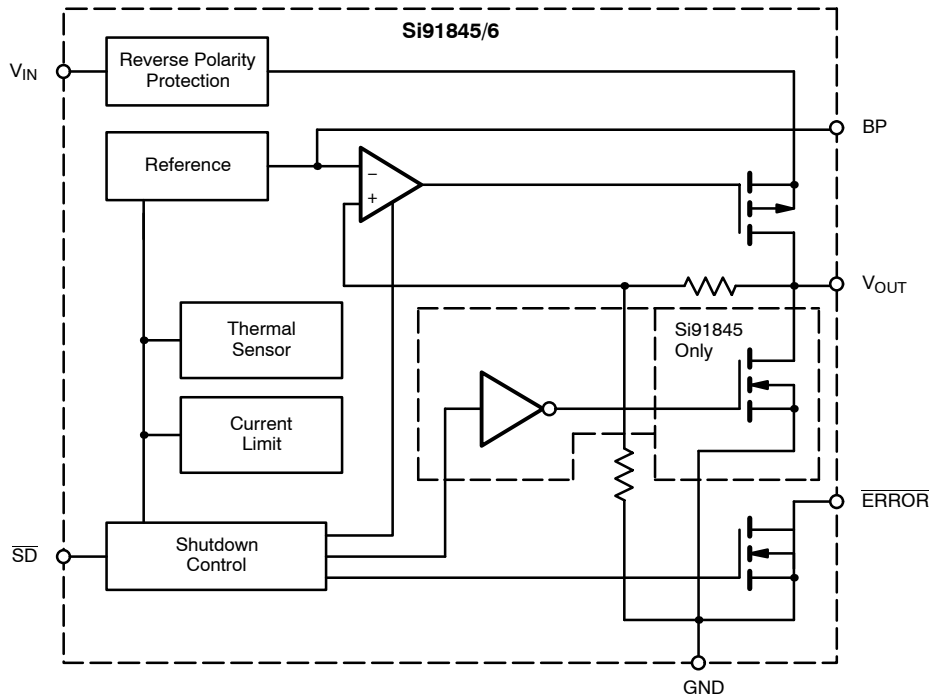


10 Hz

1 MHz

$V_{IN} = 4\text{ V}$
 $V_{OUT} = 3\text{ V}$
 $I_{LOAD} = 150\text{ mA}$
 $C_{NOISE} = 0.01\text{ }\mu\text{F}$

BLOCK DIAGRAM



DETAILED DESCRIPTION

The Si91845/6 is a low-noise, low drop-out and low quiescent current linear voltage regulator, packaged in a small footprint Thin SOT23-6 package. The Si91845/6 can supply loads up to 300 mA. As shown in the block diagram, the circuit consists of a bandgap reference, error amplifier, p-channel pass transistor and feedback resistor string. An external bypass capacitor connected to the BP pin reduces noise at the output. Additional blocks, not shown in the block diagram, include a precise current limiter, reverse battery and current protection, and thermal sensor.

Thermal Overload Protection

The thermal overload protection limits the total power dissipation and protects the device from being damaged. When the junction temperature exceeds 150°, the device turns the p-channel pass transistor off.

Reverse Battery Protection

The Si91845/6 has a battery reverse protection circuitry that disconnects the internal circuitry when V_{IN} drops below the GND voltage. There is no current drawn in such an event. When the \overline{SD} pin is hardwired to V_{IN} , the user must connect the \overline{SD} pin to V_{IN} via a 100-k Ω resistor if reverse battery protection is desired. Hardwiring the \overline{SD} pin directly to the V_{IN} pin is allowed when reverse battery protection is not desired.

Noise Reduction

An external 10-nF bypass capacitor at BP is used to create a low pass filter for noise reduction. The start-up time is fast, since a

power-on circuit pre-charges the bypass capacitor. After the power-up sequence the pre-charge circuit is switched to standby mode in order to save current. It is therefore not recommended to use larger bypass capacitor values than 50 nF. When the circuit is used without a capacitor, stable operation is guaranteed.

ERROR

\overline{ERROR} is an open drain output that goes low when V_{OUT} is less than 4% of its normal value. To obtain a logic level output, connect a pull-up resistor from \overline{ERROR} to V_{OUT} or any other voltage equal to or less than V_{IN} . \overline{ERROR} pin is high impedance (off) when \overline{SD} pin is low.

Auto-Discharge/No-Discharge

V_{OUT} has an internal 100- Ω (typ.) discharge path to ground when \overline{SD} pin is low. This applies only to the Si91845. The Si91846 does not have a discharge path when the \overline{SD} pin is low.

Stability

The circuit is stable with only a small output capacitor equal to 6 nF/mA (= 1 μ F @ 150 mA). Since the bandwidth of the error amplifier is around 1–3 MHz and the dominant pole is at the output node, the capacitor should be capacitive in this range, i.e., for 150-mA load current, an ESR <0.4 Ω is necessary. Parasitic inductance of about 10 nH can be tolerated.