DATA SHEET

Xilinx has acquired the entire Phillips CoolRunner Low Power CPLD Product Family. For more technical or sales information, please see: www.xilinx.com

XCR5064

64 macrocell CPLD

Product specification
Supersedes data of 1997 Mar 05
IC27 Data Handbook

1998 Jul 23

Philips
Semiconductors

PHILIPS

64 macrocell CPLD

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FEATURES

- Industry's first TotalCMOS™ PLD – both CMOS design and process technologies
- Fast Zero Power (FZP™) design technique provides ultra-low power and very high speed
- High speed pin-to-pin delays of 7.5ns
- Ultra-low static power of less than 100µA
- Dynamic power that is 70% lower at 50MHz than competing devices
- 100% routable with 100% utilization while all pins and all macrocells are fixed
- Deterministic timing model that is extremely simple to use
- 4 clocks with programmable polarity at every macrocell
- Support for asynchronous clocking
- Innovative XPLA™ architecture combines high speed with extreme flexibility
- 1000 erase/program cycles guaranteed
- 20 years data retention guaranteed
- Logic expandable to 37 product terms
- PCI compliant
- Advanced 0.5µ E^2CMOS process
- Security bit prevents unauthorized access
- Design entry and verification using industry standard and Philips CAE tools
- Reprogrammable using industry standard device programmers
- Innovative Control Term structure provides either sum terms or product terms in each logic block for:
  - Programmable 3-State buffer
  - Asynchronous macrocell register preset/reset
- Programmable global 3-State pin facilitates 'bed of nails' testing without using logic resources
- Available in PLCC, TQFP, and PQFP packages
- Available in both Commercial and Industrial grades

Table 1. PZ5064 Features

	PZ5064
Usable gates	2000
Maximum inputs	68
Maximum I/Os	64
Number of macrocells	64
Propagation delay (ns)	7.5
Packages	44-pin PLCC, 44-pin TQFP, 68-pin PLCC, 84-pin PLCC, 100-pin PQFP

DESCRIPTION

The PZ5064 CPLD (Complex Programmable Logic Device) is the second in a family of Fast Zero Power (FZP™) CPLDs from Philips Semiconductors. These devices combine high speed and zero power in a 64 macrocell CPLD. With the FZP™ design technique, the PZ5064 offers true pin-to-pin speeds of 7.5ns, while simultaneously delivering power that is less than 100µA at standby without the need for 'turbo bits' or other power down schemes. By replacing conventional sense amplifier methods for implementing product terms (a technique that has been used in PLDs since the bipolar era) with a cascaded chain of pure CMOS gates, the dynamic power is also substantially lower than any competing CPLD – 70% lower at 50MHz. These devices are the first TotalCMOS™ PLDs, as they use both a CMOS process technology **and** the patented full CMOS FZP™ design technique. For 3V applications, Philips also offers the high speed PZ3064 CPLD that offers these features in a full 3V implementation.

The Philips FZP™ CPLDs introduce the new patent-pending XPLA™ (eXtended Programmable Logic Array) architecture. The XPLA™ architecture combines the best features of both PLA and PAL™ type structures to deliver high speed and flexible logic allocation that results in superior ability to make design changes with fixed pinouts. The XPLA™ structure in each logic block provides a fast 7.5ns PAL™ path with 5 dedicated product terms per output. This PAL™ path is joined by an additional PLA structure that deploys a pool of 32 product terms to a fully programmable OR array that can allocate the PLA product terms to any output in the logic block. This combination allows logic to be allocated efficiently throughout the logic block and supports as many as 37 product terms on an output. The speed with which logic is allocated from the PLA array to an output is only 2.0ns, regardless of the number of PLA product terms used, which results in worst case t_{PD}'s of only 9.5ns from any pin to any other pin. In addition, logic that is common to multiple outputs can be placed on a single PLA product term and shared across multiple outputs via the OR array, effectively increasing design density.

The PZ5064 CPLDs are supported by industry standard CAE tools (Cadence, Exemplar Logic, Minc, Mentor, Synopsys, Synario, Viewlogic, MINC), using text (Abel, VHDL, Verilog) and/or schematic entry. Design verification uses industry standard simulators for functional and timing simulation. Development is supported on personal computer, Sparc, and HP platforms. Device fitting uses either Minc or Philips Semiconductors-developed tools.

The PZ5064 CPLD is reprogrammable using industry standard device programmers from vendors such as Data I/O, BP Microsystems, SMS, and others.

PAL is a registered trademark of Advanced Micro Devices, Inc.

ORDERING INFORMATION

ORDER CODE	DESCRIPTION	DESCRIPTION	DRAWING NUMBER
PZ5064-7A44	44-pin PLCC, 7.5ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT187-2
PZ5064-10A44	44-pin PLCC, 10ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT187-2
PZ5064I10A44	44-pin PLCC, 10ns t_{PD}	Industrial temp range, 5 volt power supply, ± 10%	SOT187-2
PZ5064I12A44	44-pin PLCC, 12ns t_{PD}	Industrial temp range, 5 volt power supply, ± 10%	SOT187-2
PZ5064-7BC	44-pin TQFP, 7.5ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT376-1
PZ5064-10BC	44-pin TQFP, 10ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT376-1
PZ5064I10BC	44-pin TQFP, 10ns t_{PD}	Industrial temp range, 5 volt power supply, ± 10%	SOT376-1
PZ5064I12BC	44-pin TQFP, 12ns t_{PD}	Industrial temp range, 5 volt power supply, ± 10%	SOT376-1
PZ5064-7A68	68-pin PLCC, 7.5ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT188-3
PZ5064-10A68	68-pin PLCC, 10ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT188-3
PZ5064I10A68	68-pin PLCC, 10ns t_{PD}	Industrial temp range, 5 volt power supply, ± 10%	SOT188-3
PZ5064I12A68	68-pin PLCC, 12ns t_{PD}	Industrial temp range, 5 volt power supply, ± 10%	SOT188-3
PZ5064-7A84	84-pin PLCC, 7.5ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT189-3
PZ5064-10A84	84-pin PLCC, 10ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT189-3
PZ5064I10A84	84-pin PLCC, 10ns t_{PD}	Industrial temp range, 5 volt power supply, ± 10%	SOT189-3
PZ5064I12A84	84-pin PLCC, 12ns t_{PD}	Industrial temp range, 5 volt power supply, ± 10%	SOT189-3
PZ5064-7BB1	100-pin PQFP, 7.5ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT382-1
PZ5064-10BB1	100-pin PQFP, 10ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT382-1
PZ5064I10BB1	100-pin PQFP, 10ns t_{PD}	Industrial temp range, 5 volt power supply, ± 10%	SOT382-1
PZ5064I12BB1	100-pin PQFP, 12ns t_{PD}	Industrial temp range, 5 volt power supply, ± 10%	SOT382-1

XPLA™ ARCHITECTURE

Figure 1 shows a high level block diagram of a 64 macrocell device implementing the XPLA™ architecture. The XPLA™ architecture consists of logic blocks that are interconnected by a Zero-power Interconnect Array (ZIA). The ZIA is a virtual crosspoint switch. Each logic block is essentially a 36V16 device with 36 inputs from the ZIA and 16 macrocells. Each logic block also provides 32 ZIA feedback paths from the macrocells and I/O pins.

From this point of view, this architecture looks like many other CPLD architectures. What makes the CoolRunner™ family unique is what is inside each logic block and the design technique used to implement these logic blocks. The contents of the logic block will be described next.

Logic Block Architecture

Figure 2 illustrates the logic block architecture. Each logic block contains control terms, a PAL array, a PLA array, and 16 macrocells. the 6 control terms can individually be configured as either SUM or PRODUCT terms, and are used to control the preset/reset and output enables of the 16 macrocells' flip-flops. The PAL array consists of a programmable AND array with a fixed OR array, while the PLA array consists of a programmable AND array with a programmable OR array. The PAL array provides a high speed path through the array, while the PLA array provides increased product term density.

Each macrocell has 5 dedicated product terms from the PAL array. The pin-to-pin t_{PD} of the PZ5064 device through the PAL array is 7.5ns. If a macrocell needs more than 5 product terms, it simply gets the additional product terms from the PLA array. The PLA array consists of 32 product terms, which are available for use by all 16 macrocells. The additional propagation delay incurred by a macrocell using 1 or all 32 PLA product terms is just 2.0ns. So the total pin-to-pin t_{PD} for the PZ5064 using 6 to 37 product terms is 9.5ns (7.5ns for the PAL + 2.0ns for the PLA).

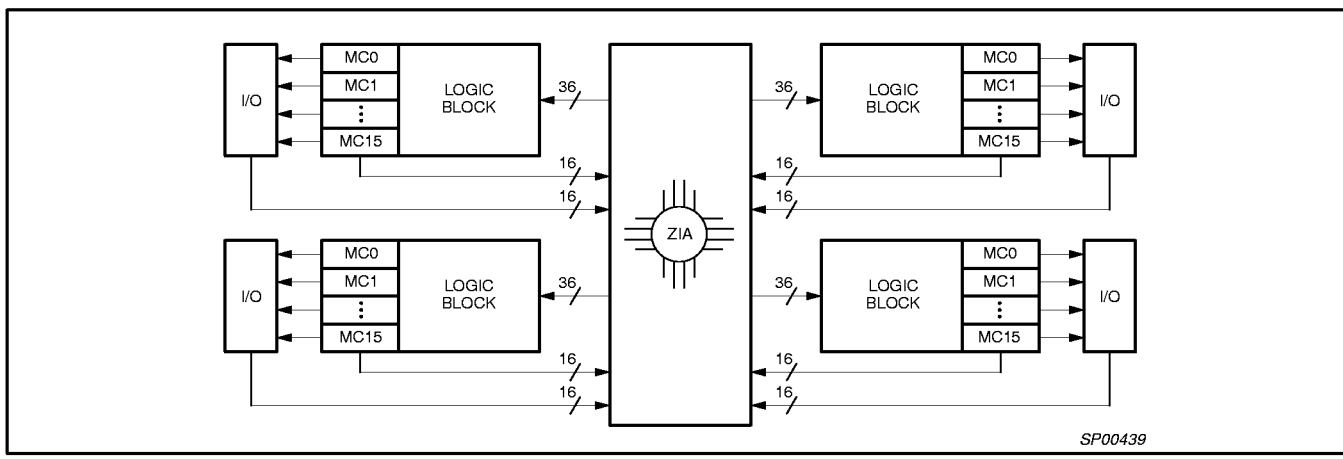


Figure 1. Philips XPLA CPLD Architecture

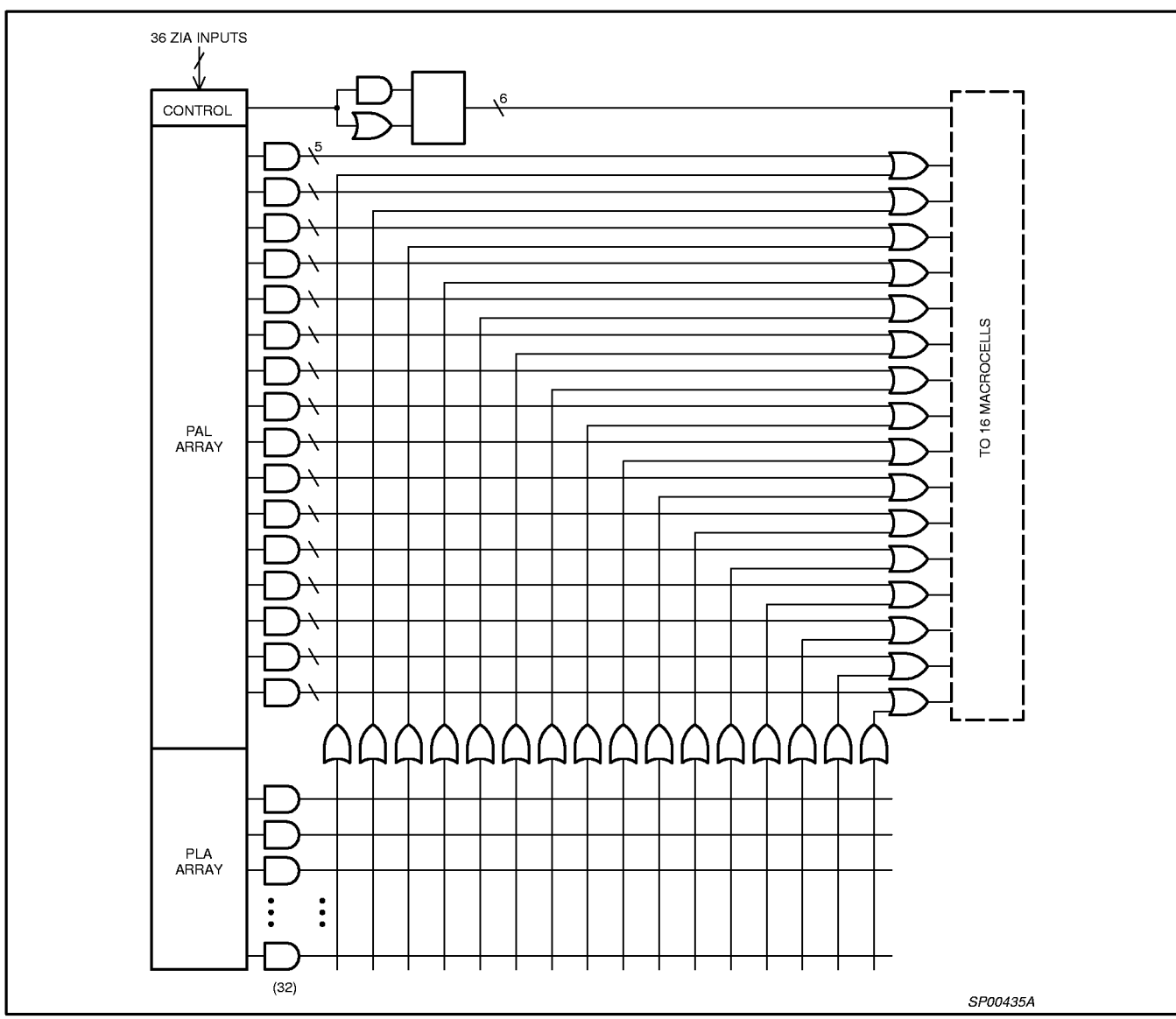


Figure 2. Philips XPLA Logic Block Architecture

Macrocell Architecture

Figure 3 shows the architecture of the macrocell used in the CoolRunner™ family. The macrocell consists of a flip-flop that can be configured as either a D or T type. A D-type flip-flop is generally more useful for implementing state machines and data buffering. A T-type flip-flop is generally more useful in implementing counters. All CoolRunner™ family members provide both synchronous and asynchronous clocking and provide the ability to clock off either the falling or rising edges of these clocks. These devices are designed such that the skew between the rising and falling edges of a clock are minimized for clocking integrity. There are 4 clocks available on the PZ5064 device. Clock 0 (CLK0) is designated as the "synchronous" clock and must be driven by an external source. Clock 1 (CLK1), Clock 2 (CLK2), and Clock 3 (CLK3) can either be used as a synchronous clock (driven by an external source) or as an asynchronous clock (driven by a macrocell equation). The timing for asynchronous clocks is different in that the t_{CO} time is extended by the amount of time that it takes for the signal to propagate through the array and reach the clock network, and the t_{SU} time is reduced. Please see the application note titled "Understanding CoolRunner Clocking Options" for more detail.

Two of the control terms (CT0 and CT1) are used to control the Preset/Reset of the macrocell's flip-flop. The Preset/Reset feature for each macrocell can also be disabled. Note that the Power-on Reset leaves all macrocells in the "zero" state when power is properly applied. The other 4 control terms (CT2–CT5) can be used to control the Output Enable of the macrocell's output buffers. The reason there are as many control terms dedicated for the Output Enable of the macrocell is to insure that all CoolRunner™ devices are PCI compliant. The macrocell's output buffers can also be always enabled or disabled. All CoolRunner™ devices also provide a Global Tri-State ($\overline{GTS}$) pin, which, when enabled and pulled Low, will 3-State all the outputs of the device. This pin is provided to support "In-Circuit Testing" or "Bed-of-Nails Testing".

There are two feedback paths to the ZIA: one from the macrocell, and one from the I/O pin. The ZIA feedback path before the output buffer is the macrocell feedback path, while the ZIA feedback path after the output buffer is the I/O pin ZIA path. When the macrocell is used as an output, the output buffer is enabled, and the macrocell feedback path can be used to feedback the logic implemented in the macrocell. When the I/O pin is used as an input, the output buffer will be 3-Stated and the input signal will be fed into the ZIA via the I/O feedback path, and the logic implemented in the buried macrocell can be fed back to the ZIA via the macrocell feedback path. It should be noted that unused inputs or I/Os should be properly terminated.

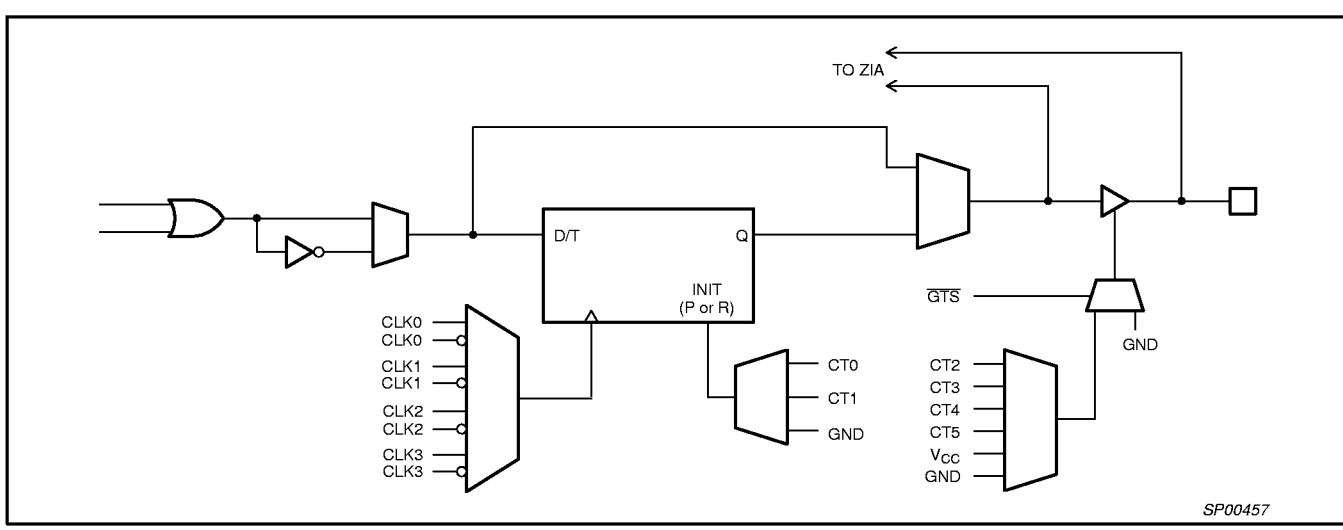


Figure 3. PZ5064 Macrocell Architecture

Simple Timing Model

Figure 4 shows the CoolRunner™ Timing Model. The CoolRunner™ timing model looks very much like a 22V10 timing model in that there are three main timing parameters, including t_{PD}, t_{SU}, and t_{CO}. In other competing architectures, the user may be able to fit the design into the CPLD, but is not sure whether system timing requirements can be met until after the design has been fit into the device. This is because the timing models of competing architectures are very complex and include such things as timing dependencies on the number of parallel expanders borrowed, sharable expanders, varying number of X and Y routing channels used, etc. In the XPLA™ architecture, the user knows up front whether the design will meet system timing requirements. This is due to the simplicity of the timing model. For example, in the PZ5064 device, the user knows up front that if a given output uses 5 product terms or less, the t_{PD} = 7.5ns, the t_{SU_PAL} = 4ns, and the t_{CO} = 5.5ns. If an output is using 6 to 37 product terms, an additional 2ns must be added to the t_{PD} and t_{SU} timing parameters to account for the time to propagate through the PLA array.

TotalCMOS™ Design Technique for Fast Zero Power

Philips is the first to offer a TotalCMOS™ CPLD, both in process technology and design technique. Philips employs a cascade of CMOS gates to implement its Sum of Products instead of the traditional sense amp approach. This CMOS gate implementation allows Philips to offer CPLDs which are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. Refer to Figure 5 and Table 2 showing the I_{DD} vs. Frequency of our PZ5064 TotalCMOS™ CPLD.

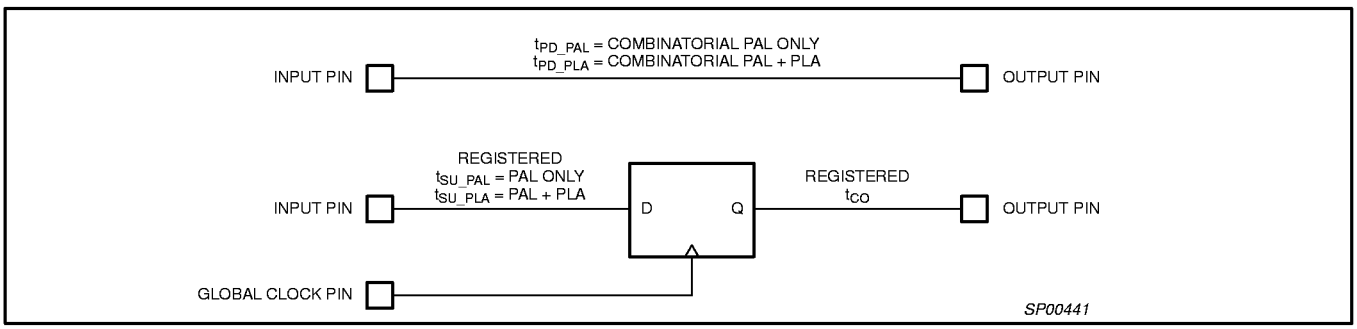


Figure 4. CoolRunner™ Timing Model

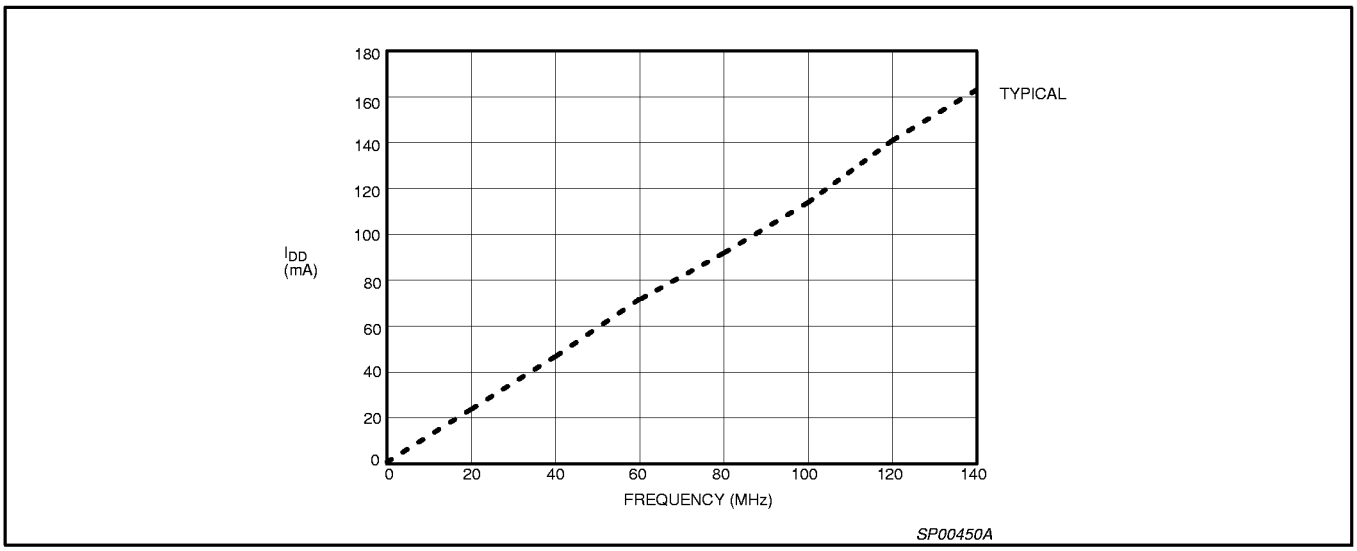


Figure 5. I_{DD} vs. Frequency @ V_{DD} = 5.0V, 25°C

Table 2. I_{DD} vs. Frequency

V_{DD} = 5.00V

FREQUENCY (MHz)	0	20	40	60	80	100	120	140
Typical I_{DD} (mA)	0.08	24	47	72	92	114	141	163

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Supply voltage[2]	–0.5	7.0	V
V_I	Input voltage	–1.2	V_{DD}+0.5	V
V_{OUT}	Output voltage	–0.5	V_{DD}+0.5	V
I_{IN}	Input current	–30	30	mA
I_{OUT}	Output current	–100	100	mA
T_J	Maximum junction temperature	–40	150	°C
T_{str}	Storage temperature	–65	150	°C

NOTES:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification is not implied.
2. The chip supply voltage must rise monotonically.

OPERATING RANGE

PRODUCT GRADE	TEMPERATURE	VOLTAGE
Commercial	0 to +70°C	5.0 ±5% V
Industrial	–40 to +85°C	5.0 ±10% V

DC ELECTRICAL CHARACTERISTICS FOR COMMERCIAL GRADE DEVICES

Commercial: 0°C ≤ T_{amb} ≤ +70°C; 4.75V ≤ V_{DD} ≤ 5.25V

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
V_{IL}	Input voltage low	V_{DD} = 4.75V		0.8	V
V_{IH}	Input voltage high	V_{DD} = 5.25V	2.0		V
V_I	Input clamp voltage	V_{DD} = 4.75V, I_{IN} = –18mA		–1.2	V
V_{OL}	Output voltage low	V_{DD} = 4.75V, I_{OL} = 12mA		0.5	V
V_{OH}	Output voltage high	V_{DD} = 4.75V, I_{OH} = –12mA	2.4		V
I_I	Input leakage current	V_{IN} = 0 to V_{DD}	–10	10	µA
I_{OZ}	3-Stated output leakage current	V_{IN} = 0 to V_{DD}	–10	10	µA
I_{DDQ}[1]	Standby current	V_{DD} = 5.25V, T_{amb} = 0°C		80	µA
I_{DDD}[1, 2]	Dynamic current	V_{DD} = 5.25V, T_{amb} = 0°C @ 1MHz		3	mA
		V_{DD} = 5.25V, T_{amb} = 0°C @ 50MHz		65	mA
I_{OS}	Short circuit output current[3]	1 pin at a time for no longer than 1 second	–50	–200	mA
C_{IN}	Input pin capacitance[3]	T_{amb} = 25°C, f = 1MHz		8	pF
C_{CLK}	Clock input capacitance[3]	T_{amb} = 25°C, f = 1MHz	5	12	pF
$C_{I/O}$	I/O pin capacitance[3]	T_{amb} = 25°C, f = 1MHz		10	pF

NOTES:
1. See Table 2 on page 6 for typical values.
2. This parameter measured with a 16-bit, loadable up/down counter loaded into every logic block, with all outputs enabled and unloaded. Inputs are tied to V_{DD} or ground. This parameter guaranteed by design and characterization, not testing.
3. Typical values, not tested.

AC ELECTRICAL CHARACTERISTICS[1] FOR COMMERCIAL GRADE DEVICES

Commercial: 0°C ≤ T_{amb} ≤ +70°C; 4.75V ≤ V_{DD} ≤ 5.25V

SYMBOL	PARAMETER	7		10		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{PD_PAL}	Propagation delay time, input (or feedback node) to output through PAL	2	7.5	2	10	ns
t_{PD_PLA}	Propagation delay time, input (or feedback node) to output through PAL & PLA	3	9.5	3	12.5	ns
t_{CO}	Clock to out (global synchronous clock from pin)	2	5.5	2	7	ns
t_{SU_PAL}	Setup time (from input or feedback node) through PAL	4		6		ns
t_{SU_PLA}	Setup time (from input or feedback node) through PAL + PLA	6		8.5		ns
t_H	Hold time		0		0	ns
t_{CH}	Clock High time	4		5		ns
t_{CL}	Clock Low time	4		5		ns
t_R	Input Rise time		20		20	ns
t_F	Input Fall time		20		20	ns
f_{MAX1}	Maximum FF toggle rate[2] $(1/t_{CH} + t_{CL})$	125		100		MHz
f_{MAX2}	Maximum internal frequency[2] $(1/t_{SUPAL} + t_{CF})$	125		87		MHz
f_{MAX3}	Maximum external frequency[2] $(1/t_{SUPAL} + t_{CO})$	105		77		MHz
t_{BUF}	Output buffer delay time		1.5		1.5	ns
t_{PDF_PAL}	Input (or feedback node) to internal feedback node delay time through PAL		6		8.5	ns
t_{PDF_PLA}	Input (or feedback node) to internal feedback node delay time through PAL+PLA		8		11	ns
t_{CF}	Clock to internal feedback node delay time		4		5.5	ns
t_{INIT}	Delay from valid V_{DD} to valid reset		50		50	µs
t_{ER}	Input to output disable[2, 3]		10		12	ns
t_{EA}	Input to output valid[2]		10		12	ns
t_{RP}	Input to register preset[2]		10		12.5	ns
t_{RR}	Input to register reset[2]		10		12.5	ns

NOTES:
1. Specifications measured with one output switching. See Figure 6 and Table 3 for derating.
2. This parameter guaranteed by design and characterization, not by test.
3. Output C_L = 5pF.

DC ELECTRICAL CHARACTERISTICS FOR INDUSTRIAL GRADE DEVICES

Industrial: $-40°C \le T_{amb} \le +85°C$; $4.5V \le V_{DD} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
V_{IL}	Input voltage low	V_{DD} = 4.5V		0.8	V
V_{IH}	Input voltage high	V_{DD} = 5.5V	2.0		V
V_I	Input clamp voltage	V_{DD} = 4.5V, I_{IN} = –18mA		–1.2	V
V_{OL}	Output voltage low	V_{DD} = 4.5V, I_{OL} = 12mA		0.5	V
V_{OH}	Output voltage high	V_{DD} = 4.5V, I_{OH} = –12mA	2.4		V
I_I	Input leakage current	V_{IN} = 0 to V_{DD}	–10	10	µA
I_{OZ}	3-Stated output leakage current	V_{IN} = 0 to V_{DD}	–10	10	µA
I_{DDQ}[1]	Standby current	V_{DD} = 5.5V, T_{amb} = –40°C		100	µA
I_{DDD}[1, 2]	Dynamic current	V_{DD} = 5.5V, T_{amb} = –40°C @ 1MHz		4	mA
		V_{DD} = 5.5V, T_{amb} = –40°C @ 50MHz		70	mA
I_{OS}	Short circuit output current[3]	1 pin at a time for no longer than 1 second	–50	–230	mA
C_{IN}	Input pin capacitance[3]	T_{amb} = 25°C, f = 1MHz		8	pF
C_{CLK}	Clock input capacitance[3]	T_{amb} = 25°C, f = 1MHz	5	12	pF
$C_{I/O}$	I/O pin capacitance[3]	T_{amb} = 25°C, f = 1MHz		10	pF

NOTE:
1. See Table 2 on page 6 for typical values.
2. This parameter measured with a 16–bit, loadable up/down counter loaded into every logic block, with all outputs enabled and unloaded. Inputs are tied to V_{DD} or ground. This parameter guaranteed by design and characterization, not testing.
3. Typical values, not tested.

AC ELECTRICAL CHARACTERISTICS[1] FOR INDUSTRIAL GRADE DEVICES

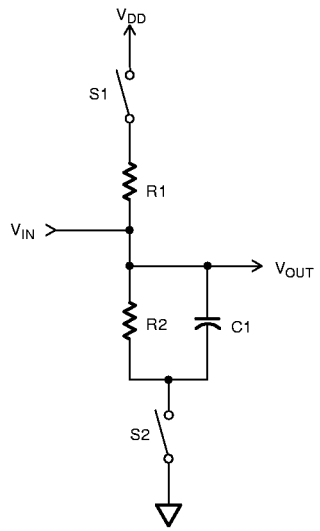
Industrial: $-40°C \le T_{amb} \le +85°C$; $4.5V \le V_{DD} \le 5.5V$

SYMBOL	PARAMETER	10		12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{PD_PAL}	Propagation delay time, input (or feedback node) to output through PAL	2	10	2	12	ns
t_{PD_PLA}	Propagation delay time, input (or feedback node) to output through PAL & PLA	3	12.5	3	14.5	ns
t_{CO}	Clock to out (global synchronous clock from pin)	2	7	2	8	ns
t_{SU_PAL}	Setup time (from input or feedback node) through PAL	6		7		ns
t_{SU_PLA}	Setup time (from input or feedback node) through PAL + PLA	8.5		9.5		ns
t_H	Hold time		0		0	ns
t_{CH}	Clock High time	5		5		ns
t_{CL}	Clock Low time	5		5		ns
t_R	Input Rise time		20		20	ns
t_F	Input Fall time		20		20	ns
f_{MAX1}	Maximum FF toggle rate[2] $(1/t_{CH} + t_{CL})$	100		100		MHz
f_{MAX2}	Maximum internal frequency[2] $(1/t_{SUPAL} + t_{CF})$	87		74		MHz
f_{MAX3}	Maximum external frequency[2] $(1/t_{SUPAL} + t_{CO})$	77		67		MHz
t_{BUF}	Output buffer delay time		1.5		1.5	ns
t_{PDF_PAL}	Input (or feedback node) to internal feedback node delay time through PAL		8.5		10.5	ns
t_{PDF_PLA}	Input (or feedback node) to internal feedback node delay time through PAL+PLA		11		13	ns
t_{CF}	Clock to internal feedback node delay time		5.5		6.5	ns
t_{INIT}	Delay from valid V_{DD} to valid reset		50		50	µs
t_{ER}	Input to output disable[2, 3]		12		13	ns
t_{EA}	Input to output valid[2]		12		13	ns
t_{RP}	Input to register preset[2]		12.5		13.5	ns
t_{RR}	Input to register reset[2]		12.5		13.5	ns

NOTES:
1. Specifications measured with one output switching. See Figure 6 and Table 3 for derating.
2. This parameter guaranteed by design and characterization, not by test.
3. Output C_L = 5pF.

SWITCHING CHARACTERISTICS

The test load circuit and load values for the AC Electrical Characteristics are illustrated below.



COMPONENT	VALUES
R1	470Ω
R2	250Ω
C1	35pF

MEASUREMENT	S1	S2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_P	Closed	Closed

NOTE: For t_{PHZ} and t_{PLZ} C = 5pF

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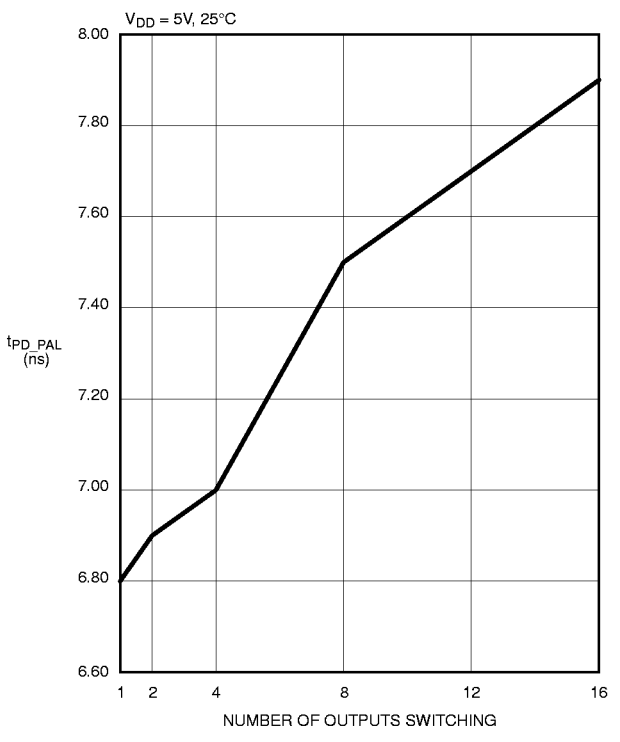

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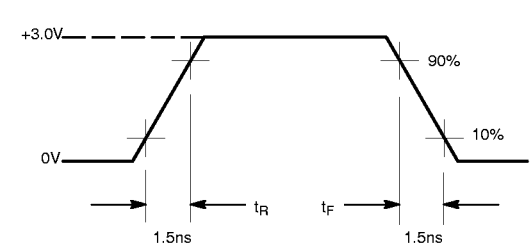
Figure 6. t_{PD_PAL} vs. Outputs Switching

VOLTAGE WAVEFORM



SP00368

MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

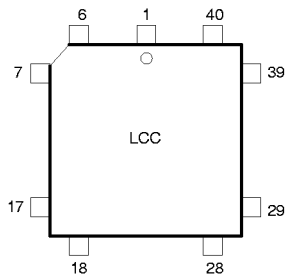
Table 3. t_{PD_PAL} vs. Number of Outputs Switching

V_{DD} = 5.00V

NUMBER OF OUTPUTS	1	2	4	8	12	16
Typical (ns)	6.8	6.9	7.0	7.5	7.7	7.9

PIN DESCRIPTIONS

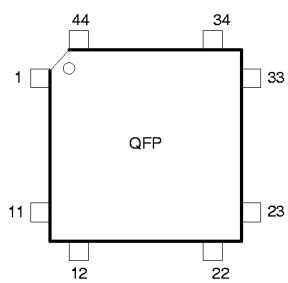
PZ5064 – 44-Pin Plastic Leaded Chip Carrier



Pin	Function	Pin	Function	Pin	Function
1	IN1	16	I/O-B10	31	I/O-C13
2	IN3	17	I/O-B8	32	I/O-C15
3	V_{DD}	18	I/O-B4	33	I/O-D15
4	I/O-A0/CK3	19	I/O-B3	34	I/O-D13
5	I/O-A2	20	I/O-B2	35	V_{DD}
6	I/O-A5	21	I/O-B0/CK2	36	I/O-D12
7	I/O-A8	22	GND	37	I/O-D11
8	I/O-A11	23	V_{DD}	38	I/O-D8
9	I/O-A12	24	I/O-C0/CK1	39	I/O-D7
10	GND	25	I/O-C2	40	I/O-D2
11	I/O-A13	26	I/O-C3	41	I/O-D0
12	I/O-A15	27	I/O-C4	42	GND
13	I/O-B15	28	I/O-C7	43	IN0-CK0
14	I/O-B13	29	I/O-C8	44	IN2-gtsn
15	V_{DD}	30	GND		

SP00452B

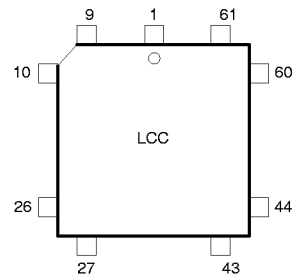
PZ5064 – 44-Pin Thin Quad Flat Package



Pin	Function	Pin	Function	Pin	Function
1	I/O-A8	16	GND	31	I/O-D11
2	I/O-A11	17	V_{DD}	32	I/O-D8
3	I/O-A12	18	I/O-C0/CK1	33	I/O-D7
4	GND	19	I/O-C2	34	I/O-D2
5	I/O-A13	20	I/O-C3	35	I/O-D0
6	I/O-A15	21	I/O-C4	36	GND
7	I/O-B15	22	I/O-C7	37	IN0/CK0
8	I/O-B13	23	I/O-C8	38	IN2-gtsn
9	V_{DD}	24	GND	39	IN1
10	I/O-B10	25	I/O-C13	40	IN3
11	I/O-B8	26	I/O-C15	41	V_{DD}
12	I/O-B4	27	I/O-D15	42	I/O-A0/CK3
13	I/O-B3	28	I/O-D13	43	I/O-A2
14	I/O-B2	29	V_{DD}	44	I/O-A5
15	I/O-B0/CK2	30	I/O-D12		

SP00453A

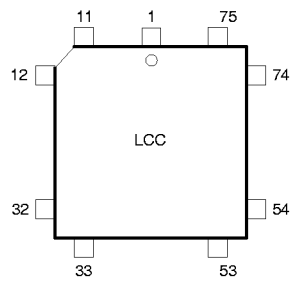
PZ5064 – 68-Pin Plastic Leaded Chip Carrier



Pin	Function	Pin	Function	Pin	Function
1	IN1	24	I/O-B10	47	I/O-C12
2	IN3	25	I/O-B8	48	GND
3	V_{DD}	26	GND	49	I/O-C13
4	I/O-A0/CK3	27	I/O-B7	50	I/O-C15
5	I/O-A2	28	I/O-B5	51	I/O-D15
6	GND	29	I/O-B4	52	I/O-D13
7	I/O-A3	30	I/O-B3	53	V_{DD}
8	I/O-A4	31	V_{DD}	54	I/O-D12
9	I/O-A5	32	I/O-B2	55	I/O-D11
10	I/O-A7	33	I/O-B0/CK2	56	I/O-D9
11	V_{DD}	34	GND	57	I/O-D8
12	I/O-A8	35	V_{DD}	58	GND
13	I/O-A10	36	I/O-C0/CK1	59	I/O-D7
14	I/O-A11	37	I/O-C2	60	I/O-D6
15	I/O-A12	38	GND	61	I/O-D4
16	GND	39	I/O-C3	62	I/O-D3
17	I/O-A13	40	I/O-C4	63	V_{DD}
18	I/O-A15	41	I/O-C5	64	I/O-D2
19	I/O-B15	42	I/O-C7	65	I/O-D0
20	I/O-B13	43	V_{DD}	66	GND
21	V_{DD}	44	I/O-C8	67	IN0/CK0
22	I/O-B12	45	I/O-C10	68	IN2-gtsn
23	I/O-B11	46	I/O-C11		

SP00454A

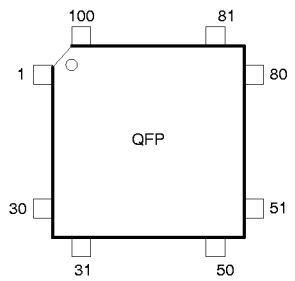
PZ5064 – 84-Pin Plastic Leaded Chip Carrier



Pin	Function	Pin	Function	Pin	Function
1	IN1	29	I/O-B10	57	I/O-C11
2	IN3	30	I/O-B9	58	I/O-C12
3	V_{DD}	31	I/O-B8	59	GND
4	I/O-A0/CK3	32	GND	60	I/O-C13
5	I/O-A1	33	I/O-B7	61	I/O-C14
6	I/O-A2	34	I/O-B6	62	I/O-C15
7	GND	35	I/O-B5	63	I/O-D15
8	I/O-A3	36	I/O-B4	64	I/O-D14
9	I/O-A4	37	I/O-B3	65	I/O-D13
10	I/O-A5	38	V_{DD}	66	V_{DD}
11	I/O-A6	39	I/O-B2	67	I/O-D12
12	I/O-A7	40	I/O-B1	68	I/O-D11
13	V_{CC}	41	I/O-B0/CK2	69	I/O-D10
14	I/O-A8	42	GND	70	I/O-D9
15	I/O-A9	43	V_{DD}	71	I/O-D8
16	I/O-A10	44	I/O-C0/CK1	72	GND
17	I/O-A11	45	I/O-C1	73	I/O-D7
18	I/O-A12	46	I/O-C2	74	I/O-D6
19	GND	47	GND	75	I/O-D5
20	I/O-A13	48	I/O-C3	76	I/O-D4
21	I/O-A14	49	I/O-C4	77	I/O-D3
22	I/O-A15	50	I/O-C5	78	V_{DD}
23	I/O-B15	51	I/O-C6	79	I/O-D2
24	I/O-B14	52	I/O-C7	80	I/O-D1
25	I/O-B13	53	V_{DD}	81	I/O-D0
26	V_{DD}	54	I/O-C8	82	GND
27	I/O-B12	55	I/O-C9	83	IN0/CK0
28	I/O-B11	56	I/O-C10	84	IN2-gtsn

SP00455A

PZ5064 – 100-Pin Plastic Quad Flat Package



Pin	Function	Pin	Function	Pin	Function
1	NC	35	I/O-B3	69	I/O-D12
2	NC	36	V_{DD}	70	I/O-D11
3	I/O-A6	37	I/O-B2	71	I/O-D10
4	I/O-A7	38	I/O-B1	72	NC
5	V_{DD}	39	I/O-B0/CK2	73	I/O-D9
6	I/O-A8	40	GND	74	NC
7	NC	41	V_{DD}	75	I/O-D8
8	I/O-A9	42	I/O-C0/CK1	76	GND
9	NC	43	I/O-C1	77	I/O-D7
10	I/O-A10	44	I/O-C2	78	I/O-D6
11	I/O-A11	45	GND	79	NC
12	I/O-A12	46	I/O-C3	80	NC
13	GND	47	I/O-C4	81	I/O-D5
14	I/O-A13	48	I/O-C5	82	I/O-D4
15	I/O-A14	49	I/O-C6	83	I/O-D3
16	I/O-A15	50	I/O-C7	84	V_{DD}
17	I/O-B15	51	NC	85	I/O-D2
18	I/O-B14	52	NC	86	I/O-D1
19	I/O-B13	53	V_{DD}	87	I/O-D0
20	V_{DD}	54	I/O-C8	88	GND
21	I/O-B12	55	NC	89	IN0/CK0
22	I/O-B11	56	I/O-C9	90	IN2-gtsn
23	I/O-B10	57	NC	91	IN1
24	NC	58	I/O-C10	92	IN3
25	I/O-B9	59	I/O-C11	93	V_{DD}
26	NC	60	I/O-C12	94	I/O-A0/CK3
27	I/O-B8	61	GND	95	I/O-A1
28	GND	62	I/O-C13	96	I/O-A2
29	NC	63	I/O-C14	97	GND
30	NC	64	I/O-C15	98	I/O-A3
31	I/O-B7	65	I/O-D15	99	I/O-A4
32	I/O-B6	66	I/O-D14	100	I/O-A5
33	I/O-B5	67	I/O-D13		
34	I/O-B4	68	V_{DD}		

SP00456A

Package Thermal Characteristics

Philips Semiconductors uses the Temperature Sensitive Parameter (TSP) method to test thermal resistance. This method meets Mil-Std-883C Method 1012.1 and is described in Philips *1995 IC Package Databook*. Thermal resistance varies slightly as a function of input power. As input power increases, thermal resistance changes approximately 5% for a 100% change in power.

Figure 7 is a derating curve for the change in Θ_{JA} with airflow based on wind tunnel measurements. It should be noted that the wind flow dynamics are more complex and turbulent in actual applications than in a wind tunnel. Also, the test boards used in the wind tunnel contribute significantly to forced convection heat transfer, and may not be similar to the actual circuit board, especially in size.

Package	Θ_{JA}
44-pin PLCC	44.9°C/W
44-pin TQFP	60.8°C/W
68-pin PLCC	44.9°C/W
84-pin PLCC	34.7°C/W
100-pin PQFP	44.5°C/W

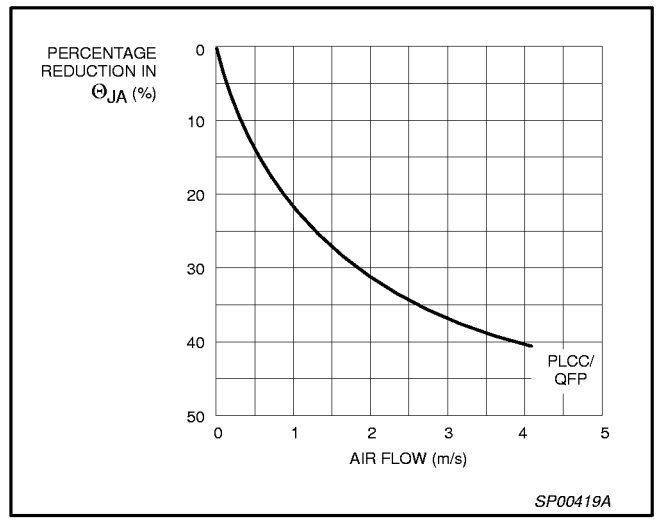
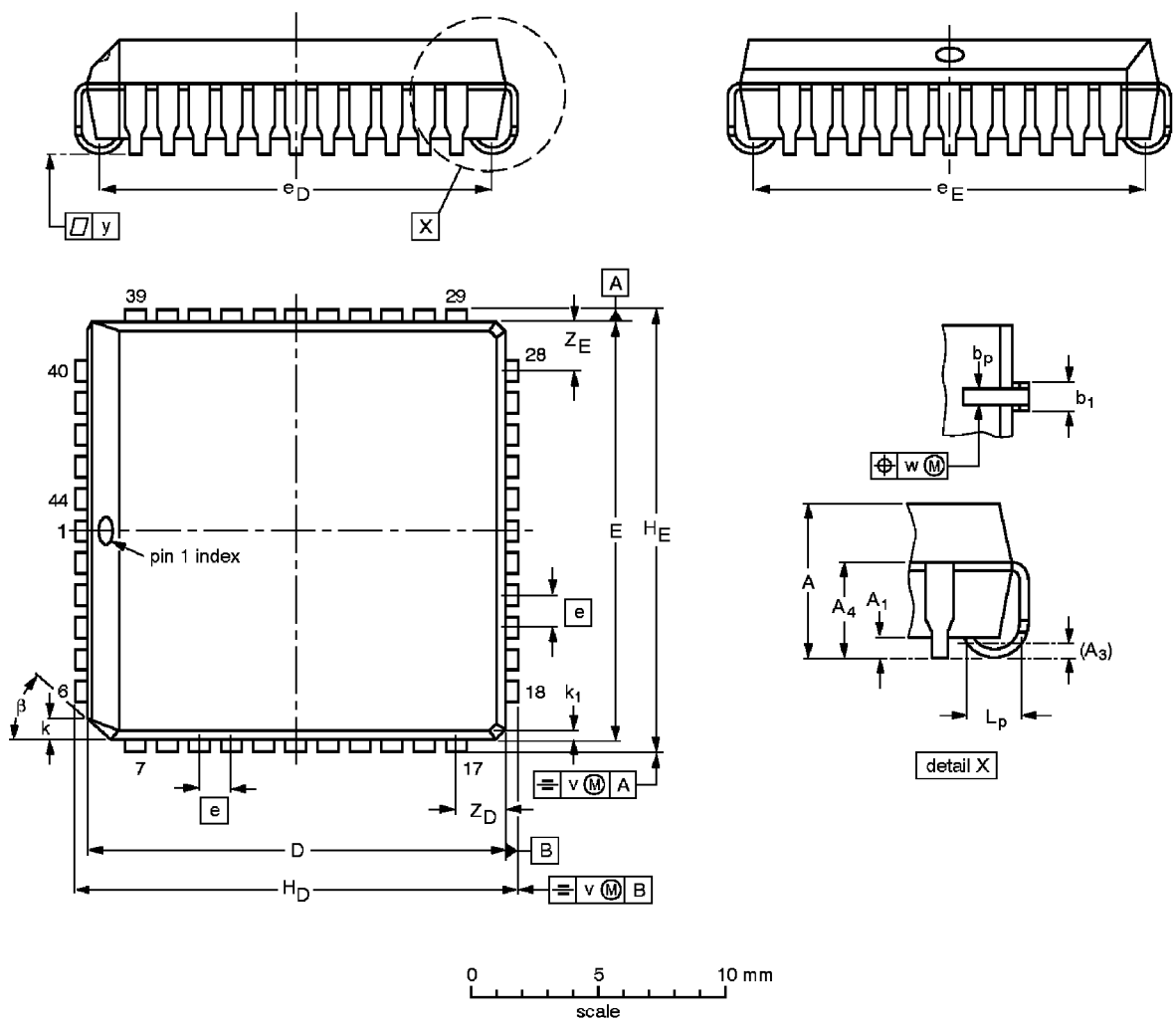


Figure 7. Average Effect of Airflow on Θ_{JA}

PLCC44: plastic leaded chip carrier; 44 leads SOT187-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

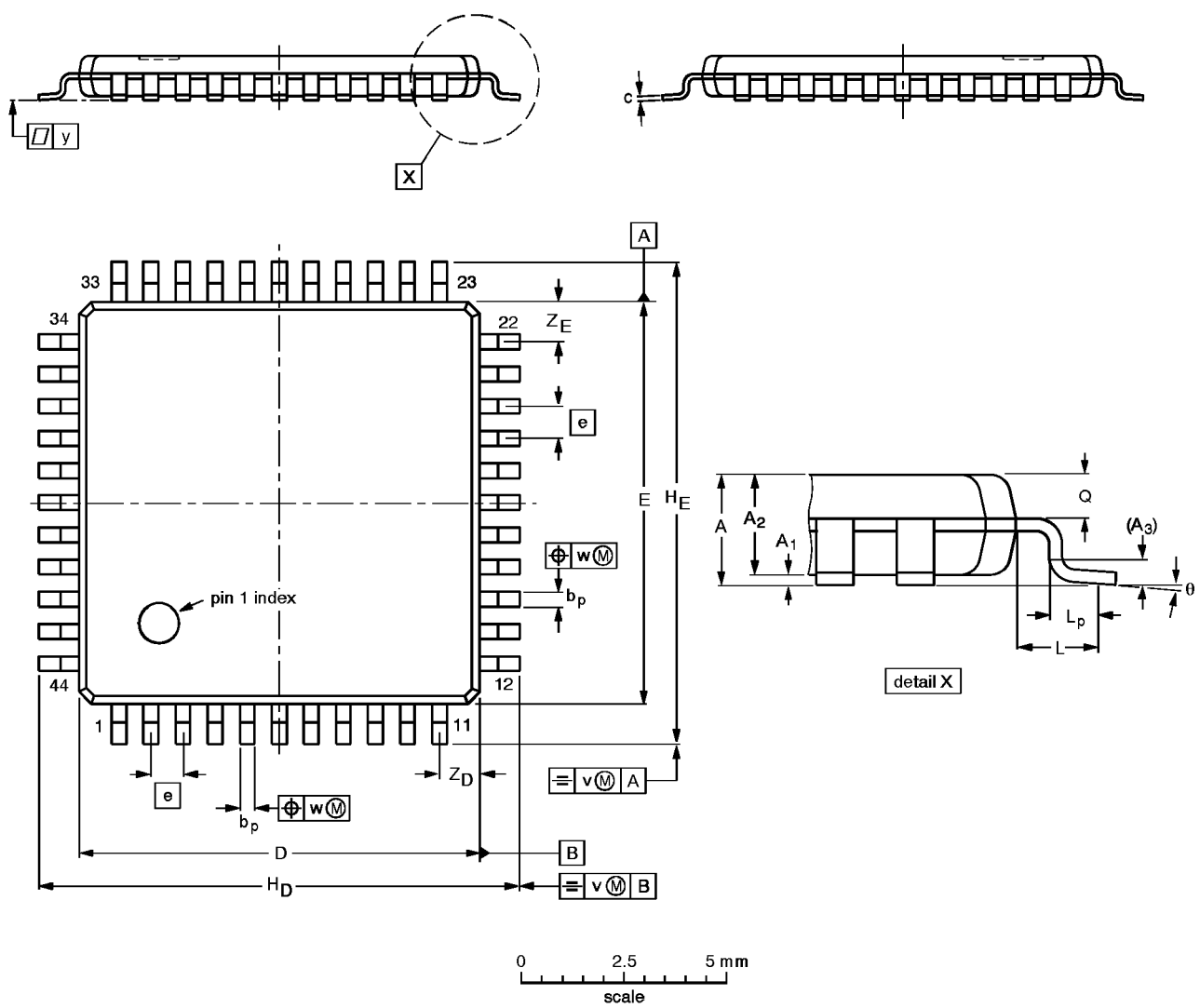
UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047AC				~~92-11-17~~ 95-02-25

TQFP44: plastic thin quad flat package; 44 leads; body 10 x 10 x 1.0 mm **SOT376-1**



DIMENSIONS (mm are the original dimensions)

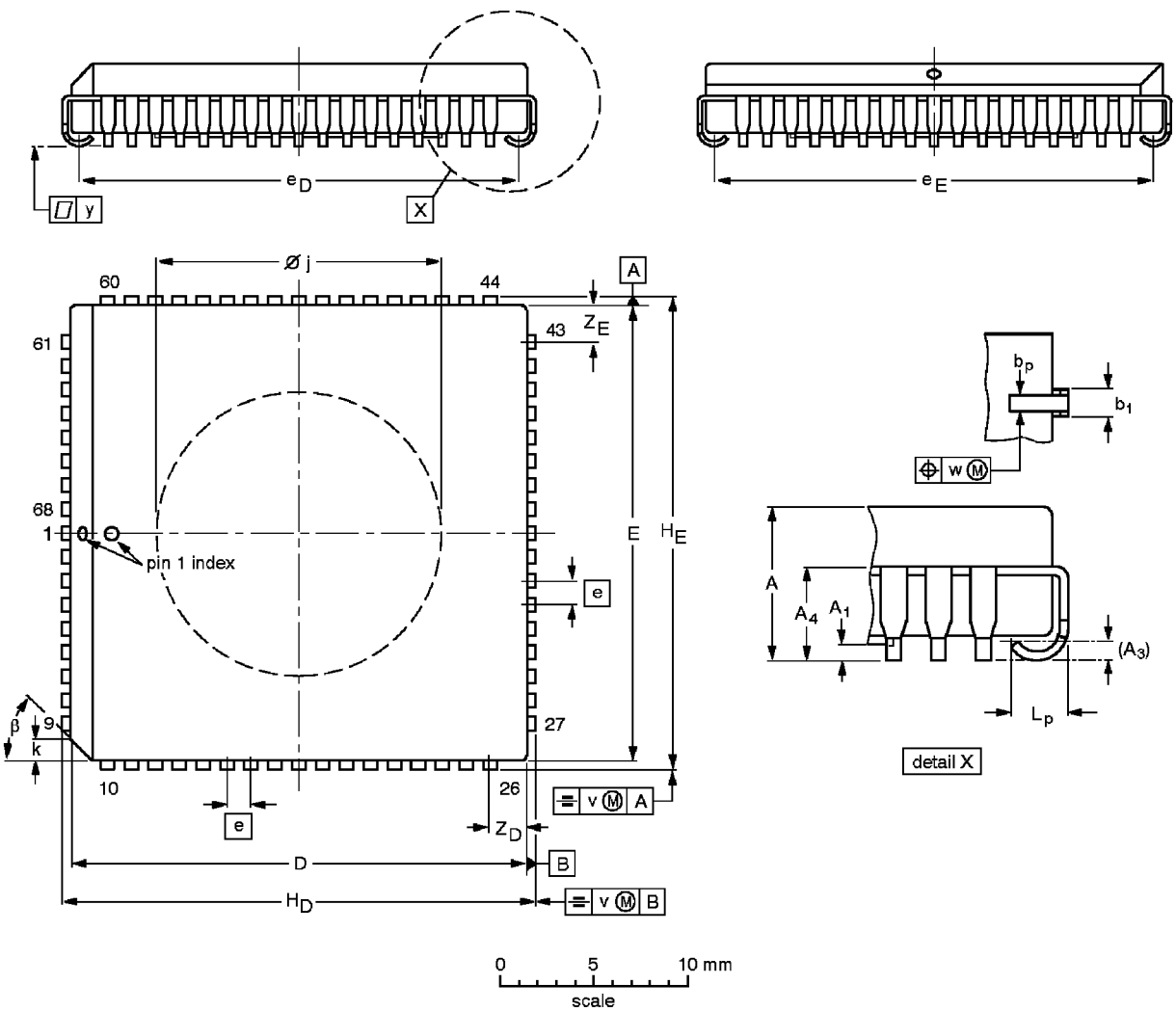
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.45 0.30	0.18 0.12	10.1 9.9	10.1 9.9	0.8	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.50 0.36	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT376-1						~~95-05-22~~ 96-04-02

PLCC68: plastic leaded chip carrier; 68 leads; pedestal SOT188-3



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

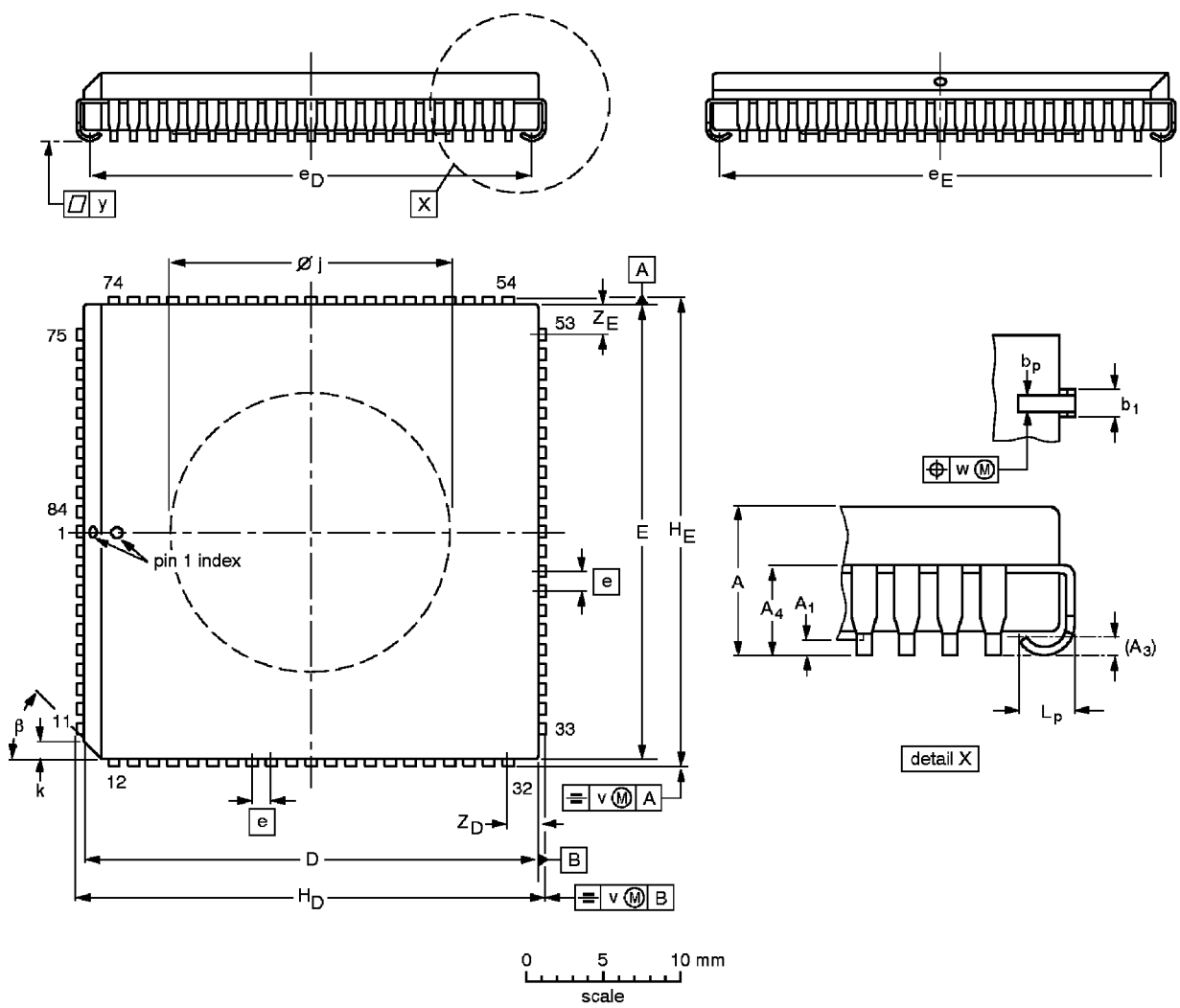
UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	$Ø_j$	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.13	0.25	3.05	0.53 0.33	0.81 0.66	24.33 24.13	24.33 24.13	1.27	23.62 22.61	23.62 22.61	25.27 25.02	25.27 25.02	1.22 1.07	15.34 15.19	1.44 1.02	0.18	0.18	0.10	2.06	2.06	45°
inches	0.180 0.165	0.005	0.01	0.12	0.021 0.013	0.032 0.026	0.958 0.950	0.958 0.950	0.05	0.930 0.890	0.930 0.890	0.995 0.985	0.995 0.985	0.048 0.042	0.604 0.598	0.057 0.040	0.007	0.007	0.004	0.081	0.081	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT188-3	112E10	MO-047AE				~~92-11-17~~ 95-02-25

PLCC84: plastic leaded chip carrier; 84 leads; pedestal SOT189-3



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

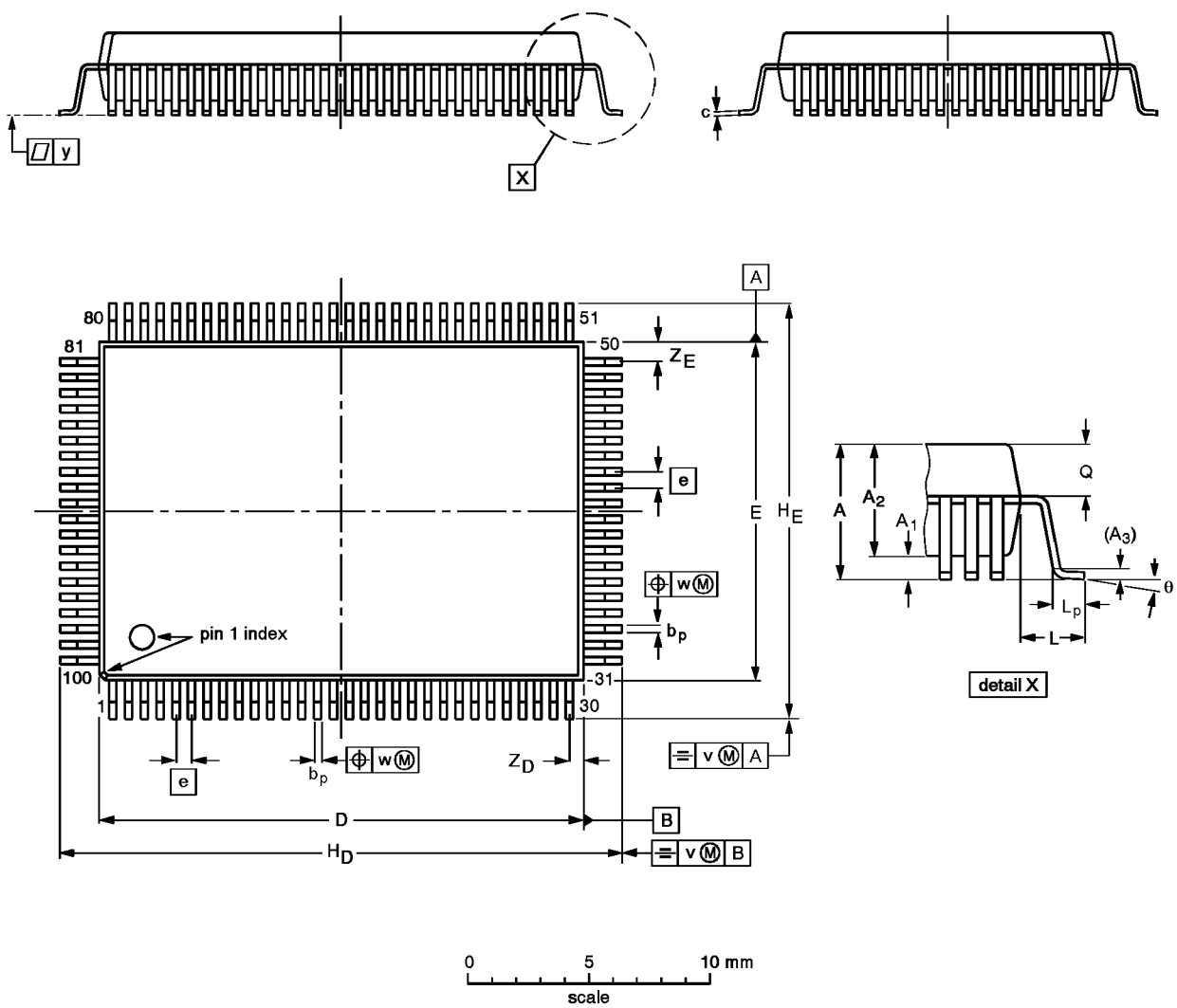
UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	Øj	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.13	0.25	3.05	0.53 0.33	0.81 0.66	29.41 29.21	29.41 29.21	1.27	28.70 27.69	28.70 27.69	30.35 30.10	30.35 30.10	1.22 1.07	15.34 15.19	1.44 1.02	0.18	0.18	0.10	2.06	2.06	45°
inches	0.180 0.165	0.005	0.01	0.12	0.021 0.013	0.032 0.026	1.158 1.150	1.158 1.150	0.05	1.130 1.090	1.130 1.090	1.195 1.185	1.195 1.185	0.048 0.042	0.057 0.040	0.057 0.040	0.007	0.007	0.004	0.081	0.081	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT189-3		MO-047AF				~~92-11-17~~ 95-02-25

QFP100: plastic quad flat package; 100 leads (lead length 1.6 mm); body 14 x 20 x 2.8 mm SOT382-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.40	0.60 0.25	3.05 2.55	0.25	0.38 0.22	0.23 0.13	20.1 19.1	14.1 13.9	0.65	23.45 22.95	17.45 16.95	1.60	1.03 0.73	1.4 1.2	0.20	0.12	0.10	0.68 0.45	0.68 0.45	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT382-1		MO-108CC-1				~~94-12-12~~ 95-02-04