FUJITSU
MICROELECTRONICS

MBM2716
MBM2716H
MBM2716-X

UV ERASABLE 16,384-BIT READ ONLY MEMORY

DESCRIPTION

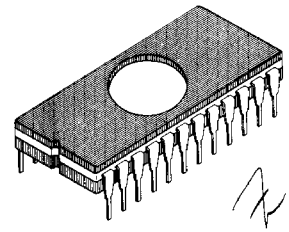
The Fujitsu MBM2716 is a high speed 16,384-bit static N-channel MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for applications where rapid turn-around and/or bit pattern experimentation are important.

A 24-pin dual in-line package with a transparent lid is used to package the MBM2716. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM2716 is fabricated using N-channel double polysilicon gate technology with single transitor stacked gate cells. It is organized as 2048 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.

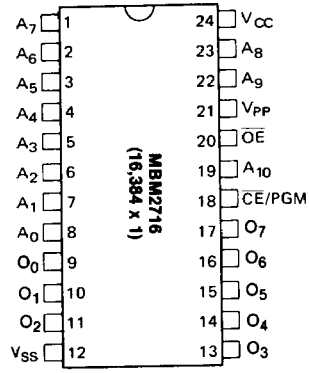
FEATURES

- **Organized as 2048 words by 8-bits, fully decoded**
- **Fast Access Time:**
  MBM2716 450ns Max.
  MBM2716H 350ns Max.
  MBM2716-X 450ns Max.
- **MBM2716-X: Extended temperature range**
  −40°C to +85°C
- **Fast programmming:**
  100 sec. for all 16,384 bits
- **Low power requirement:**
  525 mW Active
  132 mW Standby
- **No clocks required, fully static operation**
- **TTL compatible inputs and outputs**
- **Three-state output with OR-TIE capability**
- **Output Enable ($\overline{OE}$) pin for simplified memory expansion and bus control**
- **Single +5V Operation**
- **Standard 24-pin DIP package**
- **MBM2716/MBM2716H are compatible with Intel 2716**
- **MBM2716-X is compatible with Intel I2716**

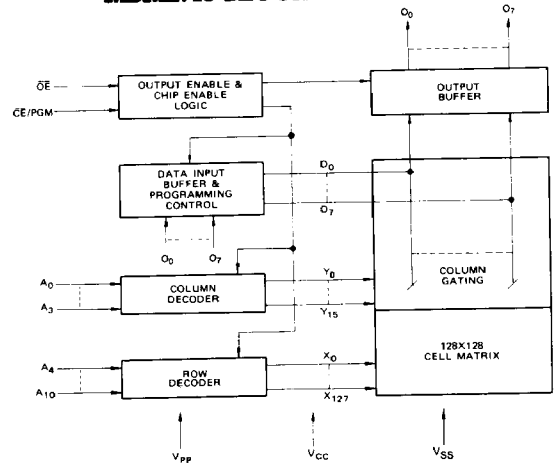


CERDIP PACKAGE
DIP-24C-C02

PIN ASSIGNMENT



MBM2716 BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see Note)

Rating		Symbol	Value	Unit
Temperature Under Bias	MBM2716/MBM2716H	T_A	−25 to +85	°C
	MBM2716-X		−50 to +95	°C
Storage Temperature		T_{stg}	−65 to +125	°C
Inputs/Outputs (Except V_{PP}) with Respect to V_{SS}		V_{IN}, V_{OUT}	−0.3 to +7	V
Program Input with Respect to V_{SS}		V_{PP}	−0.3 to +26.5	V
V_{CC} with Respect to V_{SS}		V_{CC}	−0.3 to +7	V
Power Dissipation		P_D	1.6	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS} = GND)

Parameter		Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage(1)	MBM2716 MBM2716-X	V_{CC}	4.75	5.0	5.25	V	MBM2716/MBM2716H 0°C to +70°C
	MBM2716H		4.5	5.0	5.5		
Supply Voltage		V_{SS}	—	GND	—	V	MBM2716-X −40°C to +85°C
V_{PP} Power Supply(2)		V_{PP}	0.0	5.0	V_{CC} +0.6	V	
Input High Voltage		V_{IH}	2.0	—	V_{CC} +1	V	
Input Low Voltage		V_{IL}	−0.1	—	0.8	V	

Note: (1) V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.
(2) During read operation, V_{PP} may be connected either to V_{CC} or V_{SS}.
When connected to V_{CC}, V_{CC} current would be the sum of I_{CC} and I_{PP1}.

FUNCTIONS AND PIN CONNECTIONS $V_{CC}(24)$ = +5V, $V_{SS}(12)$ = GND

Function (Pin No.) / Mode	Address Input (1 ~ 8, 19, 22, 23)	Data I/O (9 ~ 11, 13 ~ 17)	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} Supply (21)	I_{CC} Supply (24)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	+5	I_{CC2}
Output Disable	A_{IN}	High Z	V_{IL}	V_{IH}	+5	I_{CC2}
Stand By	Don't Care	High Z	V_{IH}	Don't Care	+5	I_{CC1}
Program	A_{IN}	D_{IN}	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	I_{CC2}
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	+25	I_{CC2}
Program Inhibit	Don't Care	High Z	V_{IL}	V_{IH}	+25	I_{CC2}

CAPACITANCE (T_A = 25°C; f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = OV)	C_{IN}	—	4	6	pF
Output Capacitance (V_{OUT} = OV)	C_{OUT}	—	8	12	pF

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.25V)	I_{LI}	—	—	10	μA
Output Leakage Current (V_{OUT} = 5.25V)	I_{LO}	—	—	10	μA
V_{PP} Supply Current (V_{PP} = 5.85V)	I_{PP1}	—	—	5	mA
V_{CC} Supply Current (Standby)	I_{CC1}	—	—	25	mA
V_{CC} Supply Current (Active)	I_{CC2}	—	—	100	mA
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}	—	—	0.45	V
Output High Voltage (I_{OH} = −400μA)	V_{OH}	2.4	—	—	V

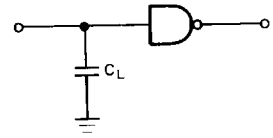
AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input Pulse Levels: 0.8V to 2.2V

Input Rise and Fall Time: ≤ 20nS

Timing Measurement Reference Levels: 1.0V and 2.0V for inputs
0.8V and 2.0V for outputs

Output Load: 1 TTL gate and C_L = 100pF

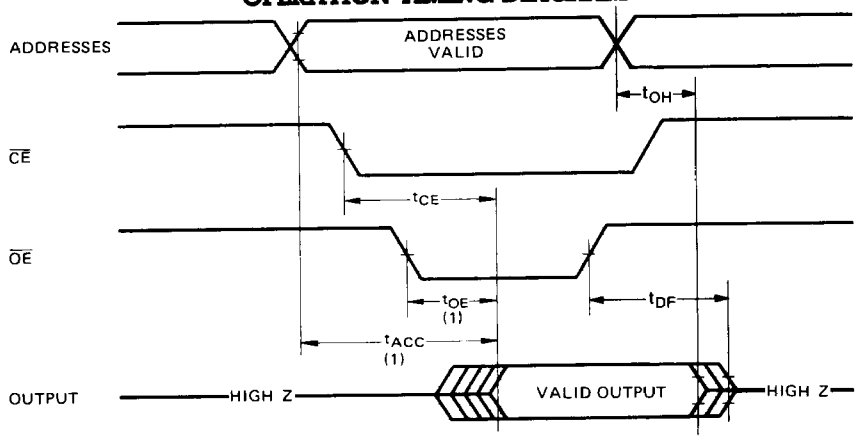


AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Parameter	Symbol	MBM2716		MBM2716H		MBM2716-X		Unit
		Min	Max	Min	Max	Min	Max	
Address Access Time	t_{ACC}	—	450	—	350	—	450	ns
Chip Enable to Output Delay	t_{CE}	—	450	—	350	—	450	ns
Output Enable to Output Delay	t_{OE}	—	120	—	120	—	150	ns
Address to Output Hold	t_{OH}	0	—	0	—	0	—	ns
Output Enable High to Output Float	t_{DF}	0	100	0	100	0	130	ns

OPERATION TIMING DIAGRAM



Note: (1) $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAMMING/ERASING INFORMATION

MEMORY CELL DESCRIPTION

The MBM2716 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and top select gate (see Fig. 14). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 15). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{THO}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 15.

Fig. 14 — MEMORY CELL

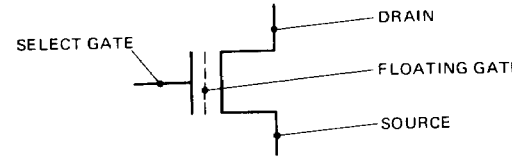
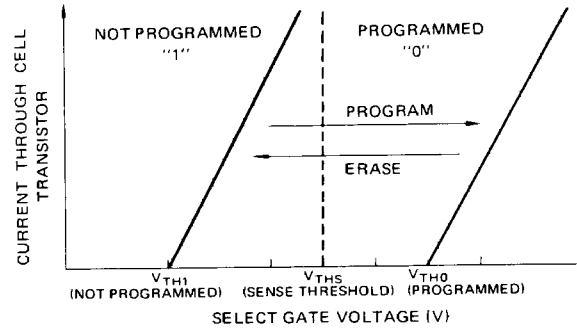


Fig. 15 — MEMORY CELL THRESHOLD SHIFT



PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM2716 has all 16,384 bits in the "1", or high, state. "O's" are loaded into the MBM2716 through the procedure of programming.

The programming mode is entered when +25V is applied to the V_{PP} pin and when $\overline{OE}$ is at V_{IH}. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data outputs pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50 msec, TTL High-level pulse is applied to the $\overline{CE}$/PGM input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{CE}$/PGM input is prohibited when programming.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the MBM2716 to an ultraviolet light source. A dosage of 15 W-seconds/cm^2 is required to completely erase an MBM2716. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000μW/cm^2 for 15 to 20 minutes. The MBM2716 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM2716 and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MBM2716, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMING INFORMATION (Continued)

DC CHARACTERISTICS

(T_A = 25°C, V_{CC}[1] = 5V ±5%, V_{PP}[1,2] = 25V ±1V, V_{SS} = 0V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Current (V_{IN} = 5.25V/0.45V)	I_{IL}	—	—	10	μA
V_{PP} Supply Current ($\overline{CE}$/PGM = V_{IL})	I_{PP1}	—	—	5	mA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$/PGM = V_H)	I_{PP2}	—	—	30	mA
V_{CC} Supply Current	I_{CC2}	—	—	100	mA
Input Low Level	V_{IL}	−0.1	—	0.8	V
Input High Level	V_{IL}	2.0	—	V_{CC} + 1	V

Note: (1) V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
(2) V_{PP} must not be greater than 26 volts including overshoot. Permanent device damage may occur if the device is taken out or put into a socket remaining V_{PP} = 25 volts. Also, during $\overline{OE}$ = $\overline{CE}$/PGM = V_{IH}, V_{PP} must not be switched from 5 volts to 25 volts or vise-versa.

AC CHARACTERISTICS

(T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2	—	—	μs
Output Enable Setup Time	t_{OES}	2	—	—	μs
Data Setup Time	t_{DS}	2	—	—	μs
Address Hold Time	t_{AH}	2	—	—	μs
Output Enable Hold Time	t_{OEH}	2	—	—	μs
Data Hold Time	t_{DH}	2	—	—	μs
Output Disable to Output Float Delay ($\overline{CE}$/PGM = V_{IL})	t_{DF}	0	—	120	ns
Output Enable to Output Delay ($\overline{CE}$/PGM = V_{IL})	t_{OE}	—	—	120	ns
Program Pulse Width	t_{PW}	45	50	55	ms
Program Rise Pulse Time	t_{PRT}	5	—	—	ns
Program Pulse Fall Time	t_{PFT}	5	—	—	ns

PROGRAMMING WAVEFORMS