CA3028A, CA3028B, CA3053

Differential/Cascode Amplifiers for Commercial and Industrial Equipment from DC to 120MHz

November 1996

Features

- **Controlled for Input Offset Voltage, Input Offset Current and Input Bias Current (CA3028 Series Only)**
- **Balanced Differential Amplifier Configuration with Controlled Constant Current Source**
- **Single-Ended and Dual-Ended Operation**

Applications

- **RF and IF Amplifiers (Differential or Cascode)**
- **DC, Audio and Sense Amplifiers**
- **Converter in the Commercial FM Band**
- **Oscillator**
- **Mixer**
- **Limiter**
- **Related Literature**
  - **Application Note AN5337 "Application of the CA3028 Integrated Circuit Amplifier in the HF and VHF Ranges." This note covers characteristics of different operating modes, noise performance, mixer, limiter, and amplifier design considerations**

Description

The CA3028A and CA3028B are differential/cascode amplifiers designed for use in communications and industrial equipment operating at frequencies from DC to 120MHz.

The CA3028B is like the CA3028A but is capable of premium performance particularly in critical DC and differential amplifier applications requiring tight controls for input offset voltage, input offset current, and input bias current.

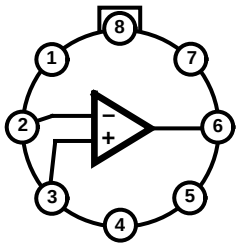
The CA3053 is similar to the CA3028A and CA3028B but is recommended for IF amplifier applications.

Ordering Information

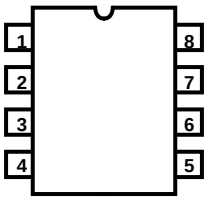
PART NUMBER (BRAND)	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
CA3028A	-55 to 125	8 Pin Metal Can	T8.C
CA3028AE	-55 to 125	8 Ld PDIP	E8.3
CA3028AM (3028A)	-55 to 125	8 Ld SOIC	M8.15
CA3028AM96 (3028A)	-55 to 125	8 Ld SOIC Tape and Reel	M8.15
CA3028B	-55 to 125	8 Pin Metal Can	T8.C
CA3028BE	-55 to 125	8 Ld PDIP	E8.3
CA3028BM (3028B)	-55 to 125	8 Ld SOIC	M8.15
CA3053	-55 to 125	8 Pin Metal Can	T8.C
CA3053E	-55 to 125	8 Ld PDIP	E8.3

Pinouts

CA3028A/B, CA3053 (METAL CAN)
TOP VIEW

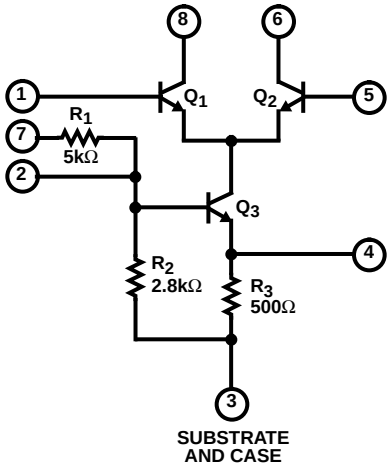


CA3028A/B, (PDIP, SOIC) CA3053 (PDIP)
TOP VIEW



Schematic Diagram

(Terminal Numbers Apply to All Packages)



File Number **382.3**

Operating Conditions

Temperature Range . . . . . -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Metal Can Package	225	140
PDIP Package	155	N/A
SOIC Package	185	N/A

Maximum Junction Temperature (Metal Can Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Absolute Maximum Voltage Ratings $T_A = 25°C$

The following chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of the horizontal Terminal 4 with respect to Terminal 2 is -1V to +5V.

TERM NO.	1	2	3	4	5	6	7	8
1		0 to -15 (Note 4)	0 to -15 (Note 4)	0 to -15 (Note 4)	+5 to -5	Note 3	Note 3	+20 to 0 (Note 5)
2			+5 to -11	+5 to -1	+15 to 0 (Note 6)	Note 3	+15 to 0 (Note 6)	Note 3
3 (Note 2)				+10 to 0	+15 to 0 (Note 6)	+30 to 0 (Note 7)	+15 to 0 (Note 6)	+30 to 0 (Note 7)
4					+15 to 0 (Note 6)	Note 3	Note 3	Note 3
5						+20 to 0 (Note 5)	Note 3	Note 3
6							Note 3	Note 3
7								Note 3
8								

Absolute Maximum Current Ratings

TERM NO.	I_{IN} mA	I_{OUT} mA
1	0.6	0.1
2	4	0.1
3	0.1	23
4	20	0.1
5	0.6	0.1
6	20	0.1
7	4	0.1
8	20	0.1

NOTES:

2. Terminal No. 3 is connected to the substrate and case.
3. Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe, if the specified voltage limits between all other terminals are not exceeded.
4. Limit is -12V for CA3053.
5. Limit is +15V for CA3053.
6. Limit is +12V for CA3053.
7. Limit is +24V for CA3028A and +18V for CA3053.

Electrical Specifications $T_A = 25°C$

PARAMETER	SYMBOL	TEST CONDITIONS	CA3028A			CA3028B			CA3053			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DC CHARACTERISTICS												
Input Offset Voltage (Figures 1, 14)	V_{IO}	V_{CC} = 6V, V_{EE} = -6V	-	-	-	-	0.98	5.0	-	-	-	mV
		V_{CC} = 12V, V_{EE} = -12V	-	-	-	-	0.89	5.0	-	-	-	mV
Input Offset Current (Figures 2, 14)	I_{IO}	V_{CC} = 6V, V_{EE} = -6V	-	-	-	-	0.56	5.0	-	-	-	µA
		V_{CC} = 12V, V_{EE} = -12V	-	-	-	-	1.06	6.0	-	-	-	µA
Input Bias Current (Figures 2, 3, 15, 16)	I_I	V_{CC} = 6V, V_{EE} = -6V	-	16.6	70	-	16.6	40	-	-	-	µA
		V_{CC} = 12V, V_{EE} = -12V	-	36	106	-	36	80	-	-	-	µA
		V_{CC} = 9V		-	-	-	-	-	-	29	85	µA
		V_{CC} = 12V	-	-	-	-	-	-	-	36	125	µA

Electrical Specifications $T_A = 25^oC$ **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		CA3028A			CA3028B			CA3053			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Operating Current (Figures 2, 3, 17, 18, 19)	I_6, I_8	V_{CC} = 6V, V_{EE} = -6V		0.8	1.25	2.0	1.0	1.25	1.5	-	-	-	mA
		V_{CC} = 12V, V_{EE} = -12V		2.0	3.3	5.0	2.5	3.3	4.0	-	-	-	mA
		V_{CC} = 9V		-	-	-	-	-	-	1.2	2.2	3.5	mA
		V_{CC} = 12V		-	-	-	-	-	-	2.0	3.3	5.0	mA
AGC Bias Current (Into Constant Current Source Terminal 7) (Figures 4, 20)	I_7	V_{CC} = 12V, V_{AGC} = 9V		-	1.28	-	-	1.28	-	-	-	-	mA
		V_{CC} = 12V, V_{AGC} = 12V		-	1.65	-	-	1.65	-	-	-	-	mA
		V_{CC} = 9V		-	-	-	-	-	-	-	1.15	-	mA
		V_{CC} = 12V		-	-	-	-	-	-	-	1.55	-	mA
Input Current (Terminal 7)	I_7	V_{CC} = 6V, V_{EE} = -6V		0.5	0.85	1.0	0.5	0.85	1.0	-	-	-	mA
		V_{CC} = 12V, V_{EE} = -12V		1.0	1.65	2.1	1.0	1.65	2.1	-	-	-	mA
Power Dissipation (Figures 2, 3, 21)	P_T	V_{CC} = 6V, V_{EE} = -6V		24	36	54	24	36	42	-	-	-	mW
		V_{CC} = 12V, V_{EE} = -12V		120	175	260	120	175	220	-	-	-	mW
		V_{CC} = 9V		-	-	-	-	-	-	-	50	80	mW
		V_{CC} = 12V		-	-	-	-	-	-	-	100	150	mW
DYNAMIC CHARACTERISTICS													
Power Gain (Figures 5, 6, 7, 22, 24, 26)	G_P	f = 100MHz, V_{CC} = 9V	Cascode	16	20	-	16	20	-	-	-	-	dB
			Diff. Amp.	14	17	-	14	17	-	-	-	-	dB
		f = 10.7MHz, V_{CC} = 9V	Cascode (Note 8)	35	39	-	35	39	-	35	39	-	dB
			Diff. Amp. (Note 8)	28	32	-	28	32	-	28	32	-	dB
Noise Figure (Figures 5, 6, 7, 23, 25, 26)	NF	f = 100MHz, V_{CC} = 9V	Cascode	-	7.2	9.0	-	7.2	9.0	-	-	-	dB
			Diff. Amp.	-	6.7	9.0	-	6.7	9.0	-	-	-	dB
Input Admittance (Figures 27, 28)	Y_{11}	f = 10.7MHz, V_{CC} = 9V	Cascode	-	0.6 + j1.6	-	-	0.6 + j1.6	-	-	0.6 + j1.6	-	mS
			Diff. Amp.	-	0.5 + j0.5	-	-	0.5 + j0.5	-	-	0.5 + j0.5	-	mS
Reverse Transfer Admittance (Figures 29, 30)	Y_{12}	f = 10.7MHz, V_{CC} = 9V	Cascode	-	0.0003 - j0	-	-	0.0003 - j0	-	-	0.0003 - j0	-	mS
			Diff. Amp.	-	0.01 - j0.0002	-	-	0.01 - j0.0002	-	-	0.01 - j0.0002	-	mS
Forward Transfer Admittance (Figures 31, 32)	Y_{21}	f = 10.7MHz, V_{CC} = 9V	Cascode	-	99 - j18	-	-	99 - j18	-	-	99 - j18	-	mS
			Diff. Amp.	-	-37 + j0.5	-	-	-37 + j0.5	-	-	-37 + j0.5	-	mS
Output Admittance (Figures 33, 34)	Y_{22}	f = 10.7MHz, V_{CC} = 9V	Cascode	-	0 + j0.08	-	-	0 + j0.08	-	-	0 + j0.08	-	mS
			Diff. Amp.	-	0.04 + j0.23	-	-	0.04 + j0.23	-	-	0.04 + j0.23	-	mS
Output Power (Untuned) (Figures 8, 35)	P_O	f = 10.7MHz, V_{CC} = 9V	Diff. Amp., 50Ω Input-Output	-	5.7	-	-	5.7	-	-	-	-	µW
AGC Range (Maximum Power Gain to Full Cut-off) (Figures 9, 36)	AGC	f = 10.7MHz, V_{CC} = 9V	Diff. Amp.	-	62	-	-	62	-	-	-	-	dB
Voltage Gain (Figures 10, 11, 37, 38)	A	f = 10.7MHz, V_{CC} = 9V, R_L = 1kΩ	Cascode	-	40	-	-	40	-	-	40	-	dB
			Diff. Amp.	-	30	-	-	30	-	-	30	-	dB
Differential Voltage Gain at f = 1kHz (Figure 12)	A	V_{CC} = 6V, V_{EE} = -6V, R_L = 2kΩ		-	-	-	35	38	42	-	-	-	dB
		V_{CC} = 12V, V_{EE} = -12V, R_L = 1.6kΩ		-	-	-	40	42.5	45	-	-	-	dB

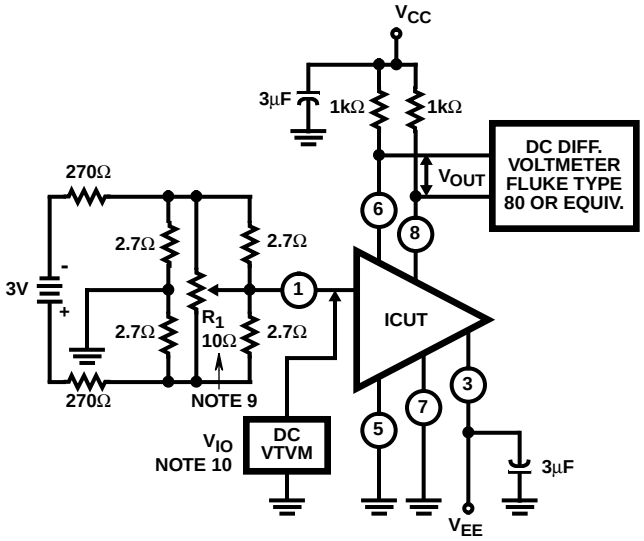
Electrical Specifications $T_A = 25^oC$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		CA3028A MIN	CA3028A TYP	CA3028A MAX	CA3028B MIN	CA3028B TYP	CA3028B MAX	CA3053 MIN	CA3053 TYP	CA3053 MAX	UNIT
Max Peak-to-Peak Output Voltage at f = 1kHz (Figure 12)	V_O(P-P)	V_{CC} = 6V, V_{EE} = -6V, R_L = 2kΩ		-	-	-	7.0	11.5	-	-	-	-	V_{P-P}
		V_{CC} = 12V, V_{EE} = -12V, R_L = 1.6kΩ		-	-	-	15	23	-	-	-	-	V_{P-P}
Bandwidth at -3dB Point (Figure 12)	BW	V_{CC} = 6V, V_{EE} = -6V, R_L = 2kΩ		-	-	-	-	7.3	-	-	-	-	MHz
		V_{CC} = 12V, V_{EE} = -12V, R_L = 1.6kΩ		-	-	-	-	8.0	-	-	-	-	MHz
Common Mode Input Voltage Range (Figure 13)	V_{CMR}	V_{CC} = 6V, V_{EE} = -6V		-	-	-	-2.5	-3.2 to -4.5	4	-	-	-	V
		V_{CC} = 12V, V_{EE} = -12V		-	-	-	-5.0	-7 to -9	7	-	-	-	V
Common Mode Rejection Ratio (Figure 13)	CMRR	V_{CC} = 6V, V_{EE} = -6V		-	-	-	60	110	-	-	-	-	dB
		V_{CC} = 12V, V_{EE} = -12V		-	-	-	60	90	-	-	-	-	dB
Input Impedance at f = 1kHz	Z_{IN}	V_{CC} = 6V, V_{EE} = -6V		-	-	-	-	5.5	-	-	-	-	kΩ
		V_{CC} = 12V, V_{EE} = -12V		-	-	-	-	3.0	-	-	-	-	kΩ
Peak-to-Peak Output Current	I_{P-P}	f = 10.7MHz, e_{IN} = 400mV, Diff. Amp.	V_{CC} = 9V	2.0	4.0	7.0	2.5	4.0	6.0	2.0	4.0	7.0	mA
			V_{CC} = 12V	3.5	6.0	10	4.5	6.0	8.0	3.5	6.0	10	mA

NOTE:

8. Does not apply to CA3053.

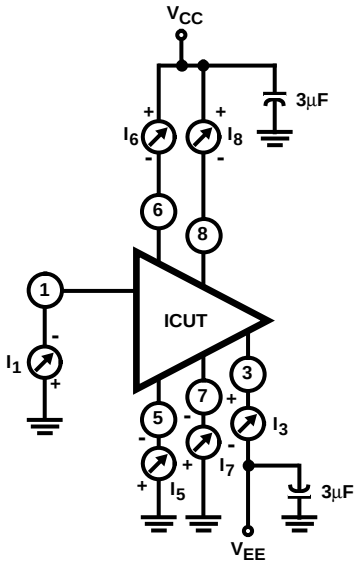
Test Circuits



NOTES:

9. Adjust R_1 for V_{OUT} = 0V ±0.1V.
10. Record Input Offset Voltage.

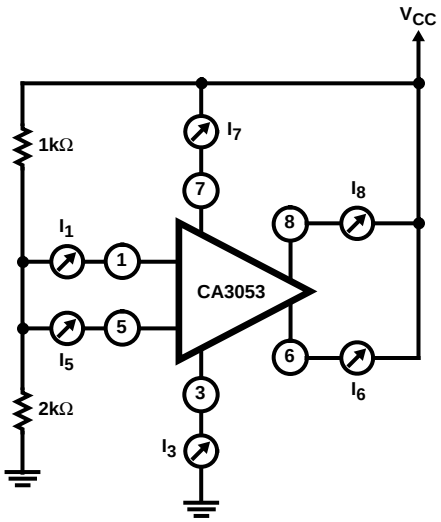
FIGURE 1. INPUT OFFSET VOLTAGE TEST CIRCUIT FOR CA3028B



NOTE: Power Dissipation = $I_3V_{EE} + (I_6 + I_8)V_{CC}$.

FIGURE 2. INPUT OFFSET CURRENT, INPUT BIAS CURRENT, POWER DISSIPATION, AND QUIESCENT OPERATING CURRENT TEST CIRCUIT FOR CA3028A AND CA3028B

Test Circuits (Continued)



NOTE: Power Dissipation = $V_{CC}I_3$.

FIGURE 3. INPUT BIAS CURRENT, POWER DISSIPATION AND QUIESCENT OPERATING CURRENT TEST CIRCUIT FOR CA3053

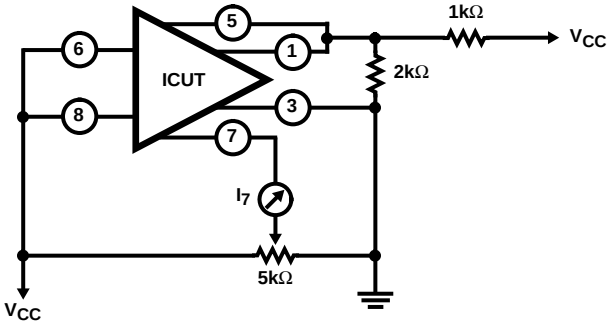
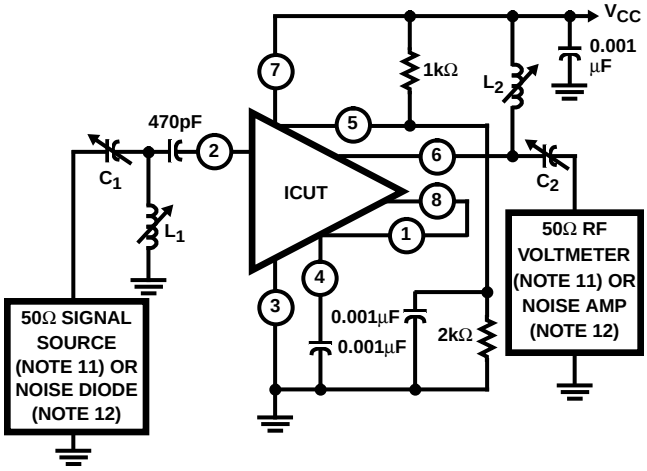


FIGURE 4. AGC BIAS CURRENT TEST CIRCUIT (DIFFERENTIAL AMPLIFIER CONFIGURATION) FOR CA3028A AND CA3028B

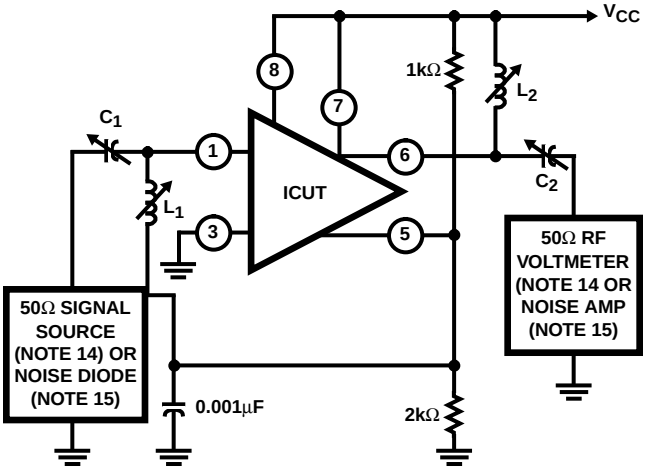


f (MHz)	C_1 (pF)	C_2 (pF)	L_1 (μH)	L_2 (μH)
10.7	20 - 60	20 - 60	3 - 5	3 - 5
100	3 - 30	3 - 30	0.1 - 0.25	0.15 - 0.3

NOTES:

11. For Power Gain Test.
12. For Noise Figure Test.
13. 10.7MHz Power Gain Test Only.

FIGURE 5. POWER GAIN AND NOISE FIGURE TEST CIRCUIT (CASCODE CONFIGURATION) FOR CA3028A, CA3028B AND CA3053 (NOTE 3)



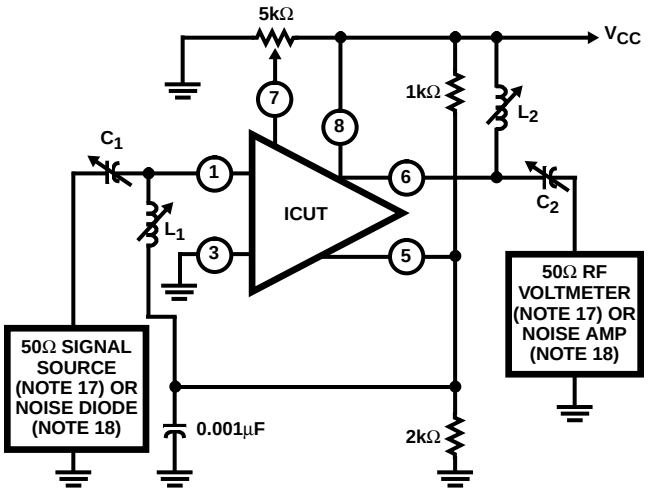
f (MHz)	C_1 (pF)	C_2 (pF)	L_1 (μH)	L_2 (μH)
10.7	30 - 60	20 - 50	3 - 6	3 - 6
100	2 - 15	2 - 15	0.2 - 0.5	0.2 - 0.5

NOTES:

14. For Power Gain Test.
15. For Noise Figure Test.
16. 10.7MHz Power Gain Test Only.

FIGURE 6. POWER GAIN AND NOISE FIGURE TEST CIRCUIT (DIFFERENTIAL AMPLIFIER CONFIGURATION AND TERMINAL 7 CONNECTED TO VCC) FOR CA3028A, CA3028B AND CA3053 (NOTE 3)

Test Circuits (Continued)



f (MHz)	C_1 (pF)	C_2 (pF)	L_1 (μH)	L_2 (μH)
10.7	30 - 60	20 - 50	3 - 6	3 - 6
100	2 - 15	2 - 15	0.2 - 0.5	0.2 - 0.5

NOTES:

17. For Power Gain Test.
18. For Noise Figure Test.

FIGURE 7. POWER GAIN AND NOISE FIGURE TEST CIRCUIT (DIFFERENTIAL AMPLIFIER CONFIGURATION) FOR CA3028A AND CA3028B

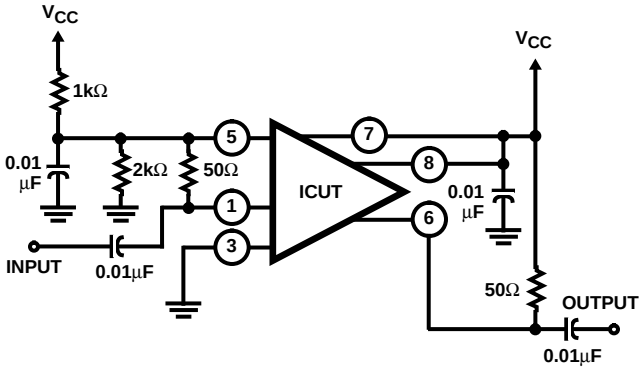
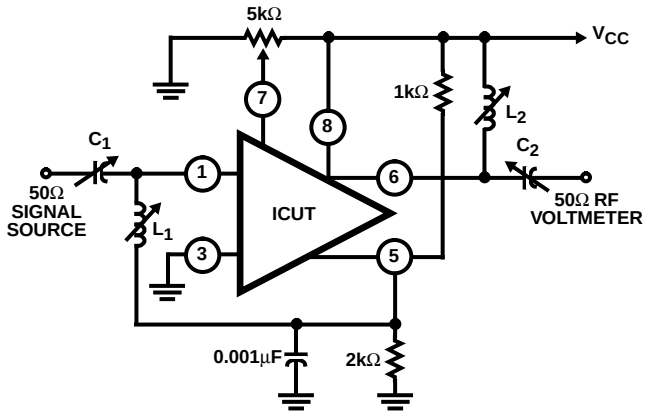


FIGURE 8. OUTPUT POWER TEST CIRCUIT FOR CA3028A AND CA3028B



f (MHz)	C_1 (pF)	C_2 (pF)	L_1 (μH)	L_2 (μH)
10.7	30 - 60	20 - 50	3 - 6	3 - 6
100	2 - 15	2 - 15	0.2 - 0.5	0.2 - 0.5

FIGURE 9. AGC RANGE TEST CIRCUIT (DIFFERENTIAL AMPLIFIER) FOR CA3028A AND CA3028B

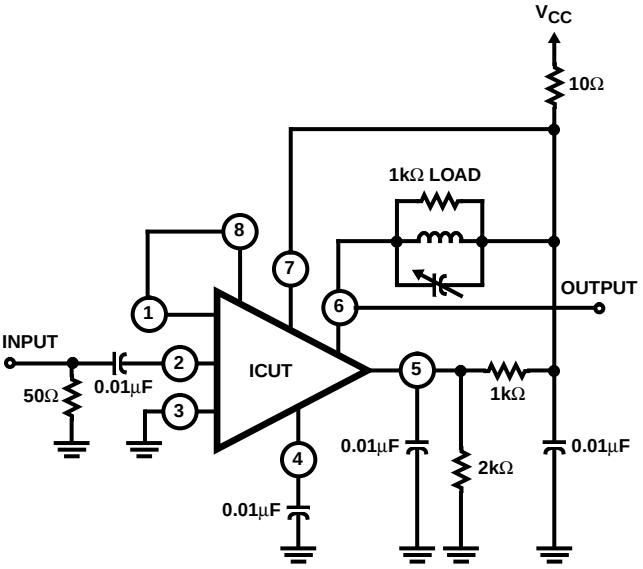


FIGURE 10. TRANSFER CHARACTERISTIC (VOLTAGE GAIN) TEST CIRCUIT (10.7MHz) CASCODE CONFIGURATION FOR CA3028A, CA3028B AND CA3053

Test Circuits (Continued)

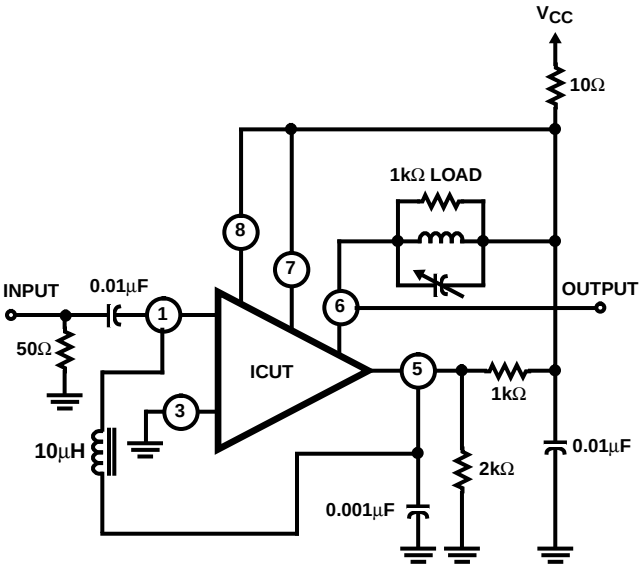
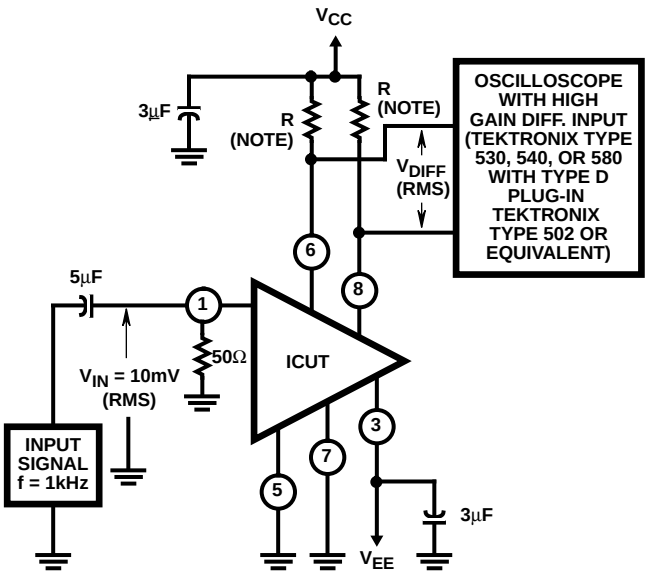
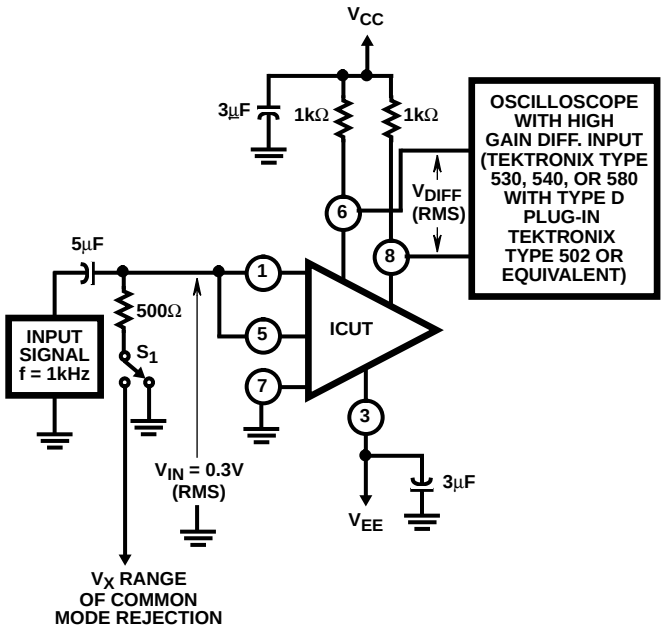


FIGURE 11. TRANSFER CHARACTERISTIC (VOLTAGE GAIN) TEST CIRCUIT (10.7MHz) DIFFERENTIAL AMPLIFIER CONFIGURATION FOR CA3028A, CA3028B AND CA3053



NOTE: For R = 1.6kΩ: V_{CC} = 12V, V_{EE} = -12V
For R = 2.0kΩ: V_{CC} = 6V, V_{EE} = -6V.

FIGURE 12. DIFFERENTIAL VOLTAGE GAIN, MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AND BANDWIDTH TEST CIRCUIT FOR CA3028B



NOTES:

19. For CMR test: S_1 to GND.

20. For Input Common Mode Voltage Range Test: S_1 to V_X.

21. Common Mode Rejection Ratio $= 20\log_{10}\frac{(A)(2)(0.3)}{V_{DIFF}(RMS)}$

A = Single-Ended Voltage Gain.

FIGURE 13. COMMON MODE REJECTION RATIO AND COMMON MODE INPUT VOLTAGE RANGE TEST CIRCUIT FOR CA3028B

Typical Performance Curves

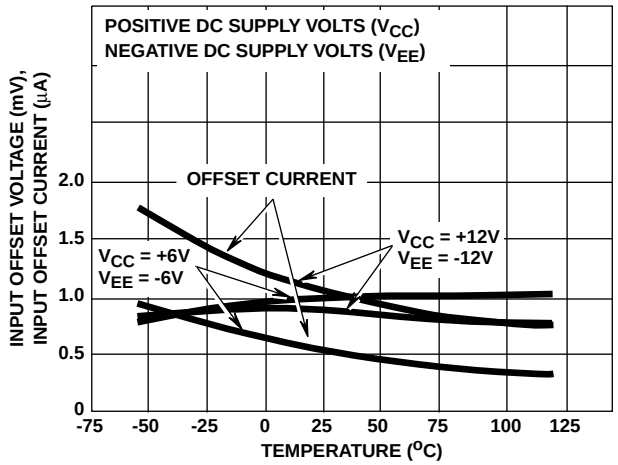


FIGURE 14. INPUT OFFSET VOLTAGE AND INPUT OFFSET CURRENT FOR CA3028B vs TEMPERATURE

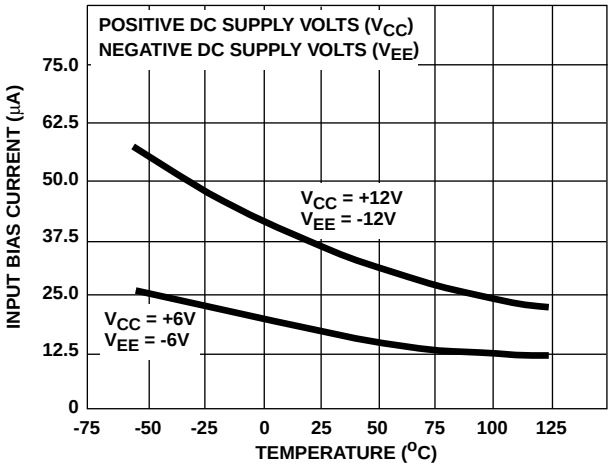


FIGURE 15. INPUT BIAS CURRENT vs TEMPERATURE FOR CA3028A AND CA3028B

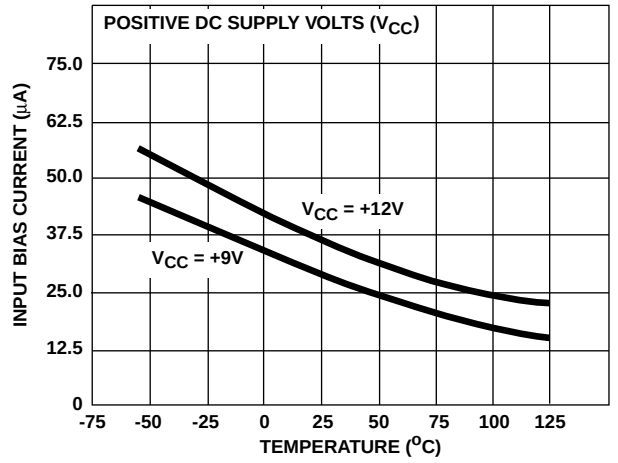


FIGURE 16. INPUT BIAS CURRENT vs TEMPERATURE FOR CA3053

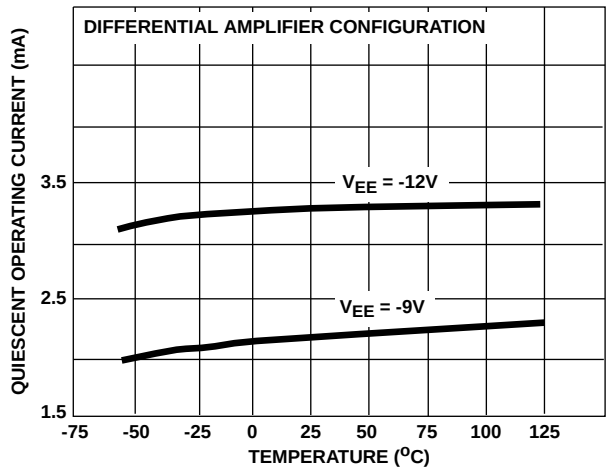


FIGURE 17. QUIESCENT OPERATING CURRENT vs TEMPERATURE FOR CA3028A AND CA3028B

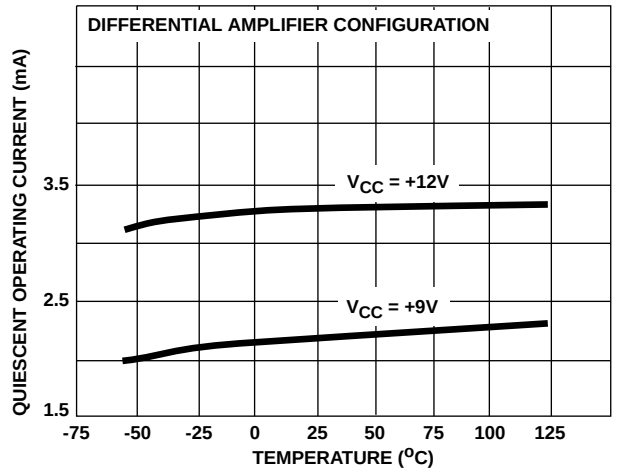


FIGURE 18. QUIESCENT OPERATING CURRENT vs TEMPERATURE FOR CA3053

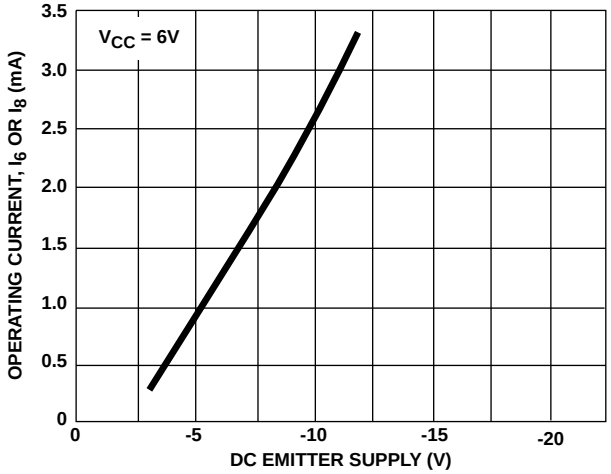


FIGURE 19. OPERATING CURRENT vs V_{EE} VOLTAGE FOR CA3028A AND CA3028B

Typical Performance Curves (Continued)

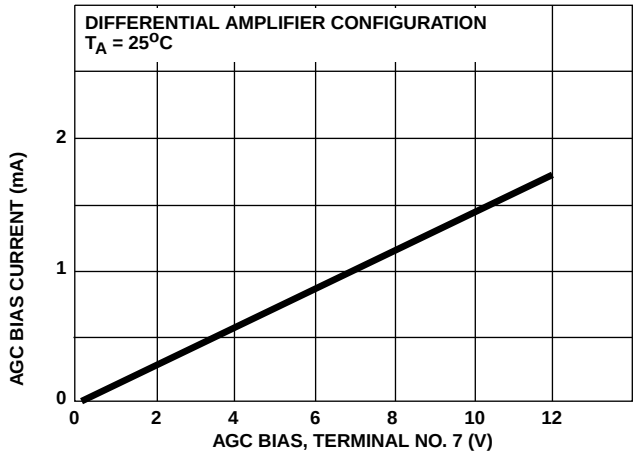


FIGURE 20. AGC BIAS CURRENT vs BIAS VOLTAGE (TERMINAL 7) FOR CA3028A AND CA3028B

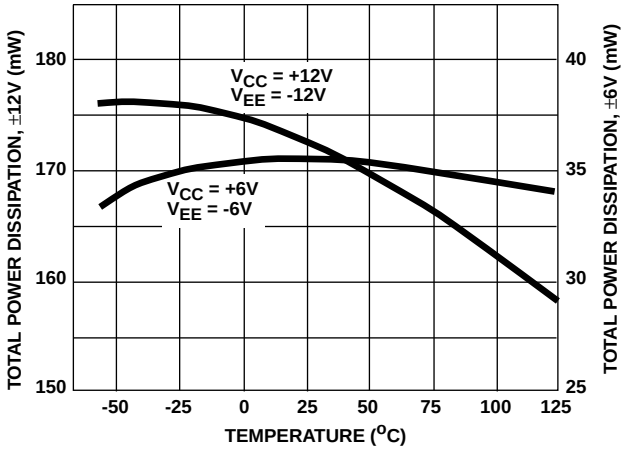


FIGURE 21. POWER DISSIPATION vs TEMPERATURE FOR CA3028A AND CA3028B

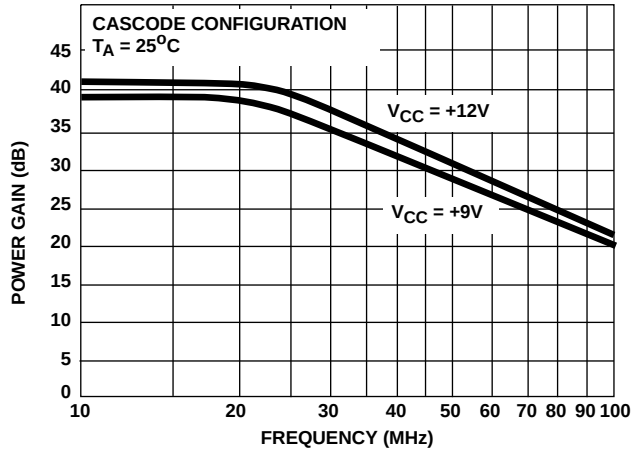


FIGURE 22. POWER GAIN vs FREQUENCY (CASCODE CONFIGURATION) FOR CA3028A AND CA3028B

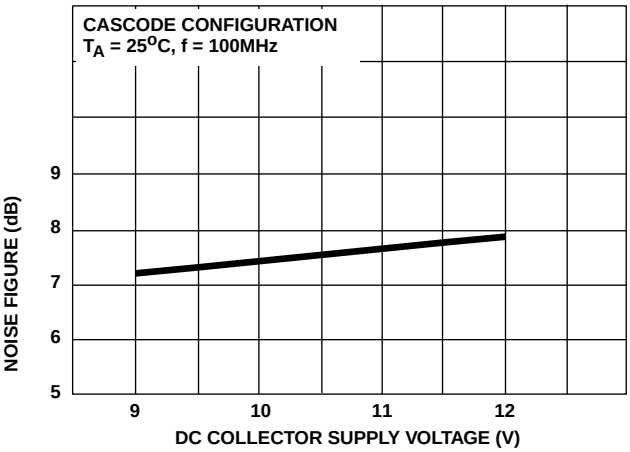


FIGURE 23. 100MHz NOISE FIGURE vs COLLECTOR SUPPLY VOLTAGE (CASCODE CONFIGURATION) FOR CA3028A AND CA3028B

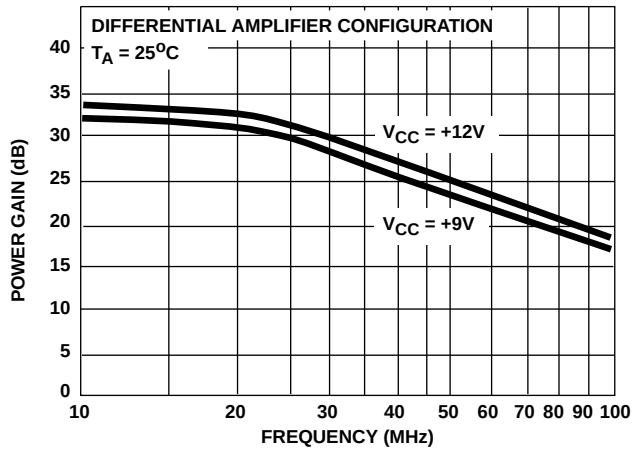


FIGURE 24. POWER GAIN vs FREQUENCY (DIFFERENTIAL AMPLIFIER CONFIGURATION) FOR CA3028A AND CA3028B

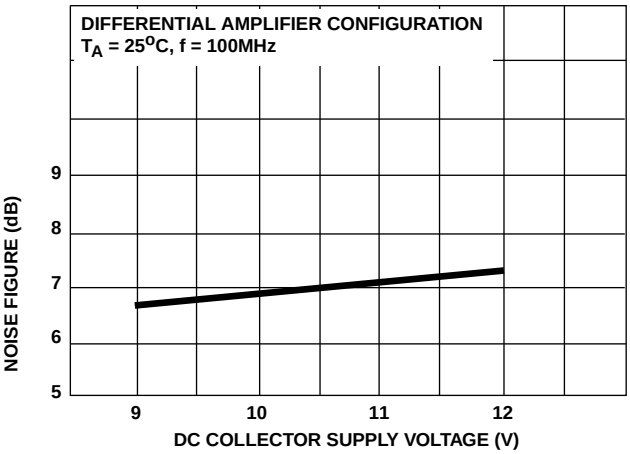


FIGURE 25. 100MHz NOISE FIGURE vs COLLECTOR SUPPLY VOLTAGE (DIFFERENTIAL AMPLIFIER CONFIGURATION) FOR CA3028A AND CA3028B

Typical Performance Curves (Continued)

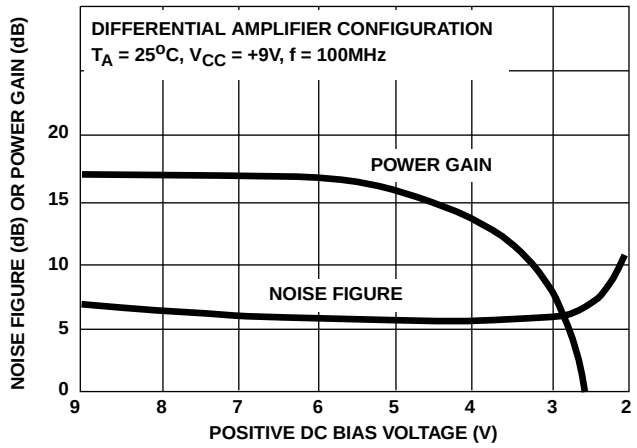


FIGURE 26. 100MHz NOISE FIGURE AND POWER GAIN vs BASE-TO-EMITTER BIAS VOLTAGE (TERMINAL 7) FOR CA3028A AND CA3028B

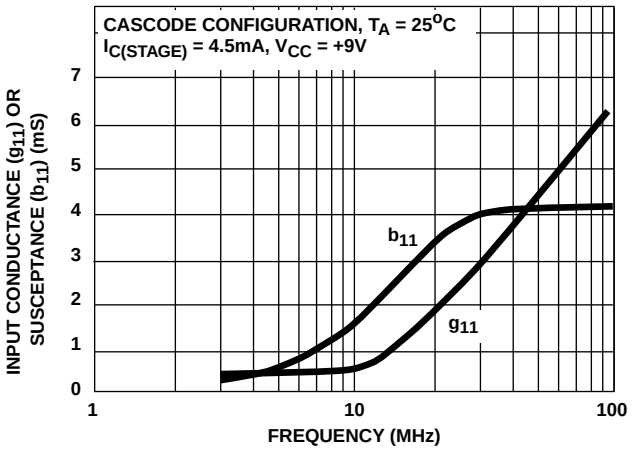


FIGURE 27. INPUT ADMITTANCE (Y_{11}) vs FREQUENCY (CASCODE CONFIGURATION)

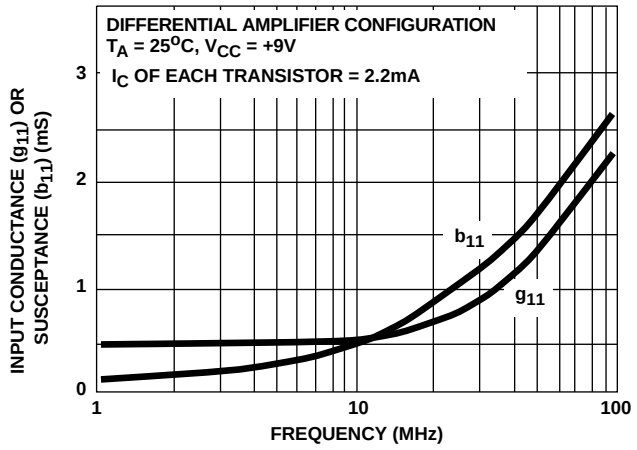


FIGURE 28. INPUT ADMITTANCE (Y_{11}) vs FREQUENCY (DIFFERENTIAL AMPLIFIER CONFIGURATION)

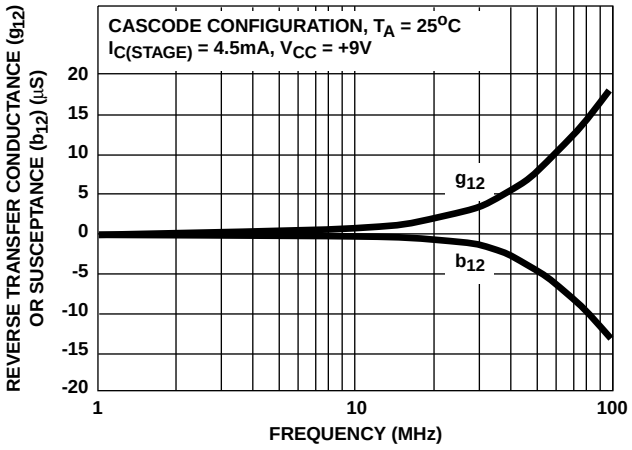


FIGURE 29. REVERSE TRANSADMITTANCE (Y_{12}) vs FREQUENCY (CASCODE CONFIGURATION)

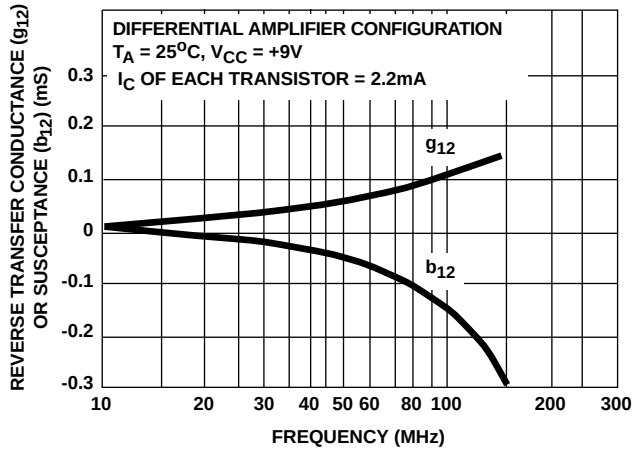


FIGURE 30. REVERSE TRANSADMITTANCE (Y_{12}) vs FREQUENCY (DIFFERENTIAL AMPLIFIER CONFIGURATION)

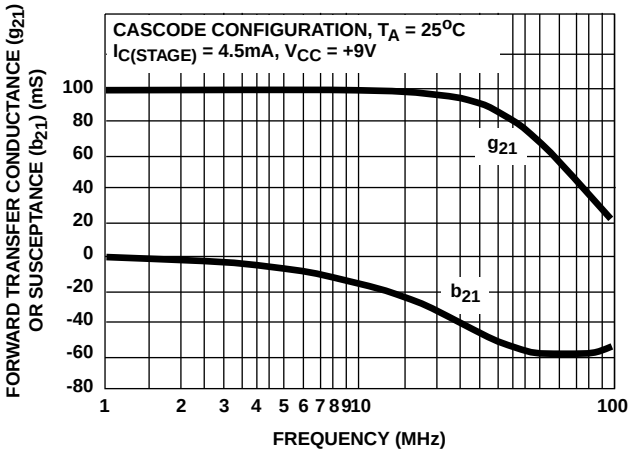


FIGURE 31. FORWARD TRANSADMITTANCE (Y_{21}) vs FREQUENCY (CASCODE CONFIGURATION)

Typical Performance Curves (Continued)

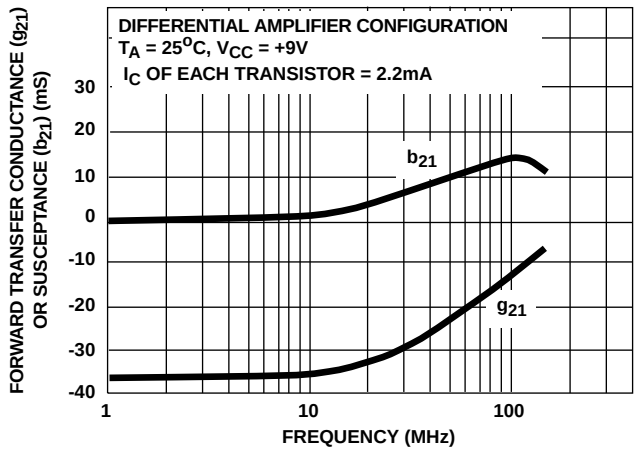


FIGURE 32. FORWARD TRANSADMITTANCE (Y_{21}) vs FREQUENCY (DIFFERENTIAL AMPLIFIER CONFIGURATION)

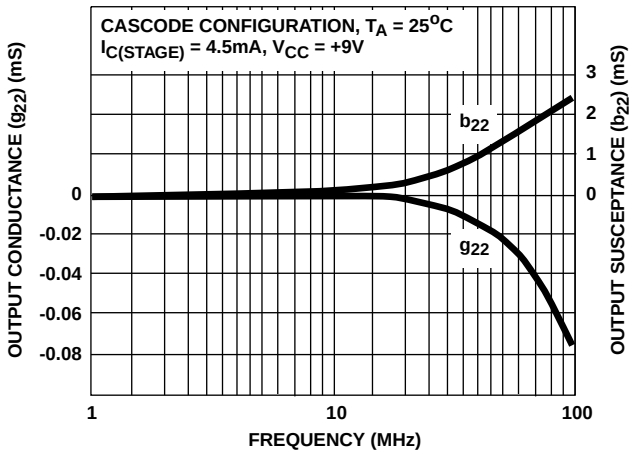


FIGURE 33. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY (CASCODE CONFIGURATION)

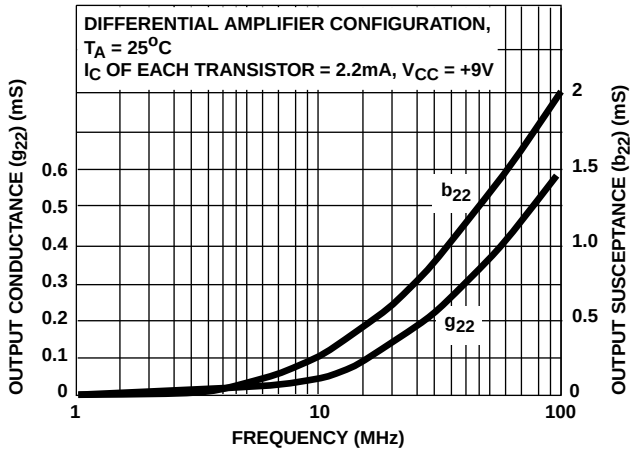


FIGURE 34. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY (DIFFERENTIAL AMPLIFIER CONFIGURATION)

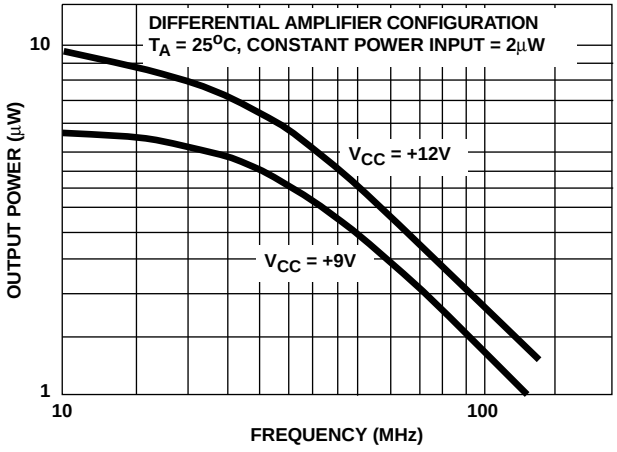


FIGURE 35. OUTPUT POWER vs FREQUENCY - 50Ω INPUT AND 50Ω OUTPUT (DIFFERENTIAL AMPLIFIER CONFIGURATION) FOR CA3028A AND CA3028B

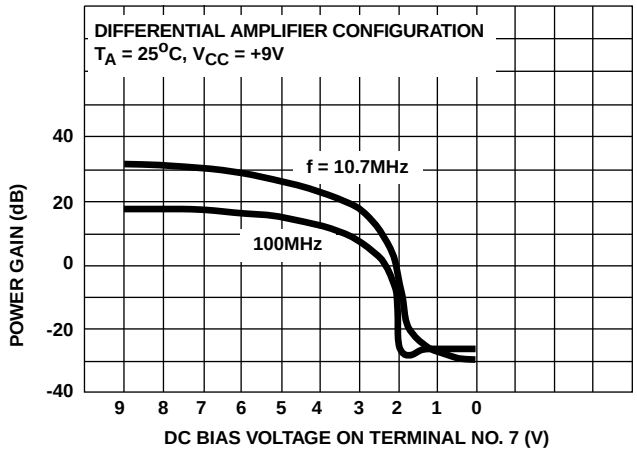


FIGURE 36. AGC CHARACTERISTICS FOR CA3028A AND CA3028B

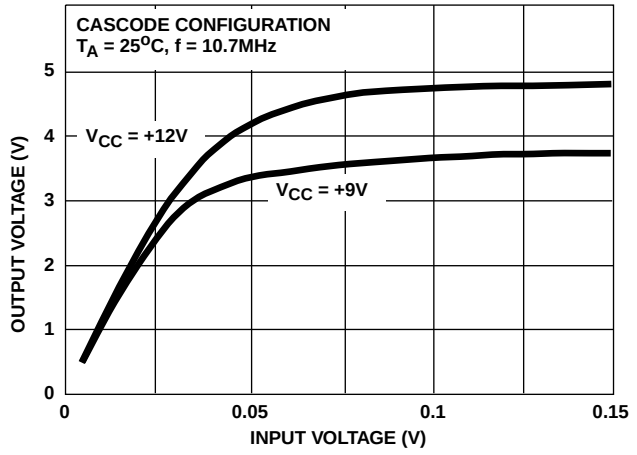


FIGURE 37. TRANSFER CHARACTERISTICS (CASCODE CONFIGURATION)

Typical Performance Curves (Continued)

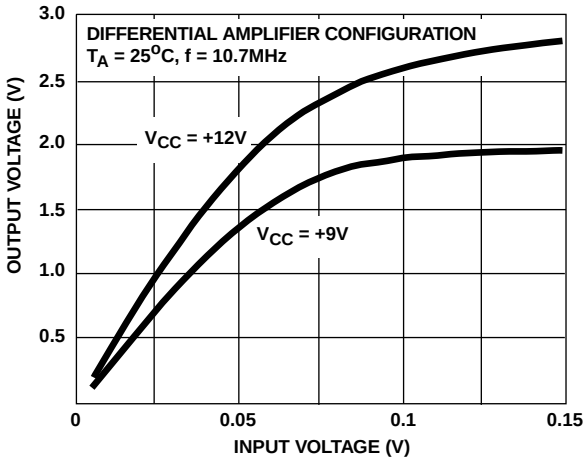


FIGURE 38. TRANSFER CHARACTERISTICS (DIFFERENTIAL AMPLIFIER CONFIGURATION)

Glossary of Terms

AGC Bias Current

The current drawn by the device from the AGC voltage source, at maximum AGC voltage.

AGC Range

The total change in voltage gain (from maximum gain to complete cutoff) which may be achieved by application of the specified range of dc voltage to the AGC input terminal of the device.

Common Mode Rejection Ratio

The ratio of the full differential voltage gain to the common mode voltage gain.

Power Dissipation

The total power drain of the device with no signal applied and no external load current.

Input Bias Current

The average value (one half the sum) of the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Input Offset Current

The difference in the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Input Offset Voltage

The difference in the DC voltages which must be applied to the input terminals to obtain equal quiescent operating voltages (zero output offset voltage) at the output terminals.

Noise Figure

The ratio of the total noise power of the device and a resistive signal source to the noise power of the signal source alone, the signal source representing a generator of zero impedance in series with the source resistance.

Power Gain

The ratio of the signal power developed at the output of the device to the signal power applied to the input, expressed in dB.

Quiescent Operating Current

The average (DC) value of the current in either output terminal.

Voltage Gain

The ratio of the change in output voltage at either output terminal with respect to ground, to a change in input voltage at either input terminal with respect to ground, with the other input terminal at AC ground.