

OKI Semiconductor

MD56V62400/H

4-Bank × 4,194,304-Word × 4-Bit SYNCHRONOUS DYNAMIC RAM

DESCRIPTION

The MD56V62400/H is a 4-bank × 4,194,304-word × 4-bit synchronous dynamic RAM, fabricated in Oki's CMOS silicon-gate process technology. The device operates at 3.3 V. The inputs and outputs are LVTTTL compatible.

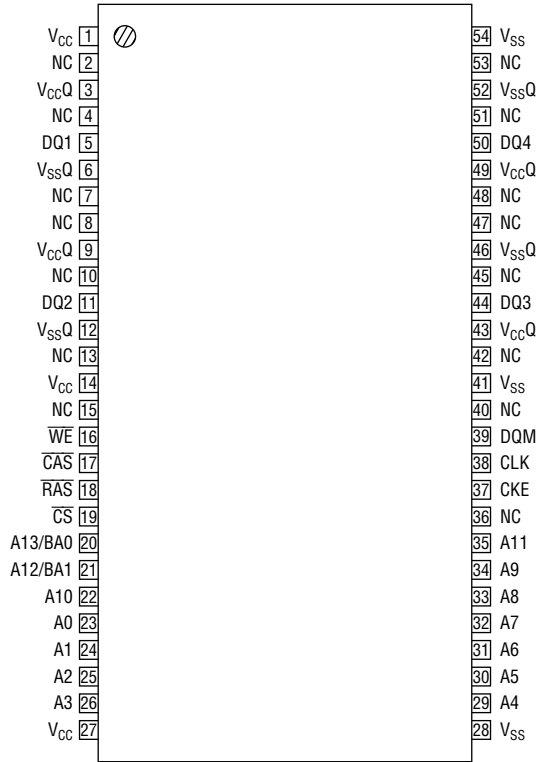
FEATURES

- Silicon gate, quadruple polysilicon CMOS, 1-transistor memory cell
- 4-bank × 4,194,304-word × 4-bit configuration
- 3.3 V power supply, ±0.3 V tolerance
- Input : LVTTTL compatible
- Output : LVTTTL compatible
- Refresh : 4096 cycles/64 ms
- Programmable data transfer mode
 - $\overline{\text{CAS}}$ latency (2, 3)
 - Burst length (2, 4, 8)
 - Data scramble (sequential, interleave)
- CBR auto-refresh, Self-refresh capability
- Package:
 - 54-pin 400 mil plastic TSOP (Type II) (TSOPII54-P-400-0.80-K) (Product : MD56V62400/H-xxTA)
 - xx indicates speed rank.

PRODUCT FAMILY

| Family | Max. Frequency | Access Time (Max.) | |
|----------------|----------------|--------------------|------------------|
| | | t _{AC2} | t _{AC3} |
| MD56V62400-10 | 100 MHz | 9 ns | 9 ns |
| MD56V62400-12 | 83 MHz | 14 ns | 10 ns |
| MD56V62400H-15 | 66 MHz | 9 ns | 9 ns |

PIN CONFIGURATION (TOP VIEW)



54-Pin Plastic TSOP (II)
(K Type)

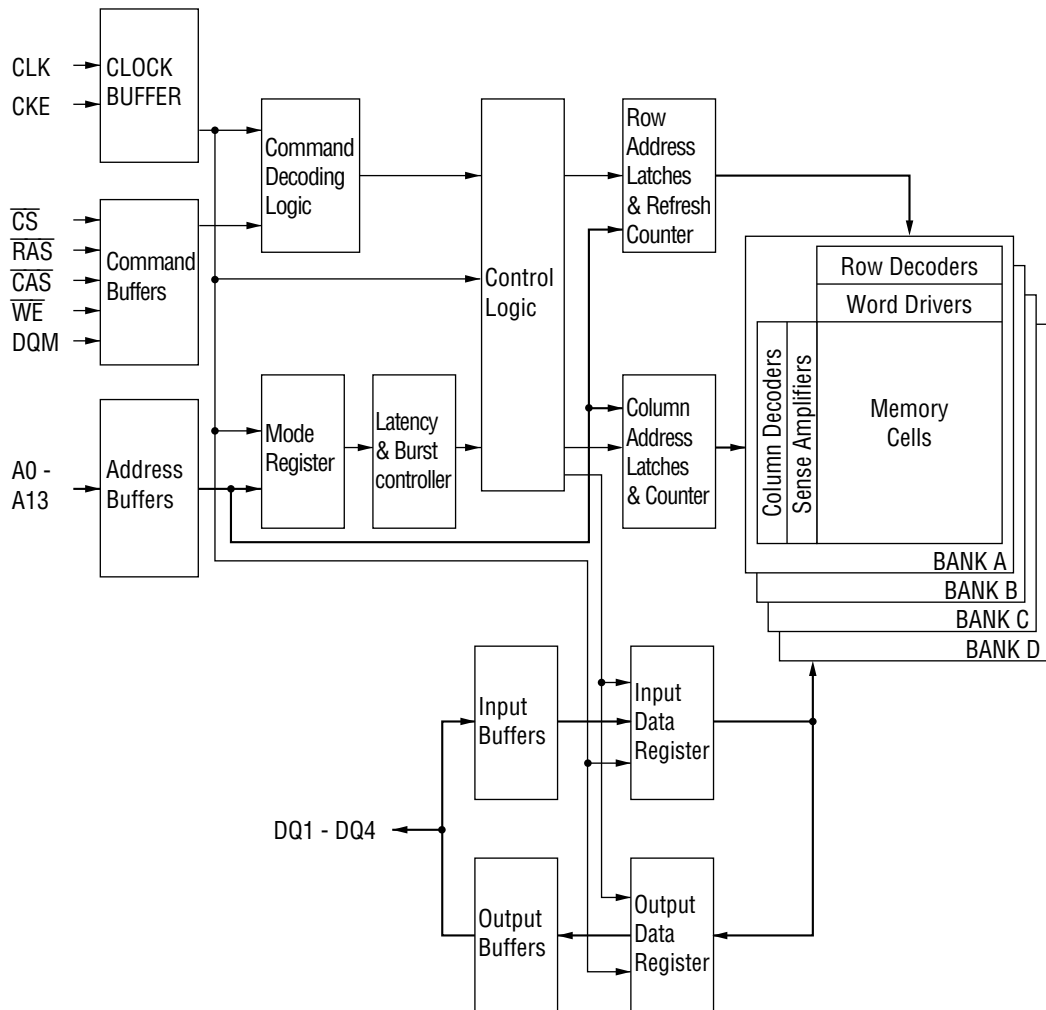
| Pin Name | Function | Pin Name | Function |
|------------------|-----------------------|------------------|----------------------------------|
| CLK | System Clock | DQM | Data Input/Output Mask |
| \overline{CS} | Chip Select | DQi | Data Input/Output |
| CKE | Clock Enable | V _{CC} | Power Supply (3.3 V) |
| A0 - A11 | Address | V _{SS} | Ground (0 V) |
| A12, A13 | Bank Select Address | V _{CCQ} | Data Output Power Supply (3.3 V) |
| \overline{RAS} | Row Address Strobe | V _{SSQ} | Data Output Ground (0 V) |
| \overline{CAS} | Column Address Strobe | NC | No Connection |
| \overline{WE} | Write Enable | | |

Note: The same power supply voltage must be provided to every V_{CC} pin and V_{CCQ} pin. The same GND voltage level must be provided to every V_{SS} pin and V_{SSQ} pin.

PIN DESCRIPTION

| | |
|---|---|
| CLK | Fetches all inputs at the "H" edge. |
| \overline{CS} | Disables or enables device operation by asserting or deactivating all inputs except CLK, CKE and DQM. |
| CKE | Masks system clock to deactivate the subsequent CLK operation. If CKE is deactivated, system clock will be masked so that the subsequent CLK operation is deactivated. CKE should be asserted at least one cycle prior to a new command. |
| Address | Row & column multiplexed. Row address: RA0 – RA11 Column address: CA0 – CA9 |
| A12, A13 (BA1, BA0) | Bank Access pins. These pins are dedicated to select one of 4 banks. |
| \overline{RAS} \overline{CAS} \overline{WE} | Functionality depends on the combination. For details, see the function truth table. |
| DQM | Masks the read data of two clocks later when DQM is set "H" at the "H" edge of the clock signal. Masks the write data of the same clock when DQM is set "H" at the "H" edge of the clock signal. |
| DQi | Data inputs/outputs are multiplexed on the same pin. |

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(Voltages referenced to V_{SS})

| Parameter | Symbol | Rating | Unit |
|---|-------------------|------------------------|------|
| Voltage on Any Pin Relative to V_{SS} | V_{IN}, V_{OUT} | -0.5 to $V_{CC} + 0.5$ | V |
| V_{CC} Supply Voltage | V_{CC}, V_{CCQ} | -0.5 to 4.6 | V |
| Storage Temperature | T_{stg} | -55 to 150 | °C |
| Power Dissipation | P_D^* | 1 | W |
| Short Circuit Current | I_{OS} | 50 | mA |
| Operating Temperature | T_{opr} | 0 to 70 | °C |

*: $T_a = 25^\circ\text{C}$

Recommended Operating Conditions

(Voltages referenced to $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|----------------------|-------------------|------|------|----------------|------|
| Power Supply Voltage | V_{CC}, V_{CCQ} | 3.0 | 3.3 | 3.6 | V |
| Input High Voltage | V_{IH} | 2.0 | — | $V_{CC} + 0.3$ | V |
| Input Low Voltage | V_{IL} | -0.3 | — | 0.8 | V |

Capacitance

($V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

| Parameter | Symbol | Min. | Max. | Unit |
|--|-----------|------|------|------|
| Input Capacitance (A0 - A13) | C_{IN1} | 2 | 5 | pF |
| Input Capacitance (CLK, CKE, \overline{CS} , RAS, \overline{CAS} , \overline{WE} , DQM) | C_{IN2} | 2 | 5 | pF |
| Input/Output Capacitance (DQ1 - DQ4) | C_{OUT} | 2 | 7 | pF |

DC Characteristics

| Parameter | Symbol | Condition | | Version | | | | | | Unit | Note |
|---|-------------------|-----------------------|--|---------|------|------|------|------|------|------|------|
| | | CKE | Others | -10 | | -12 | | H-15 | | | |
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Output High Voltage | V _{OH} | — | I _{OH} = -2 mA | 2.4 | — | 2.4 | — | 2.4 | — | V | |
| Output Low Voltage | V _{OL} | — | I _{OL} = 2 mA | — | 0.4 | — | 0.4 | — | 0.4 | V | |
| Input Leakage Current | I _{LI} | — | — | -10 | 10 | -10 | 10 | -10 | 10 | μA | |
| Output Leakage Current | I _{LO} | — | — | -10 | 10 | -10 | 10 | -10 | 10 | μA | |
| Average Power Supply Current (Operating) | I _{CC1} | CKE ≥ V _{IH} | t _{CC} = min t _{RC} = min No Burst | — | 110 | — | 95 | — | 90 | mA | 1, 2 |
| Power Supply Current (Stand by) | I _{CC2} | CKE ≥ V _{IH} | t _{CC} = min | — | 40 | — | 35 | — | 30 | mA | 3 |
| Average Power Supply Current (Clock Suspension) | I _{CC3S} | CKE ≤ V _{IL} | t _{CC} = min | — | 15 | — | 15 | — | 15 | mA | 2 |
| Average Power Supply Current (Active Stand by) | I _{CC3} | CKE ≥ V _{IH} | t _{CC} = min | — | 75 | — | 65 | — | 55 | mA | 3 |
| Power Supply Current (Burst) | I _{CC4} | CKE ≥ V _{IH} | t _{CC} = min | — | 130 | — | 110 | — | 95 | mA | 1, 2 |
| Power Supply Current (Auto-Refresh) | I _{CC5} | CKE ≥ V _{IH} | t _{CC} = min t _{RC} = min | — | 180 | — | 150 | — | 150 | mA | 2 |
| Average Power Supply Current (Self-Refresh) | I _{CC6} | CKE ≤ V _{IL} | t _{CC} = min | — | 2 | — | 2 | — | 2 | mA | |
| Average Power Supply Current (Power down) | I _{CC7} | CKE ≤ V _{IL} | t _{CC} = min | — | 2 | — | 2 | — | 2 | mA | |

- Notes:
1. Measured with outputs open.
 2. The address and data can be changed once or left unchanged during one cycle.
 3. The address and data can be changed once or left unchanged during two cycles.

Mode Set Address Keys

| CAS Latency | | | | Burst Type | | Burst Length | | | | |
|-------------|----|----|----------|------------|------------|--------------|----|----|----------|----------|
| A6 | A5 | A4 | CL | A3 | BT | A2 | A1 | A0 | BT = 0 | BT = 1 |
| 0 | 0 | 0 | Reserved | 0 | Sequential | 0 | 0 | 0 | Reserved | Reserved |
| 0 | 0 | 1 | Reserved | 1 | Interleave | 0 | 0 | 1 | 2 | 2 |
| 0 | 1 | 0 | 2 | | | 0 | 1 | 0 | 4 | 4 |
| 0 | 1 | 1 | 3 | | | 0 | 1 | 1 | 8 | 8 |
| 1 | 0 | 0 | Reserved | | | 1 | 0 | 0 | Reserved | Reserved |
| 1 | 0 | 1 | Reserved | | | 1 | 0 | 1 | Reserved | Reserved |
| 1 | 1 | 0 | Reserved | | | 1 | 1 | 0 | Reserved | Reserved |
| 1 | 1 | 1 | Reserved | | | 1 | 1 | 1 | Reserved | Reserved |

Note: A7, A8, A9, A10, A11, A12 and A13 should stay "L" during mode set cycle.

POWER ON SEQUENCE

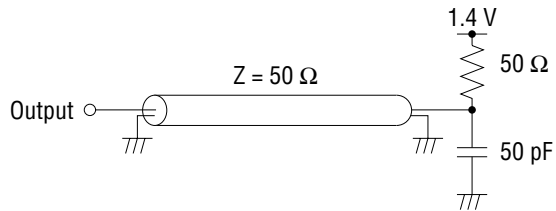
1. With inputs in NOP state, turn on the power supply and start the system clock.
2. After the V_{CC} voltage has reached the specified level, pause for 200 μs or more with the input kept in NOP state.
3. Issue the precharge all bank command.
4. Apply a CBR auto-refresh eight or more times.
5. Enter the mode register setting command.

AC Characteristics

Note 1, 2

| Parameter | Symbol | MD56V62400-10 | | MD56V62400-12 | | MD56V62400H-15 | | Unit | Note | |
|---|------------------|-------------------------|-----------------|-------------------------|-----------------|-------------------------|-----------------|-------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | | |
| Clock Cycles Time | t _{CC} | CL = 3 | 10 | — | 12 | — | 15 | — | ns | |
| | | CL = 2 | 15 | — | 17.5 | — | 15 | — | ns | |
| Access Time from Clock | t _{AC} | CL = 3 | — | 9 | — | 10 | — | 9 | ns | 3, 4 |
| | | CL = 2 | — | 9 | — | 14 | — | 9 | ns | 3, 4 |
| Clock "H" Pulse Time | t _{CH} | 3 | — | 3 | — | 3 | — | ns | | |
| Clock "L" Pulse Time | t _{CL} | 3 | — | 3 | — | 3 | — | ns | | |
| Input Setup Time | t _{SI} | 3 | — | 3 | — | 3 | — | ns | | |
| Input Hold Time | t _{HI} | 1 | — | 1.5 | — | 1 | — | ns | | |
| Output Low Impedance Time from Clock | t _{OLZ} | 3 | — | 3 | — | 3 | — | ns | | |
| Output High Impedance Time from Clock | t _{OZH} | — | 8 | — | 10 | — | 8 | ns | | |
| Output Hold from Clock | t _{OH} | 3 | — | 3 | — | 3 | — | ns | 3 | |
| $\overline{\text{RAS}}$ Cycle Time | t _{RC} | 90 | — | 115 | — | 105 | — | ns | | |
| $\overline{\text{RAS}}$ Precharge Time | t _{RP} | 30 | — | 45 | — | 30 | — | ns | | |
| $\overline{\text{RAS}}$ Active Time | t _{RAS} | 60 | 10 ⁵ | 70 | 10 ⁵ | 70 | 10 ⁵ | ns | | |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time | t _{RCD} | 30 | — | 35 | — | 30 | — | ns | | |
| Write Recovery Time | t _{WR} | 15 | — | 24 | — | 15 | — | ns | | |
| $\overline{\text{RAS}}$ to $\overline{\text{RAS}}$ Bank Active Delay Time | t _{RRD} | 20 | — | 24 | — | 24 | — | ns | | |
| Refresh Time | t _{REF} | — | 64 | — | 64 | — | 64 | ms | | |
| Power-down Exit Set-up Time | t _{PDE} | t _{SI} + 1 CLK | — | t _{SI} + 1 CLK | — | t _{SI} + 1 CLK | — | ns | | |
| Input Level Transition Time | t _T | — | 3 | — | 3 | — | 3 | ns | | |
| $\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ Delay Time (Min.) | t _{CCD} | 1 | — | 1 | — | 1 | — | Cycle | | |
| Clock Disable Time from CKE | t _{CKE} | 1 | — | 1 | — | 1 | — | Cycle | | |
| Data Output High Impedance Time from DQM | t _{DOZ} | 2 | — | 2 | — | 2 | — | Cycle | | |
| Data Input Mask Time from DQM | t _{DOD} | 0 | — | 0 | — | 0 | — | Cycle | | |
| Data Input Time from Write Command | t _{DWD} | 0 | — | 0 | — | 0 | — | Cycle | | |
| Data Output High Impedance Time from Precharge Command | t _{ROH} | 2 | — | 2 | — | 2 | — | Cycle | | |
| Active Command Input Time from Mode Register Set Command Input (Min.) | t _{MRD} | 3 | — | 3 | — | 3 | — | Cycle | | |
| Write Command Input Time from Output | t _{OWD} | 2 | — | 2 | — | 2 | — | Cycle | | |

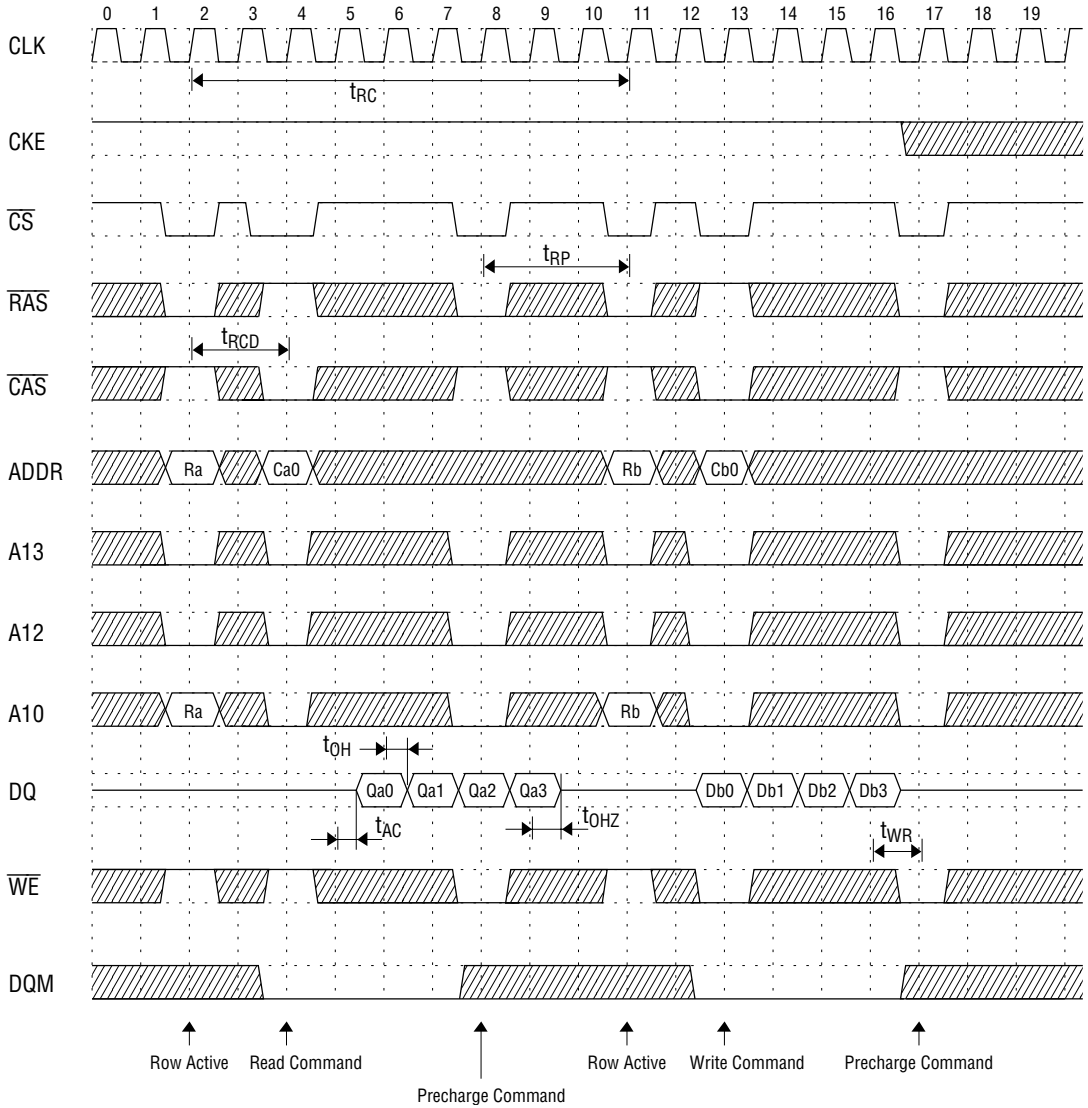
- Notes :
1. AC measurements assume that $t_T = 1$ ns.
 2. The reference level for timing of input signals is 1.4 V.
 3. Output load.



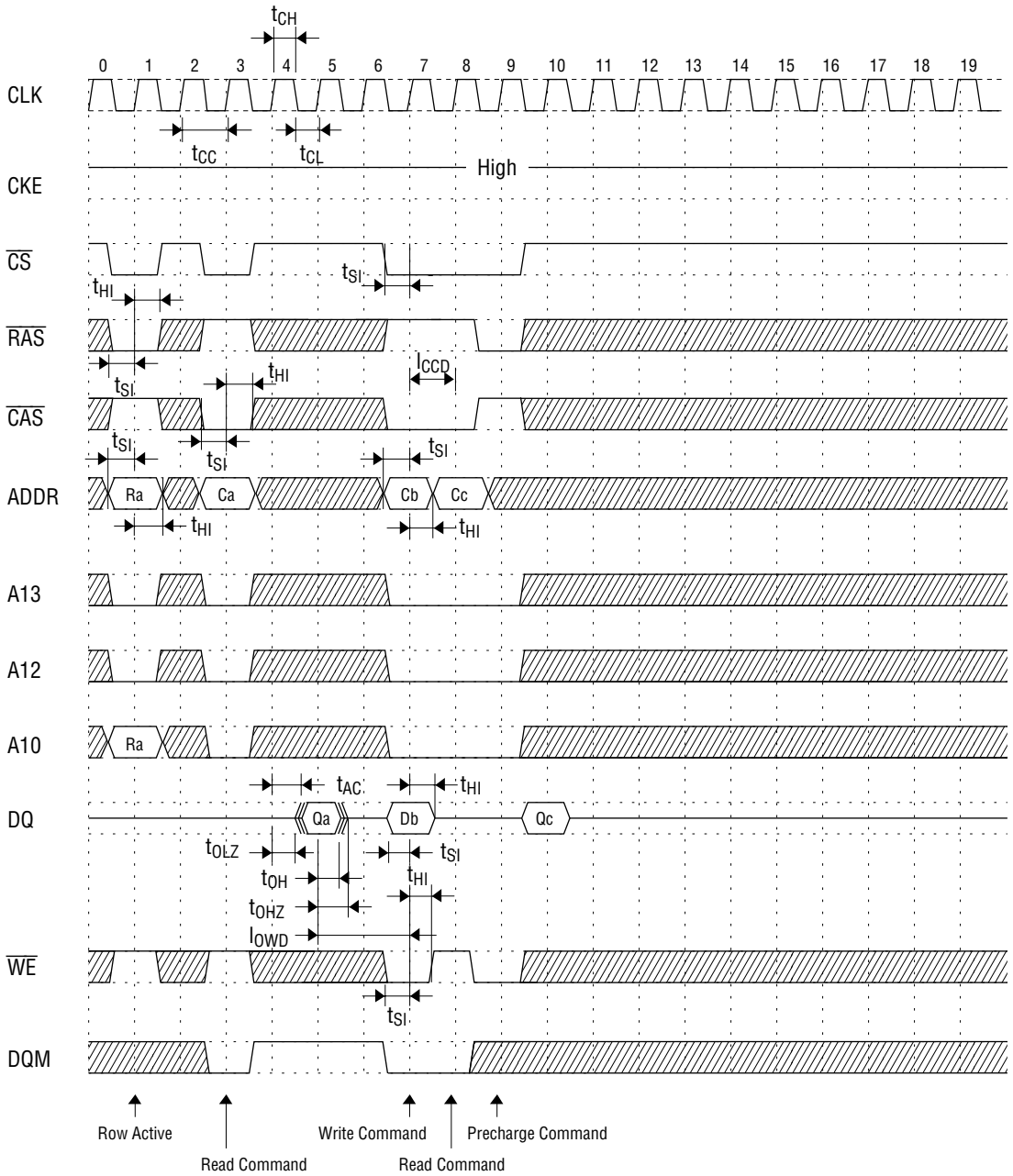
4. The access time is defined at 1.4 V.
5. If t_T is longer than 1 ns, then the reference level for timing of input signals is V_{IH} and V_{IL} .

TIMING WAVEFORM

Read & Write Cycle (Same Bank) @ $\overline{\text{CAS}}$ Latency = 2, Burst Length = 4



Single Bit Read-Write-Read Cycle (Same Page) @ $\overline{\text{CAS}}$ Latency = 2, Burst Length = 4



- *Notes:**
1. When \overline{CS} is set "High" at a clock transition from "Low" to "High", all inputs except CKE and DQM are invalid.
 2. When issuing an active, read or write command, the bank is selected by A12 and A13.

| A12 | A13 | Active, read or write |
|-----|-----|-----------------------|
| 0 | 0 | Bank A |
| 0 | 1 | Bank B |
| 1 | 0 | Bank C |
| 1 | 1 | Bank D |

3. The auto precharge function is enabled or disabled by the A10 input when the read or write command is issued.

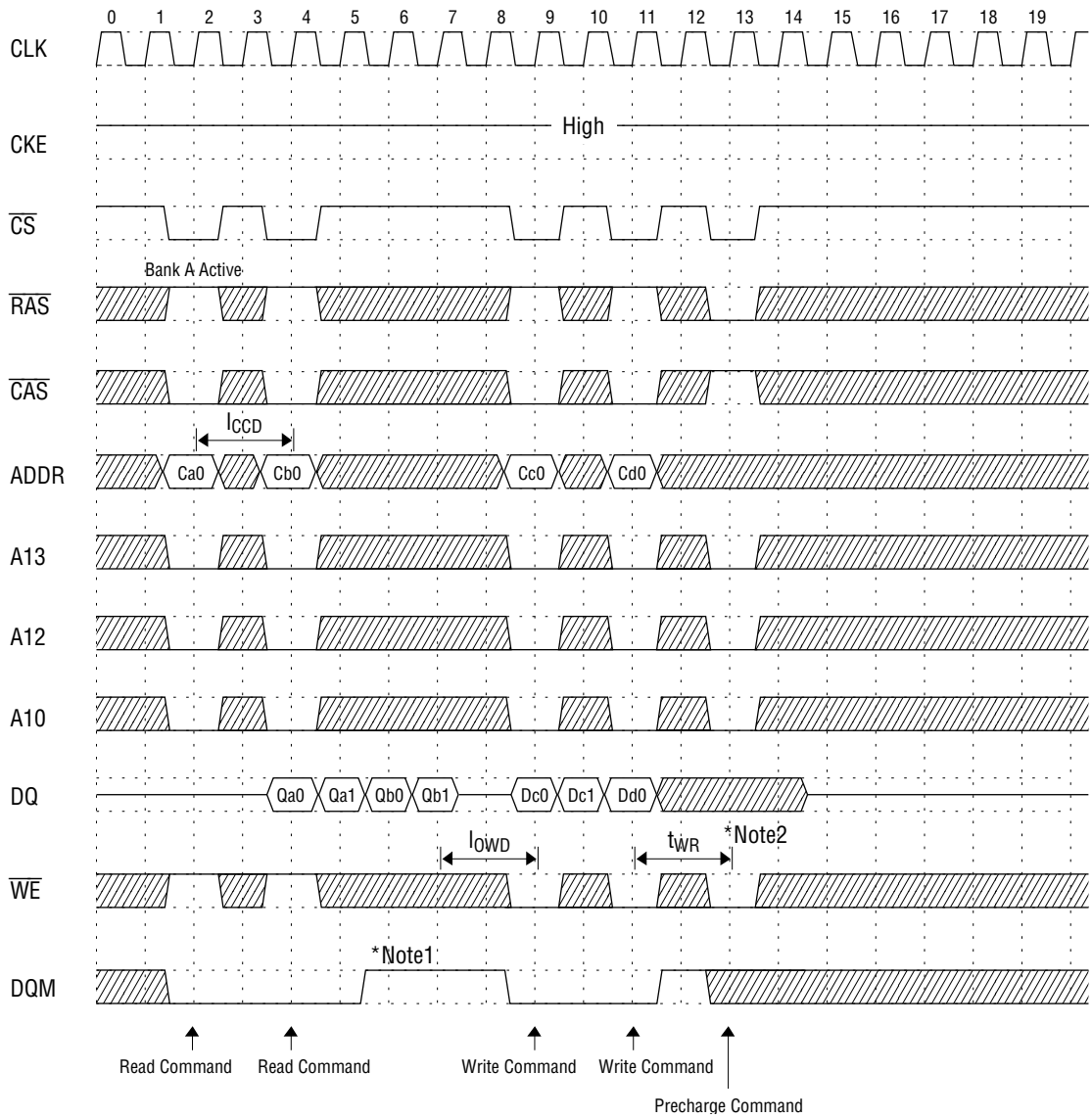
| A10 | A12 | A13 | Operation |
|-----|-----|-----|---|
| 0 | 0 | 0 | After the end of burst, bank A holds the idle status. |
| 1 | 0 | 0 | After the end of burst, bank A is precharged automatically. |
| 0 | 0 | 1 | After the end of burst, bank B holds the idle status. |
| 1 | 0 | 1 | After the end of burst, bank B is precharged automatically. |
| 0 | 1 | 0 | After the end of burst, bank C holds the idle status. |
| 1 | 1 | 0 | After the end of burst, bank C is precharged automatically. |
| 0 | 1 | 1 | After the end of burst, bank D holds the idle status. |
| 1 | 1 | 1 | After the end of burst, bank D is precharged automatically. |

4. When issuing a precharge command, the bank to be precharged is selected by the A10, A12 and A13 inputs.

| A10 | A12 | A13 | Operation |
|-----|-----|-----|---------------------------|
| 0 | 0 | 0 | Bank A is precharged. |
| 0 | 0 | 1 | Bank B is precharged. |
| 0 | 1 | 0 | Bank C is precharged. |
| 0 | 1 | 1 | Bank D is precharged. |
| 1 | X | X | All banks are precharged. |

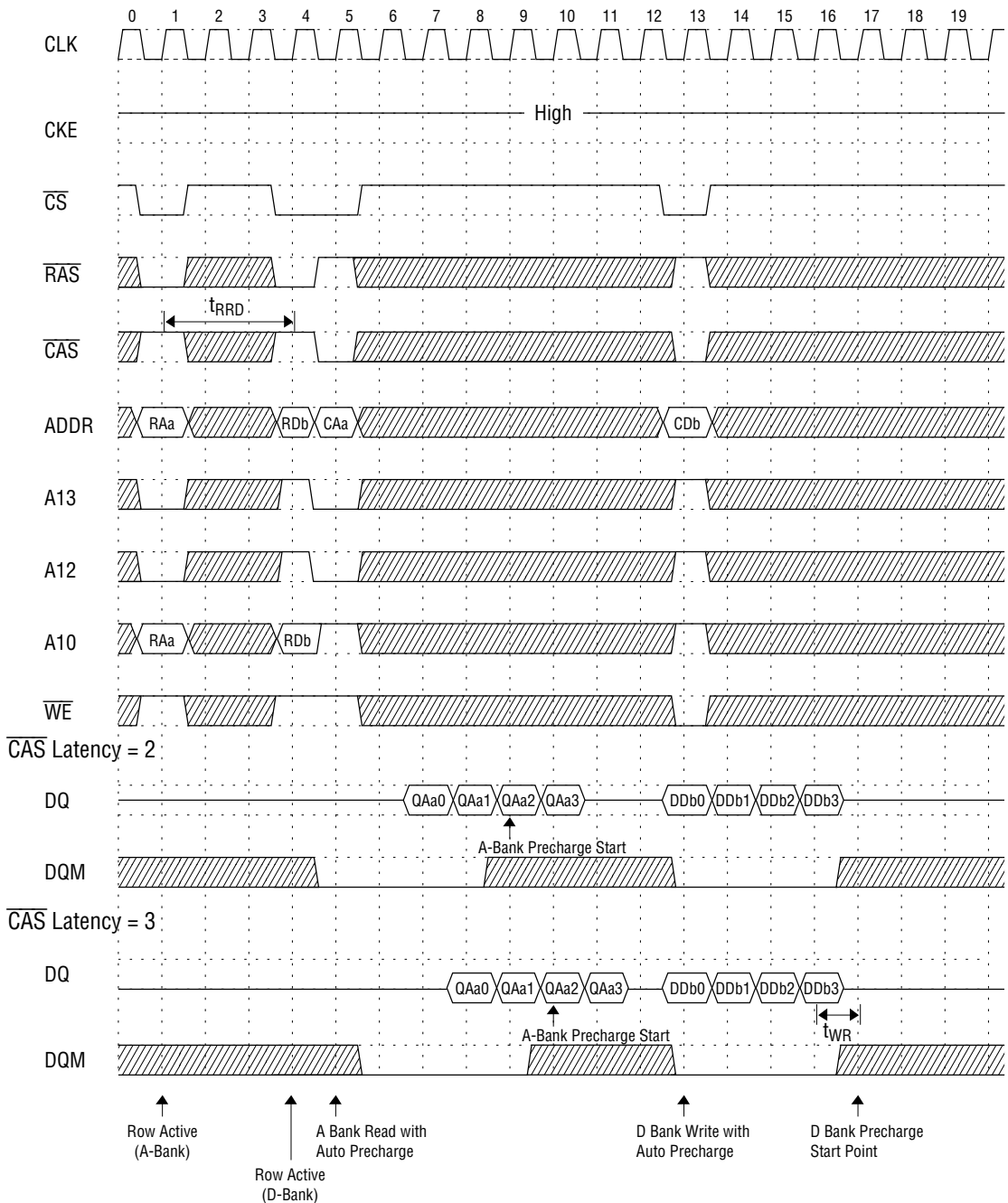
5. The input data and the write command are latched by the same clock (Write latency = 0).
6. The output is forced to high impedance by (1 CLK + t_{OHZ}) after DQM entry.

Page Read & Write Cycle (Same Bank) @ $\overline{\text{CAS}}$ Latency = 2, Burst Length = 4

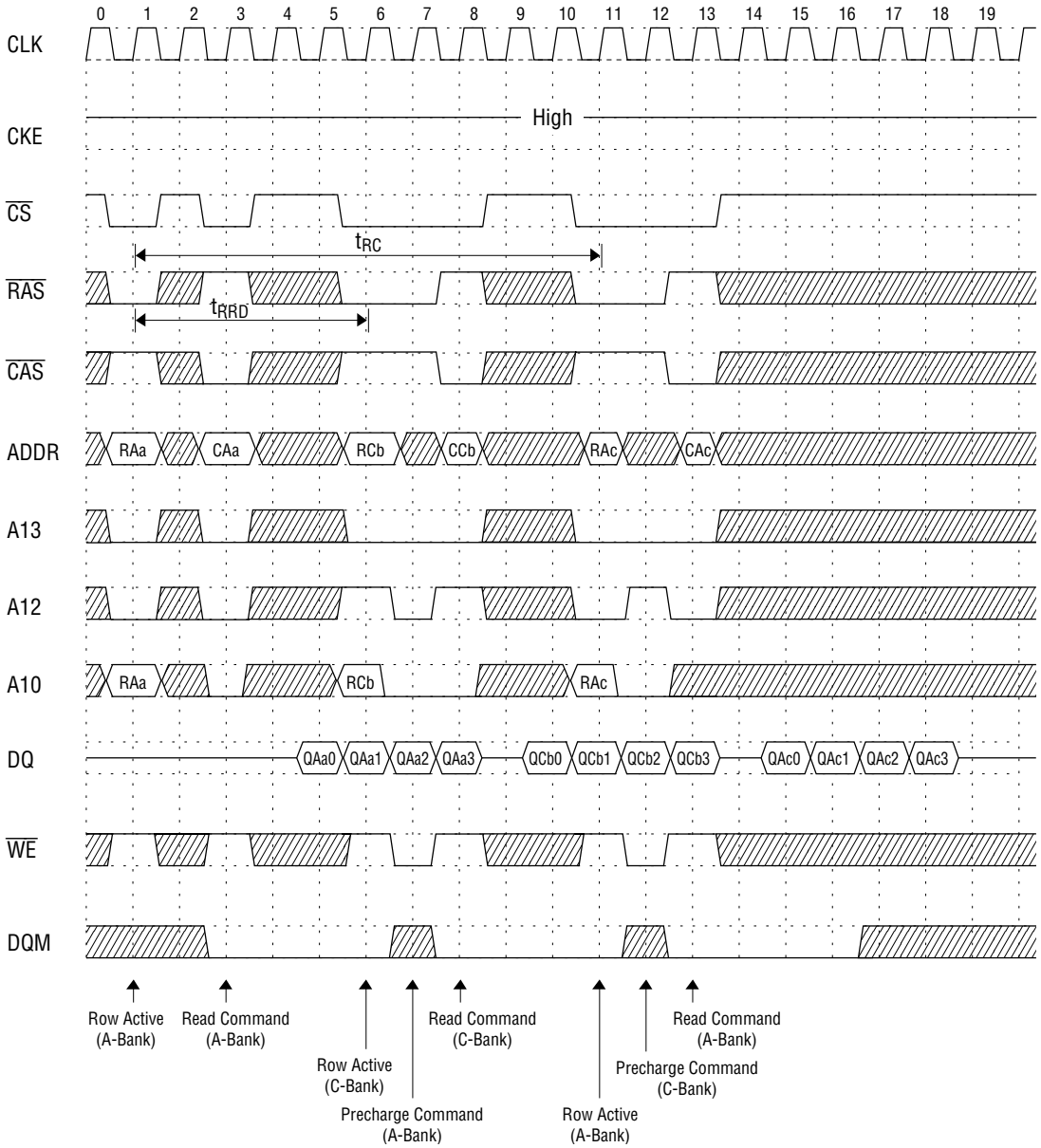


- *Notes:**
1. To write data before a burst read ends, DQM should be asserted three cycles prior to the write command to avoid bus contention.
 2. To assert row precharge before a burst write ends, wait t_{WR} after the last write data input. Input data during the precharge input cycle will be masked internally.

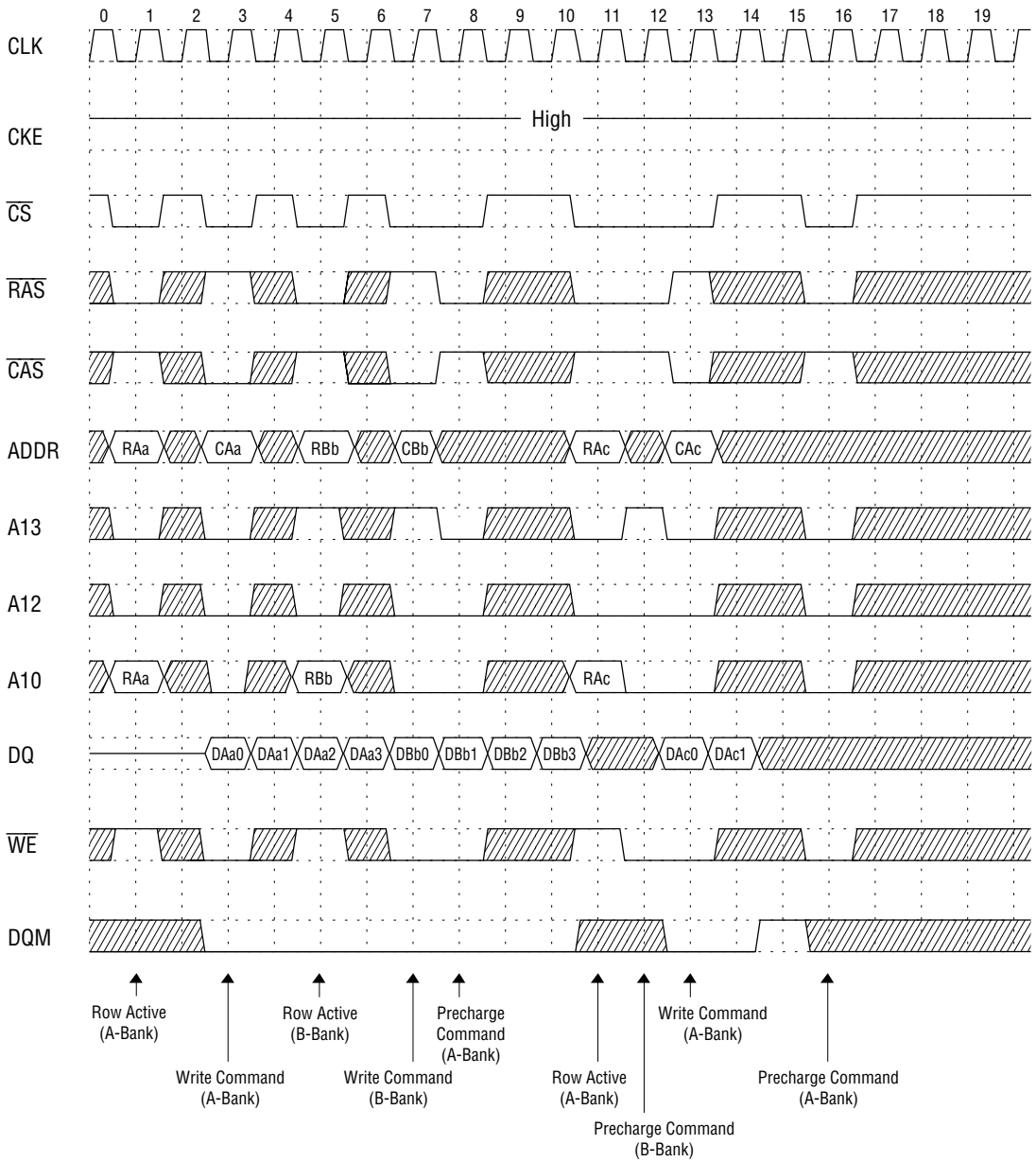
Read & Write Cycle with Auto Precharge @ Burst Length = 4



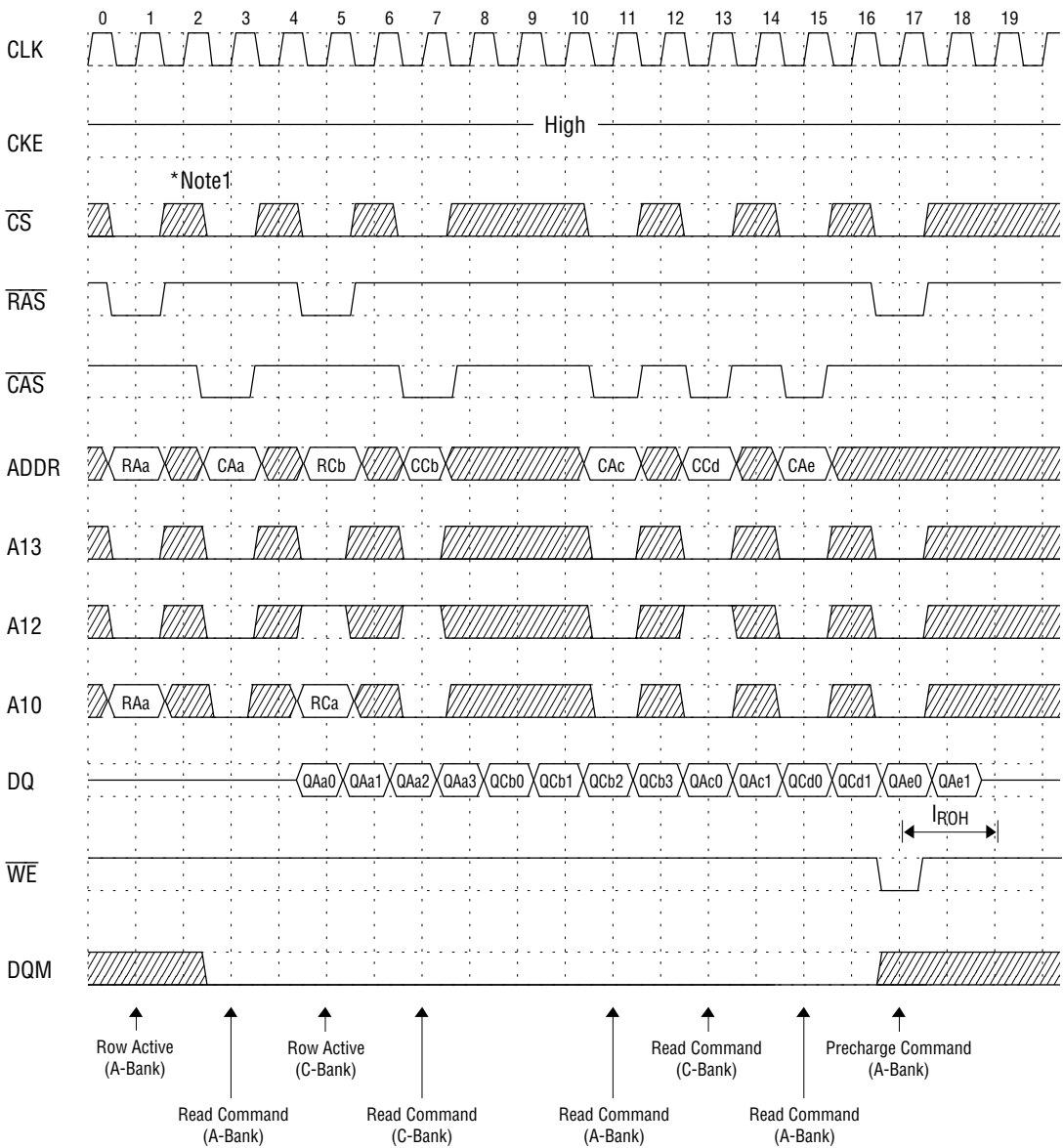
Bank Interleave Random Row Read Cycle @ $\overline{\text{CAS}}$ Latency = 2, Burst Length = 4



Bank Interleave Random Row Write Cycle @ $\overline{\text{CAS}}$ Latency = 2, Burst Length = 4

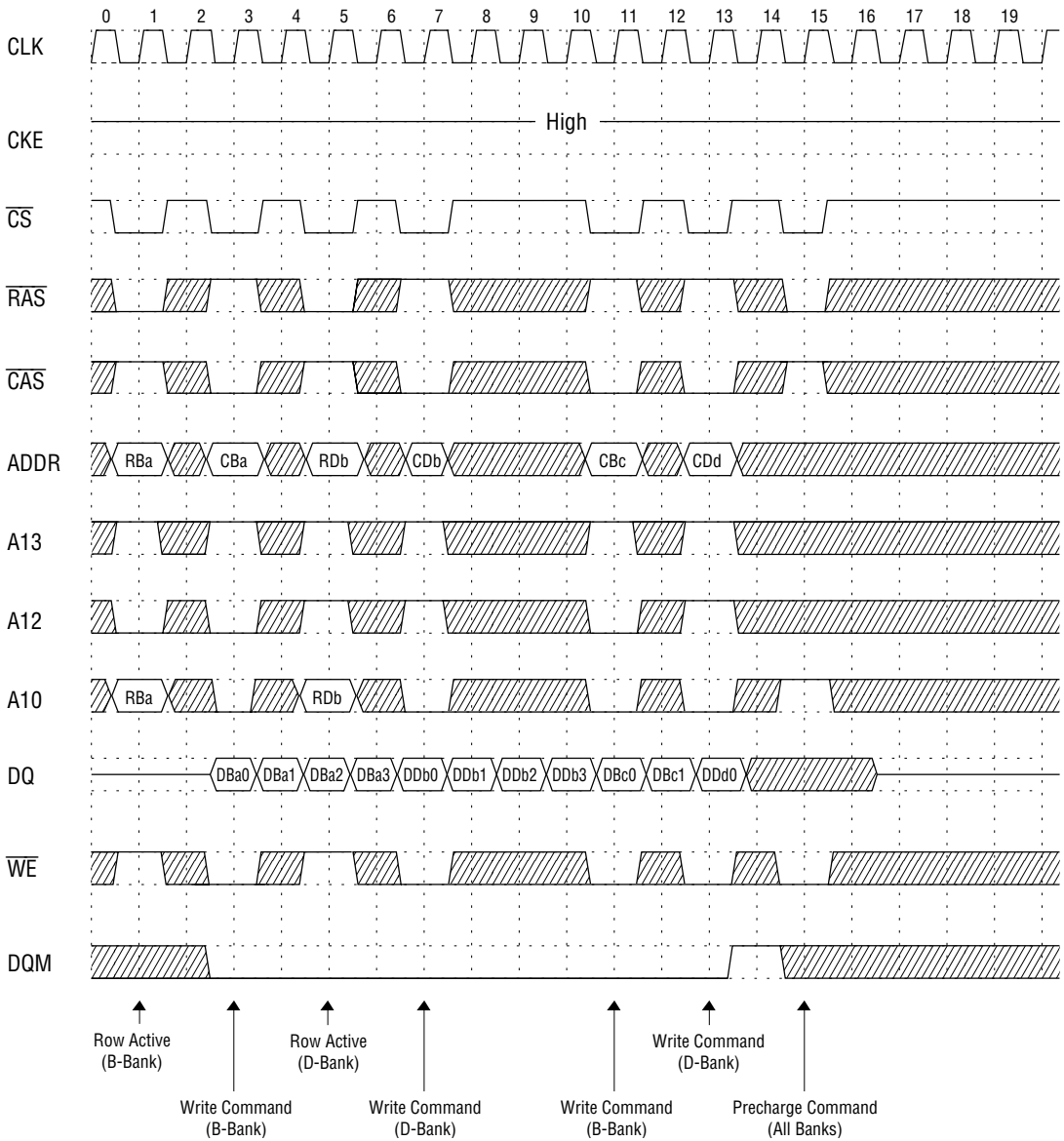


Bank Interleave Page Read Cycle @ $\overline{\text{CAS}}$ Latency = 2, Burst Length = 4

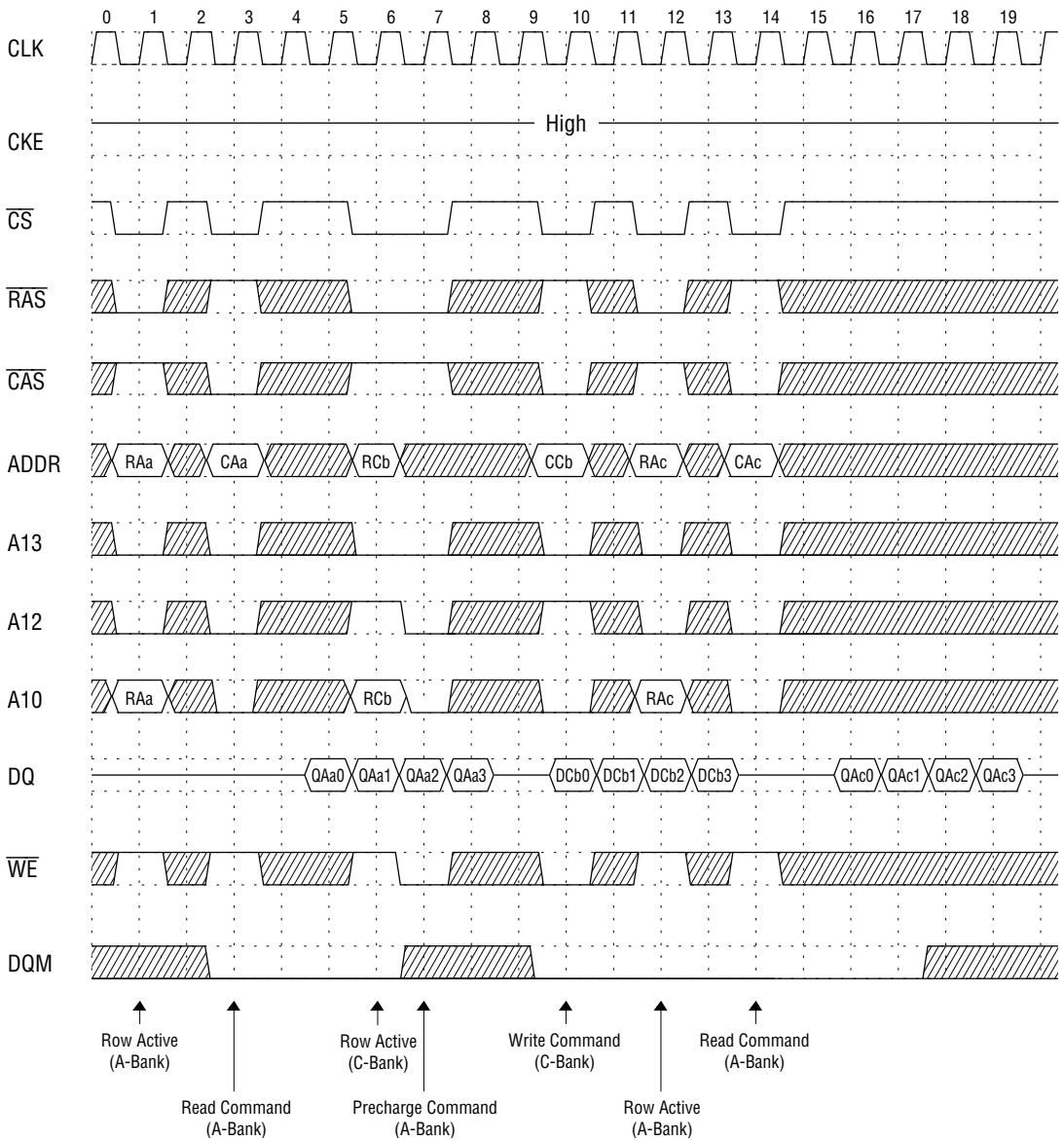


***Note:** 1. $\overline{\text{CS}}$ is ignored when $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ are high at the same cycle.

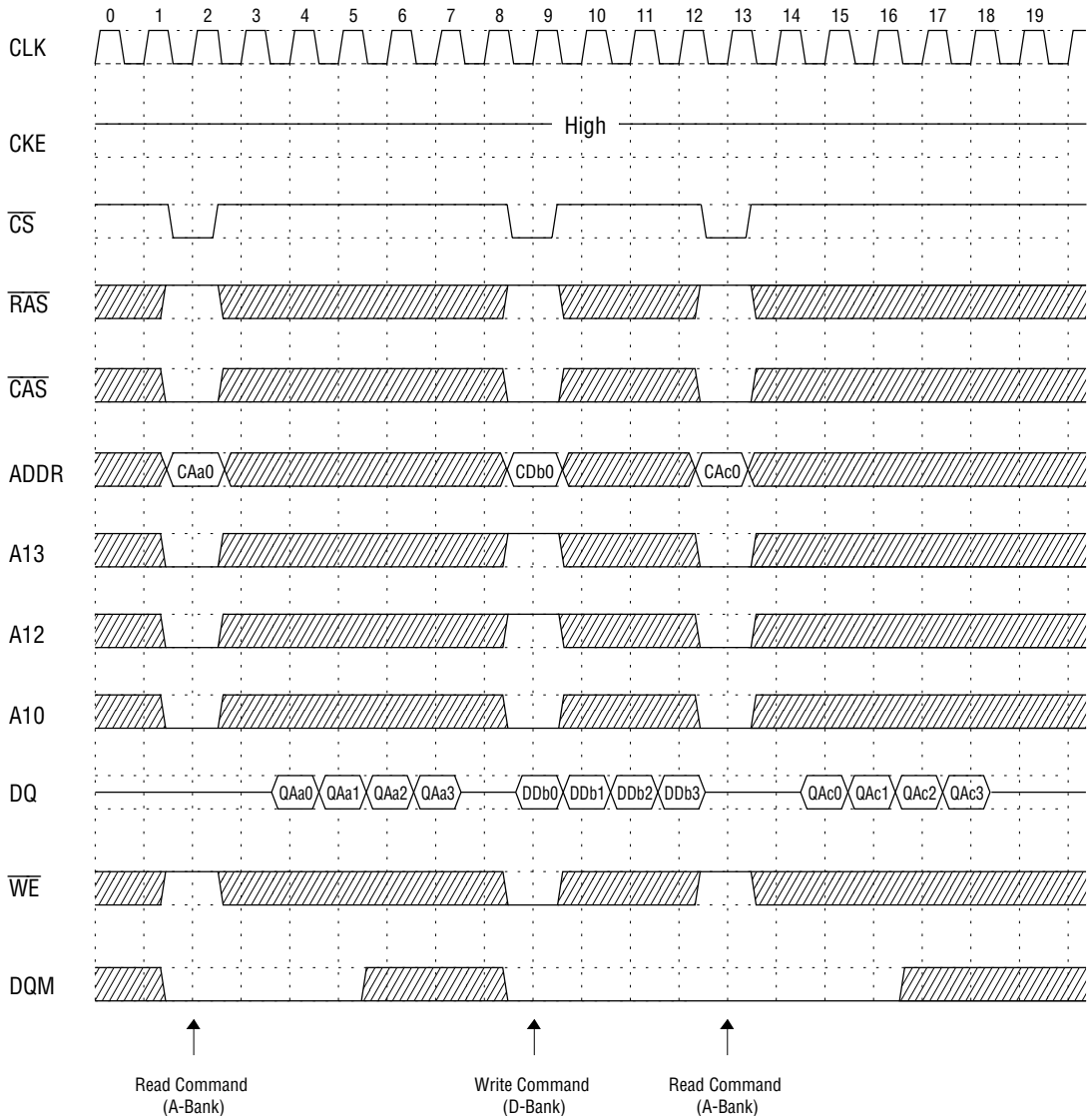
Bank Interleave Page Write Cycle @ $\overline{\text{CAS}}$ Latency = 2, Burst Length = 4



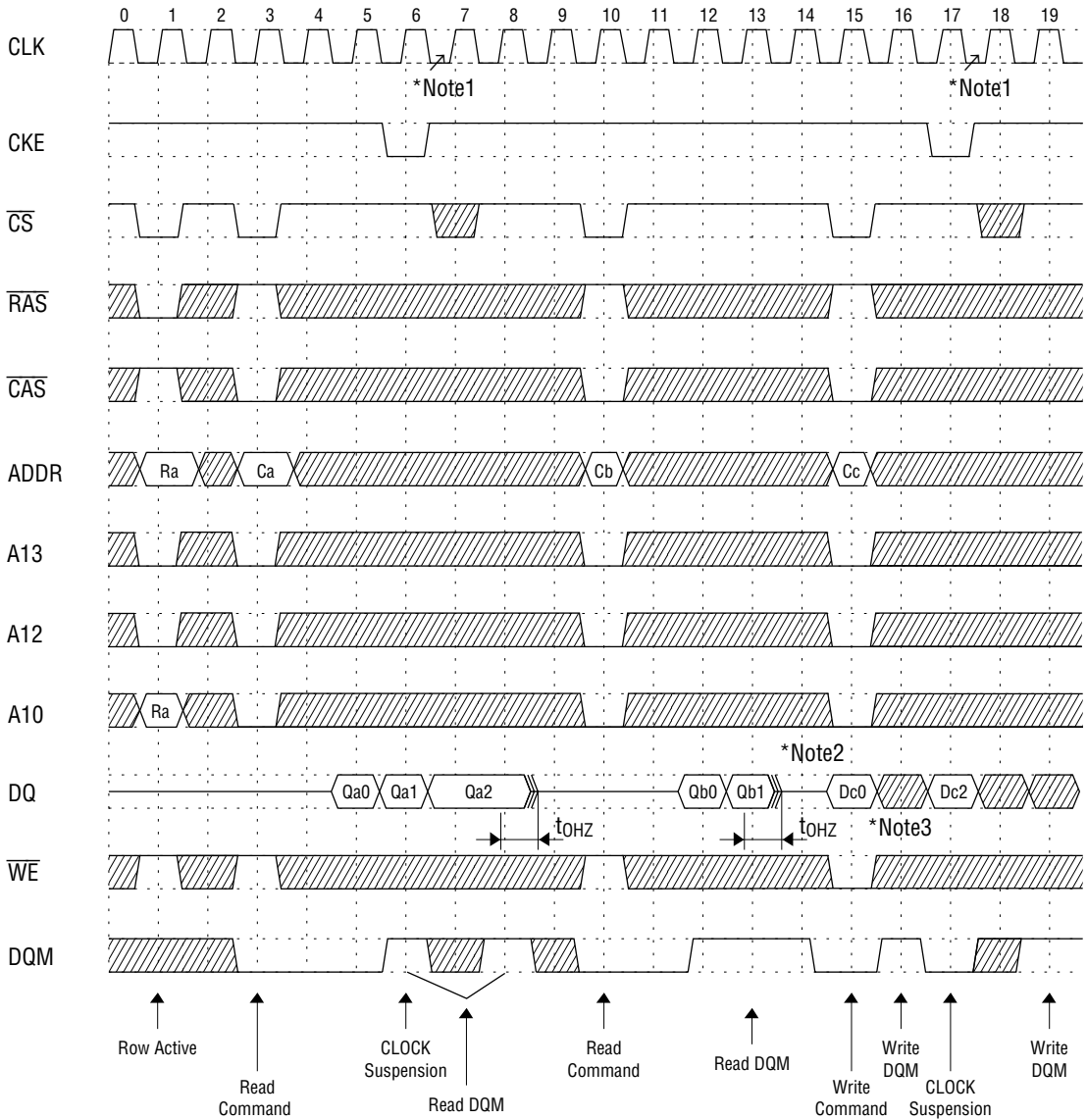
Bank Interleave Random Row Read/Write Cycle @ $\overline{\text{CAS}}$ Latency = 2, Burst Length = 4



Bank Interleave Page Read/Write Cycle @ $\overline{\text{CAS}}$ Latency = 2, Burst Length = 4

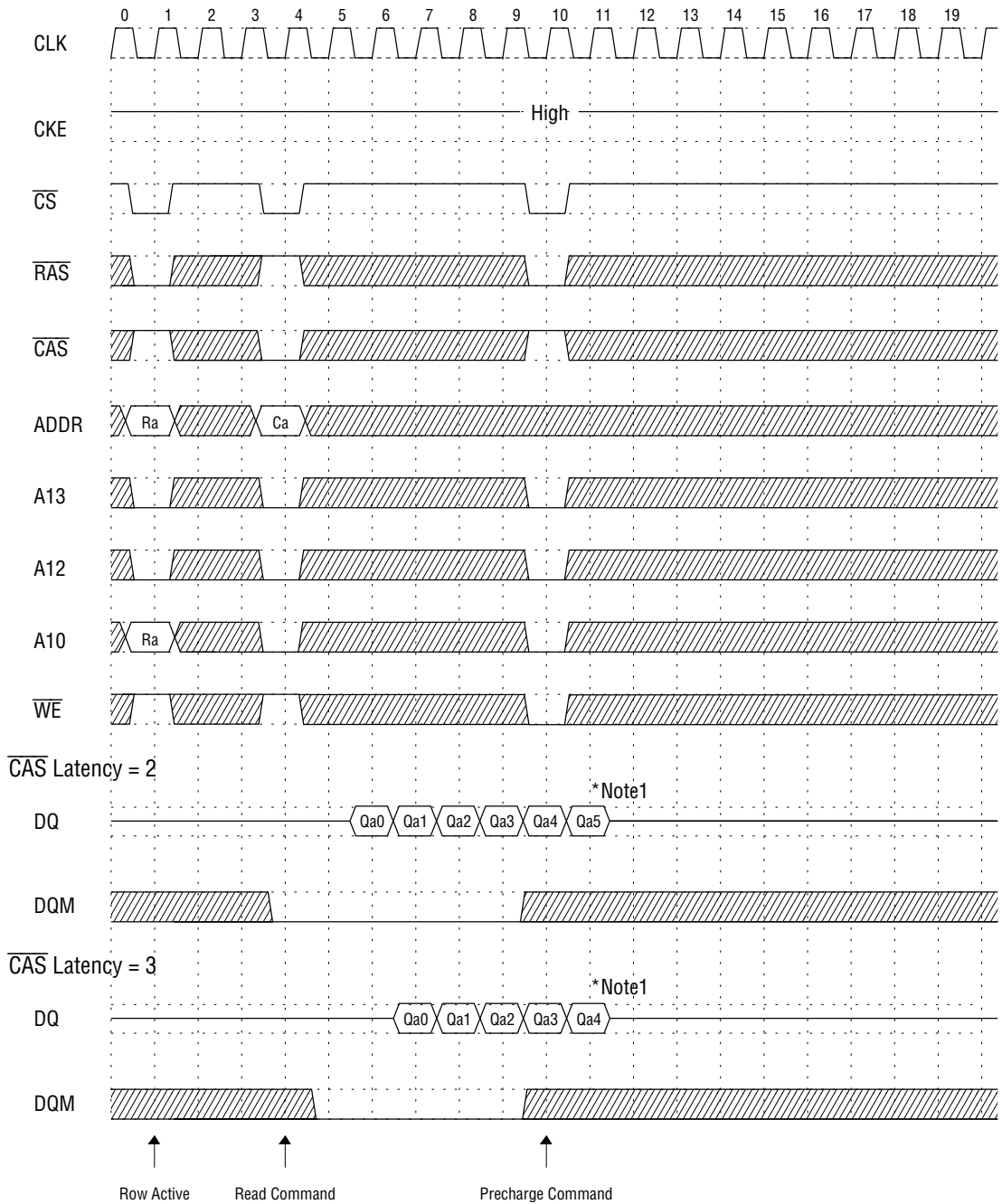


Clock Suspension & DQM Operation Cycle @ $\overline{\text{CAS}}$ Latency = 2, Burst Length = 4



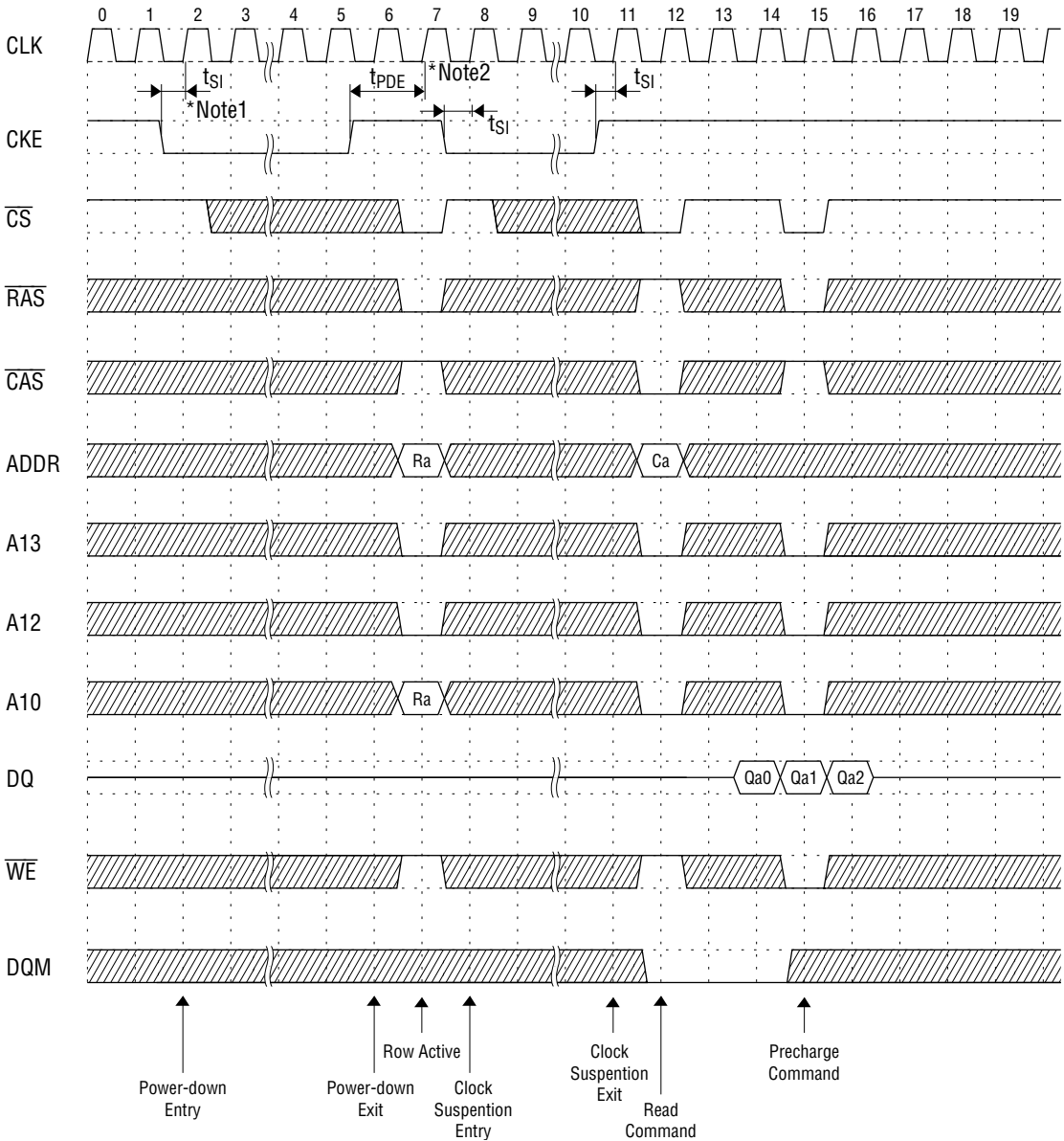
- *Notes:**
1. When Clock Suspension is asserted, the next clock cycle is ignored.
 2. When DQM is asserted, the read data after two clock cycles is masked.
 3. When DQM is asserted, the write data in the same clock cycle is masked.

Read Interruption by Precharge Command @ Burst Length = 8



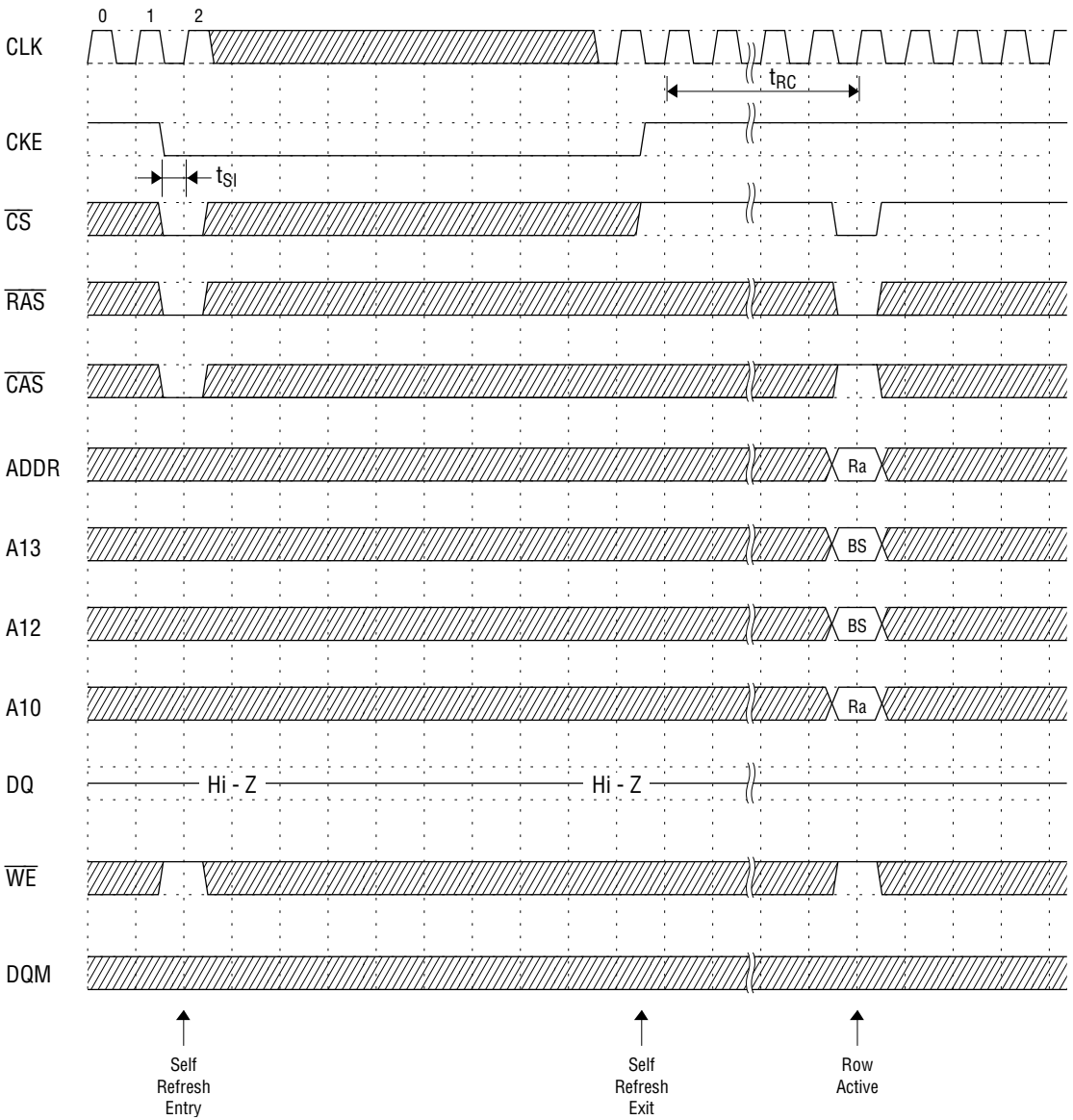
***Note:** 1. If row precharge is asserted before burst read ends, then the read data will not output after the second clock cycle of the precharge command.

Power Down Mode @ $\overline{\text{CAS}}$ Latency = 2, Burst Length = 4

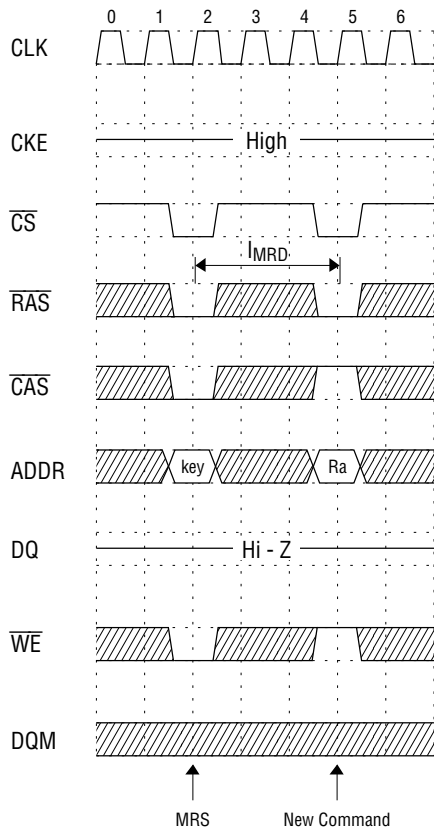


- *Notes:**
1. When all banks are in precharge state, and if CKE is set low, then the MD56V62400/H enters power-down mode and maintains the mode while CKE is low.
 2. To release the circuit from power-down mode, CKE has to be set high for longer than t_{PDE} ($t_{SI} + 1 \text{ CLK}$).

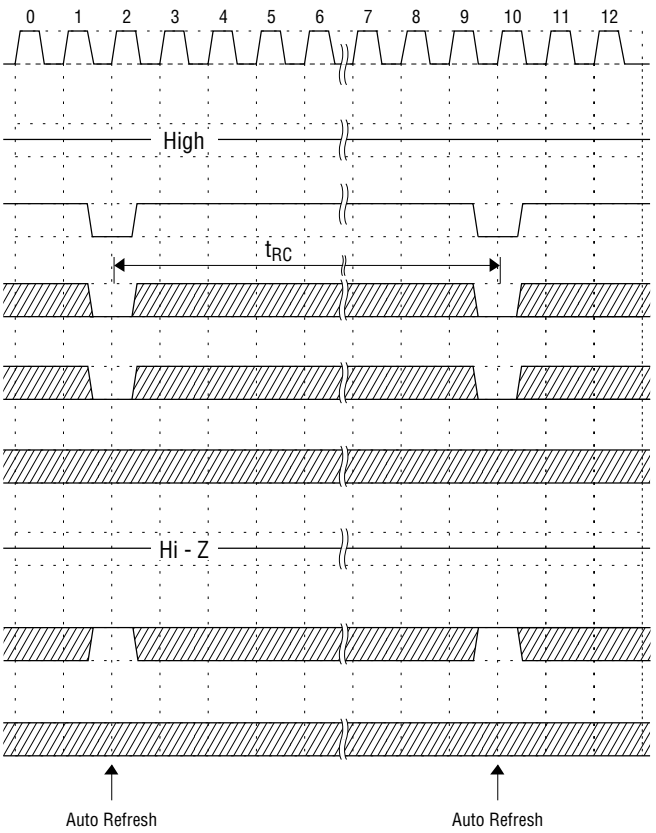
Self Refresh Cycle



Mode Register Set Cycle



Auto Refresh Cycle



FUNCTION TRUTH TABLE (Table 1) (1/2)

| Current State ¹ | CS | RAS | CAS | WE | BA | ADDR | Action |
|----------------------------|----|-----|-----|----|----|---------|---|
| Idle | H | X | X | X | X | X | NOP |
| | L | H | H | H | X | X | NOP |
| | L | H | H | L | BA | X | ILLEGAL ² |
| | L | H | L | X | BA | CA | ILLEGAL ² |
| | L | L | H | H | BA | RA | Row Active |
| | L | L | H | L | BA | A10 | NOP ⁴ |
| | L | L | L | H | X | X | Auto-Refresh or Self-Refresh ⁵ |
| | L | L | L | L | L | OP Code | Mode Register Write |
| Row Active | H | X | X | X | X | X | NOP |
| | L | H | H | X | X | X | NOP |
| | L | H | L | H | BA | CA, A10 | Read |
| | L | H | L | L | BA | CA, A10 | Write |
| | L | L | H | H | BA | RA | ILLEGAL ² |
| | L | L | H | L | BA | A10 | Precharge |
| | L | L | L | X | X | X | ILLEGAL |
| Read | H | X | X | X | X | X | NOP (Continue Row Active after Burst ends) |
| | L | H | H | H | X | X | NOP (Continue Row Active after Burst ends) |
| | L | H | H | L | BA | X | Reserved |
| | L | H | L | H | BA | CA, A10 | Term Burst, start new Burst Read |
| | L | H | L | L | BA | CA, A10 | Term Burst, start new Burst Write |
| | L | L | H | H | BA | RA | ILLEGAL ² |
| | L | L | H | L | BA | A10 | Term Burst, execute Row Precharge |
| | L | L | L | X | X | X | ILLEGAL |
| Write | H | X | X | X | X | X | NOP (Continue Row Active after Burst ends) |
| | L | H | H | H | X | X | NOP (Continue Row Active after Burst ends) |
| | L | H | H | L | BA | X | Reserved (Term Burst) --> Row Active |
| | L | H | L | H | BA | CA, A10 | Term Burst, start new Burst Read |
| | L | H | L | L | BA | CA, A10 | Term Burst, start new Burst Write |
| | L | L | H | H | BA | RA | ILLEGAL ² |
| | L | L | H | L | BA | A10 | Term Burst, execute Row Precharge |
| | L | L | L | X | X | X | ILLEGAL |
| Read with Auto Precharge | H | X | X | X | X | X | NOP (Continue Burst to End and enter Row Precharge) |
| | L | H | H | H | X | X | NOP (Continue Burst to End and enter Row Precharge) |
| | L | H | H | L | BA | X | ILLEGAL ² |
| | L | H | L | H | BA | CA, A10 | ILLEGAL ² |
| | L | H | L | L | X | X | ILLEGAL |
| | L | L | H | X | BA | RA, A10 | ILLEGAL ² |
| | L | L | L | X | X | X | ILLEGAL |
| Write with Auto Precharge | H | X | X | X | X | X | NOP (Continue Burst to End and enter Row Precharge) |
| | L | H | H | H | X | X | NOP (Continue Burst to End and enter Row Precharge) |
| | L | H | H | L | BA | X | ILLEGAL ² |
| | L | H | L | H | BA | CA, A10 | ILLEGAL ² |
| | L | H | L | L | X | X | ILLEGAL |
| | L | L | H | X | BA | RA, A10 | ILLEGAL ² |
| | L | L | L | X | X | X | ILLEGAL |

FUNCTION TRUTH TABLE (Table 1) (2/2)

| Current State ¹ | CS | RAS | CAS | WE | BA | ADDR | Action |
|----------------------------|----|-----|-----|----|----|------|---|
| Precharge | H | X | X | X | X | X | NOP --> Idle after t _{RP} |
| | L | H | H | H | X | X | NOP --> Idle after t _{RP} |
| | L | H | H | L | BA | X | ILLEGAL ² |
| | L | H | L | X | BA | CA | ILLEGAL ² |
| | L | L | H | H | BA | RA | ILLEGAL ² |
| | L | L | H | L | BA | A10 | NOP ⁴ |
| | L | L | L | X | X | X | ILLEGAL |
| Write Recovery | H | X | X | X | X | X | NOP |
| | L | H | H | H | X | X | NOP |
| | L | H | H | L | BA | X | ILLEGAL ² |
| | L | H | L | X | BA | CA | ILLEGAL ² |
| | L | L | H | H | BA | RA | ILLEGAL ² |
| | L | L | H | L | BA | A10 | ILLEGAL ² |
| | L | L | L | X | X | X | ILLEGAL |
| Row Active | H | X | X | X | X | X | NOP --> Row Active after t _{RCD} |
| | L | H | H | H | X | X | NOP --> Row Active after t _{RCD} |
| | L | H | H | L | BA | X | ILLEGAL ² |
| | L | H | L | X | BA | CA | ILLEGAL ² |
| | L | L | H | H | BA | RA | ILLEGAL ² |
| | L | L | H | L | BA | A10 | ILLEGAL ² |
| | L | L | L | X | X | X | ILLEGAL |
| Refresh | H | X | X | X | X | X | NOP --> Idle after t _{RC} |
| | L | H | H | X | X | X | NOP --> Idle after t _{RC} |
| | L | H | L | X | X | X | ILLEGAL |
| | L | L | H | X | X | X | ILLEGAL |
| | L | L | L | X | X | X | ILLEGAL |
| Mode Register Access | H | X | X | X | X | X | NOP |
| | L | H | H | H | X | X | NOP |
| | L | H | H | L | X | X | ILLEGAL |
| | L | H | L | X | X | X | ILLEGAL |
| | L | L | X | X | X | X | ILLEGAL |

ABBREVIATIONS

RA = Row Address

BA = Bank Address

NOP = No Operation command

CA = Column Address

AP = Auto Precharge

- Notes:
1. All inputs are enabled when CKE is set high for at least 1 cycle prior to the inputs.
 2. Illegal to bank in specified state, but may be legal in some cases depending on the state of bank selection.
 3. Satisfy the timing of t_{CCD} and t_{WR} to prevent bus contention.
 4. NOP to bank precharging or in idle state. Precharges activated bank by BA or A10.
 5. Illegal if any bank is not idle.

FUNCTION TRUTH TABLE for CKE (Table 2)

| Current State (n) | CKEn-1 | CKEn | CS | RAS | CAS | WE | ADDR | Action |
|--------------------------------------|--------|------|----|-----|-----|----|------|--------------------------------|
| Self Refresh | H | X | X | X | X | X | X | INVALID |
| | L | H | H | X | X | X | X | Exit Self Refresh --> ABI |
| | L | H | L | H | H | H | X | Exit Self Refresh --> ABI |
| | L | H | L | H | H | L | X | ILLEGAL |
| | L | H | L | H | L | X | X | ILLEGAL |
| | L | H | L | L | X | X | X | ILLEGAL |
| | L | L | X | X | X | X | X | NOP (Maintain Self Refresh) |
| Power Down | H | X | X | X | X | X | X | INVALID |
| | L | H | H | X | X | X | X | Exit Power Down --> ABI |
| | L | H | L | H | H | H | X | Exit Power Down --> ABI |
| | L | H | L | H | H | L | X | ILLEGAL |
| | L | H | L | H | L | X | X | ILLEGAL |
| | L | H | L | L | X | X | X | ILLEGAL ⁶ |
| | L | L | X | X | X | X | X | NOP (Continue power down mode) |
| All Banks Idle ⁶ (ABI) | H | H | X | X | X | X | X | Refer to Table 1 |
| | H | L | H | X | X | X | X | Enter Power Down |
| | H | L | L | H | H | H | X | Enter Power Down |
| | H | L | L | H | H | L | X | ILLEGAL |
| | H | L | L | H | L | X | X | ILLEGAL |
| | H | L | L | L | H | L | X | ILLEGAL |
| | H | L | L | L | L | H | X | Enter Self Refresh |
| | H | L | L | L | L | L | X | ILLEGAL |
| | L | L | X | X | X | X | X | NOP |
| Any State Other than Listed Above | H | H | X | X | X | X | X | Refer to Operations in Table 1 |
| | H | L | X | X | X | X | X | Begin Clock Suspend Next Cycle |
| | L | H | X | X | X | X | X | Enable Clock of Next Cycle |
| | L | L | X | X | X | X | X | Continue Clock Suspension |

Note: 6. Power-down and self refresh can be entered only when all the banks are in an idle state.