

HD153119

Color Palette with Triple 6-bit DA Converter

The HD153119FS/CP is a color palette with triple 6-bit DA converter. Manufactured with Hitachi's Hi-BiCMOS process, this LSI realizes high speed, high density, low power consumption and minimizes the need for externally connected parts. Also, in addition to applications for existing CRTs, the provision of digital R, G and B outputs for color LCD ensure that the HD153119 can easily accommodate future systems using full-color LCD. With color palette, advanced functions, small size and low cost, the HD153119 is an essential component for advanced graphics systems.

- In addition to existing CRT applications, direct digital RGB outputs from the color lookup table (CLT) are provided for color LCD applications.
- Variable BLACK level (0 or 7.5 IRE)
- Selectable composite or non-composite SYNC signal (composite is RGB three-channel)
- Dot rate maximum of 50/65 MHz
- Synchronous timing for pipeline control selectable between rise or fall of DOTCK.
- TTL compatible I/O levels

Features

- Displays 256 colors simultaneously from a total of 262,144 possible colors
- Three 6-bit DA converters for RGB video output on a single chip
- Pixel mask function for display control
- Compatible with personal system/2*
- For each pixel, dynamic switching between 262,144-color simultaneous display mode and normal mode.

Note: Personal System/2 is a registered trademark of IBM corporation.

Ordering Information

Type No.	Max. Operating Freq.	Package
HD153119FS	50 MHz	80 pin plastic
HD153119FS-65	65 MHz	QFP (FP-80B)
HD153119CP	50 MHz	68 pin plastic
HD153119CP-65	65 MHz	QFJ (CP-68)

Pin Arrangement

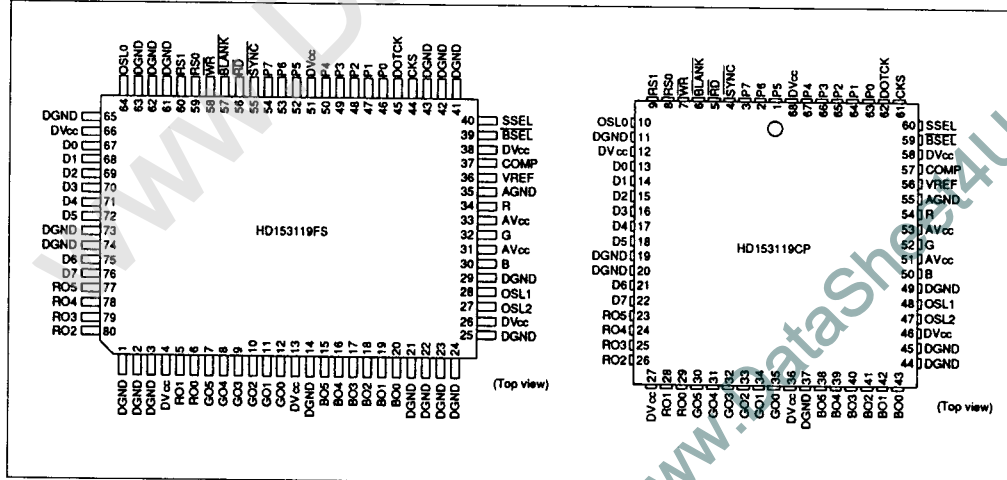
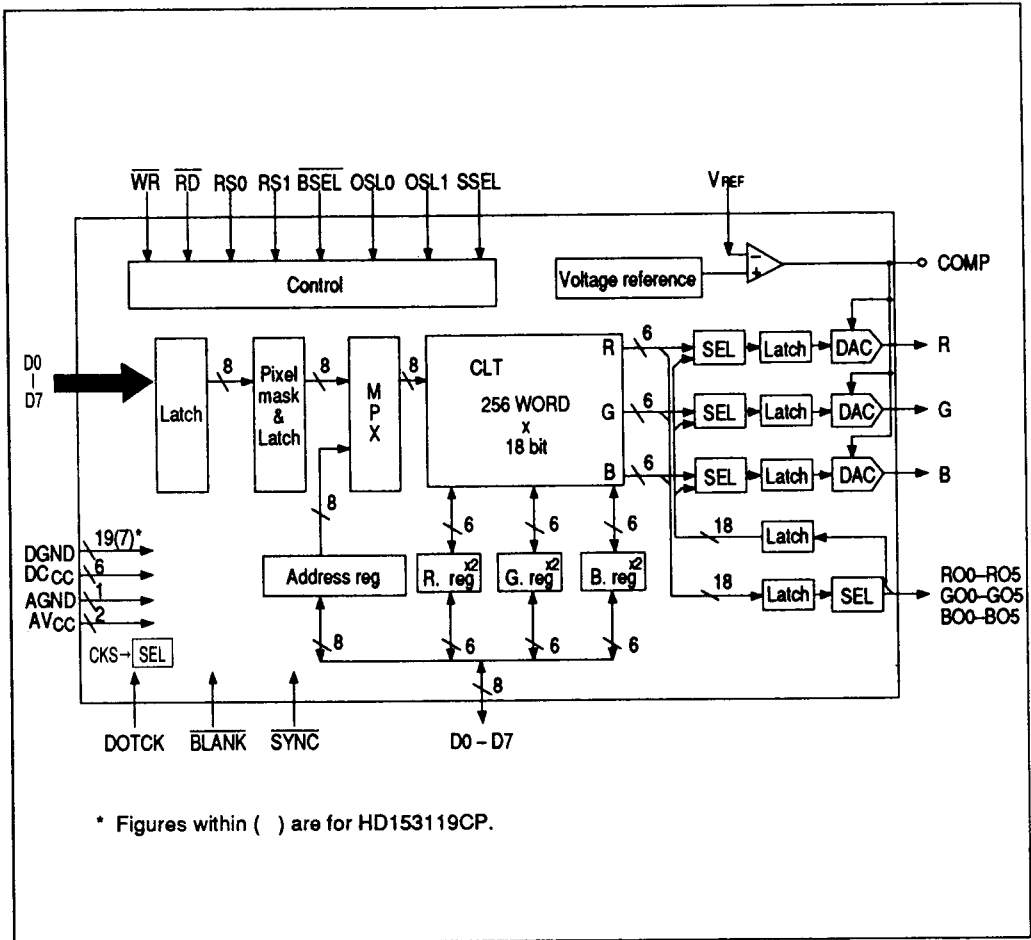


Figure 1 Pin Arrangement

Block Diagram



2

Figure 2 Block Diagram

HD153119

Table 1 Pin Description

Pin name	Pin number *	Description
P0 – P7	46 – 50 52 – 54 (63 – 67, 1 – 3)	CLT address inputs. P7 is MSB. P0 is LSB.
D0 – D7	67 – 72, 75, 76 (13 – 18, 21, 22)	Data port for reading/writing CLT or address, pixel mask, R, G and B registers. D7 is MSB, D0 is LSB.
\overline{RD}	56 (5)	Read clock input. Strokes data from CLT or address, pixel mask, R, G or B registers during read operation.
\overline{WR}	58 (7)	Write clock input. Strokes data to CLT or address, pixel mask, R, G or B registers during write operation.
RS0, RS1	59, 60 (8, 9)	Select input for CLT, address register or pixel mask register.
RO0 – RO5 GO0 – GO5 BO0 – BO5	6, 5, 80 – 77 (29, 28, 26 – 23) 12 – 7 (35 – 30) 20 – 15 (43 – 38)	Palette (CLT) digital signal outputs. RO5, GO5 and BO5 are the MSBs and RO0, GO0, and BO0 are the LSBs.
VREF	36 (56)	Terminal for connecting reference resistor to set DAC analog output level.
COMP	37 (57)	Terminal for connecting a phase-compensation capacitor
OSL0, OSL1, OSL2	64, 28, 27 (10, 48, 47)	Select inputs for digital signal outputs.
R, G, B	34, 32, 30 (54, 52, 50)	DAC analog signal outputs.
\overline{BLANK}	57 (6)	Video blank input for activating blank signal levels at DAC analog outputs.
\overline{BSEL}	39 (59)	Input for selecting DAC BLANK level (0 or 7.5 IRE)
DOTCK	45 (62)	Reference clock input for digital and analog sections. On the rise of this signal, CLT, BLANK and SYNC operations are processed and analog signal outputs become active.
CKS	44 (61)	Input for selecting active polarity of DOTCK. When CKS = 'L' operations occur on DOTCK rise. When CKS = 'H' operations occur on DOTCK fall.

* Upper pin numbers are for HD153119FS. Lower pin numbers within () are for HD153119CP.

Pin Description (cont)

Pin name	Pin number *	Description
SSEL	40 (60)	Input for selecting composite or non-composite SYNC signal. Composite when SSEL = 'H' and non-composite when SSEL = 'L'. For composite, the SYNC level is 0 IRE, blank level is 40 IRE and the WHITE level is 140 IRE.
DVCC	4, 13, 26, 38, 51, 66 (12, 27, 36, 46, 58, 68)	Digital power supply
DGND	1 – 3, 14, 21 – 25 29, 41 – 43, 61 – 63, 65, 73, 74 (11, 19, 20, 37, 44, 45, 49)	Digital GND
AV _{CC}	31, 33 (51, 53)	Analog power supply
AGND	35 (55)	Analog GND

* Upper pin numbers are for HD153119FS. Lower pin numbers within () are for HD153119CP.

Functions

Accessing the CLT and Registers

The CLT and registers are selected with inputs RS0 and RS1 (see table 2).

Table 2 Register Selection

RS1	RS0	Selection
0	0	Address register (write mode)
1	1	Address register (read mode)
0	1	CLT
1	0	Pixel mask register



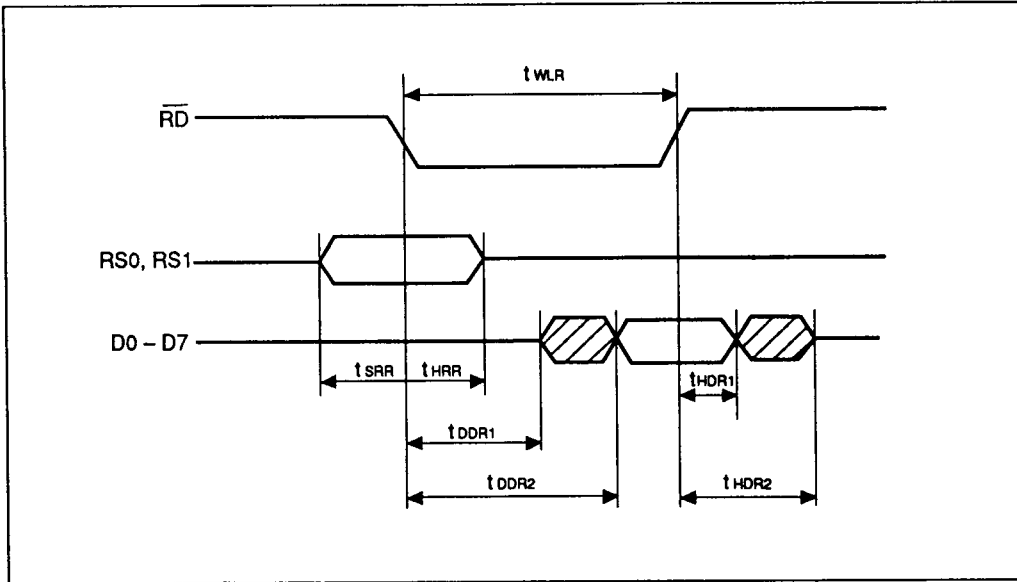
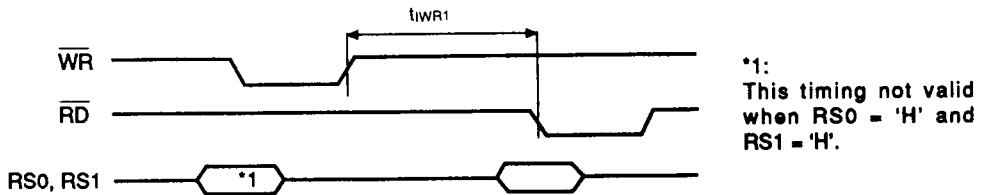


Figure 4 Read Timing

Applies to all read-after-write operations except when the write operation is placing a read address in the address register.



Applies to the case when the write operation is placing a read address in the address register.

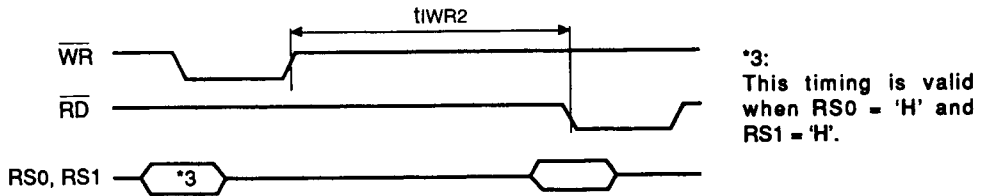


Figure 5 Read after Write

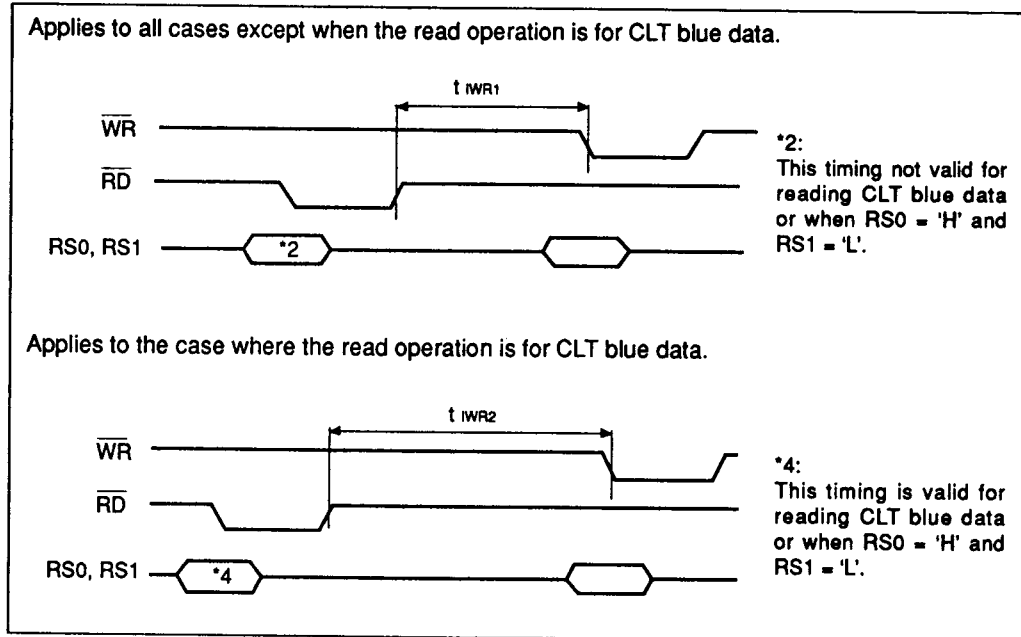


Figure 6 Write after Read

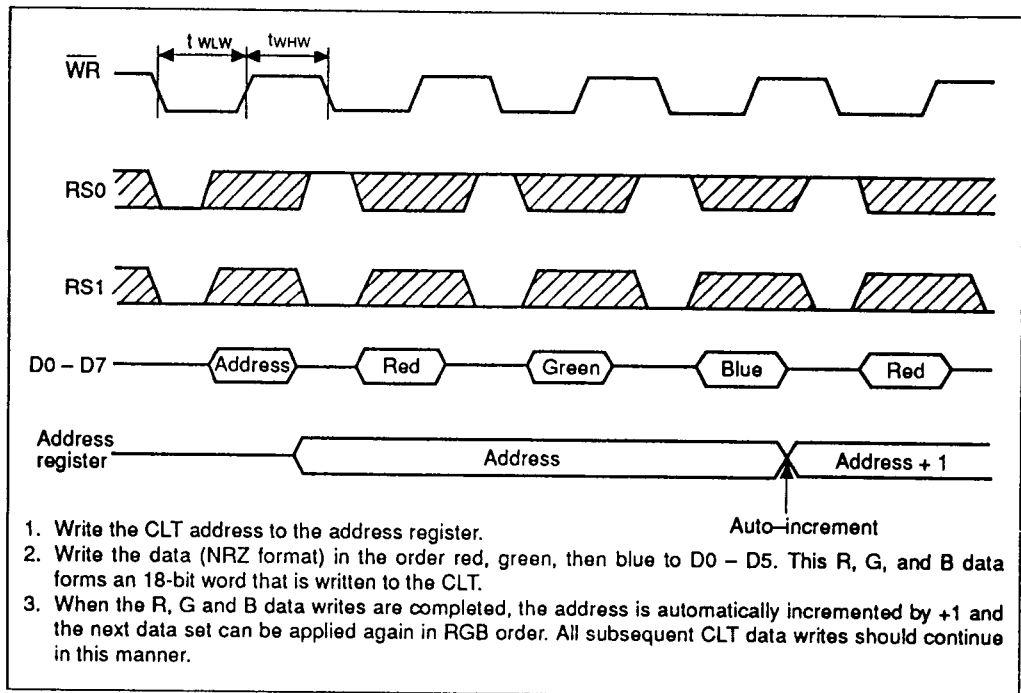


Figure 7 CLT Write

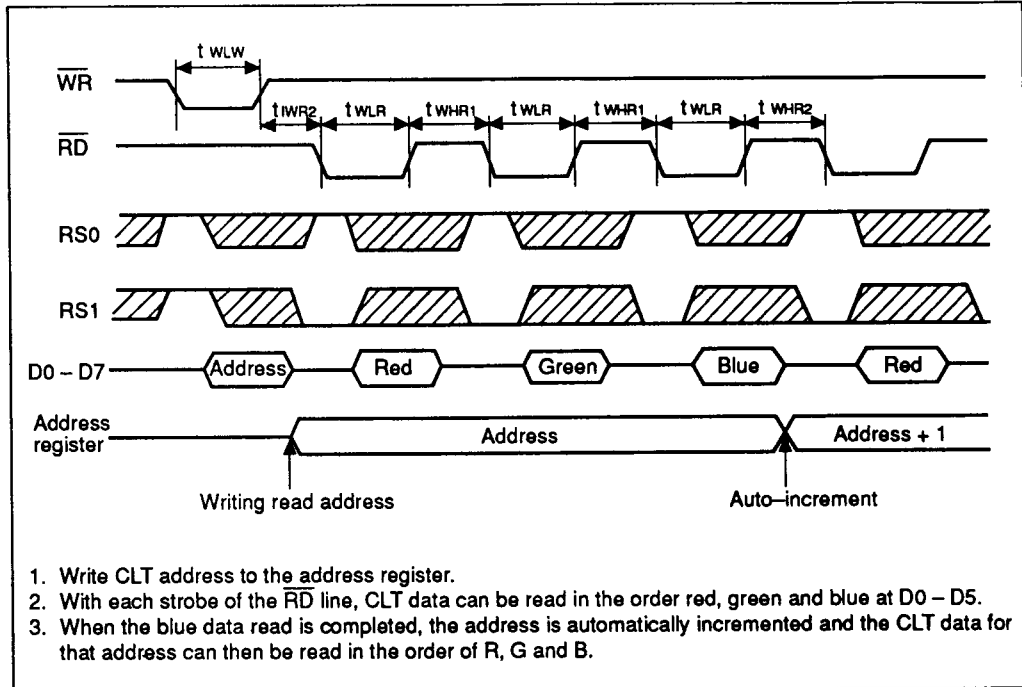


Figure 8 CLT Read

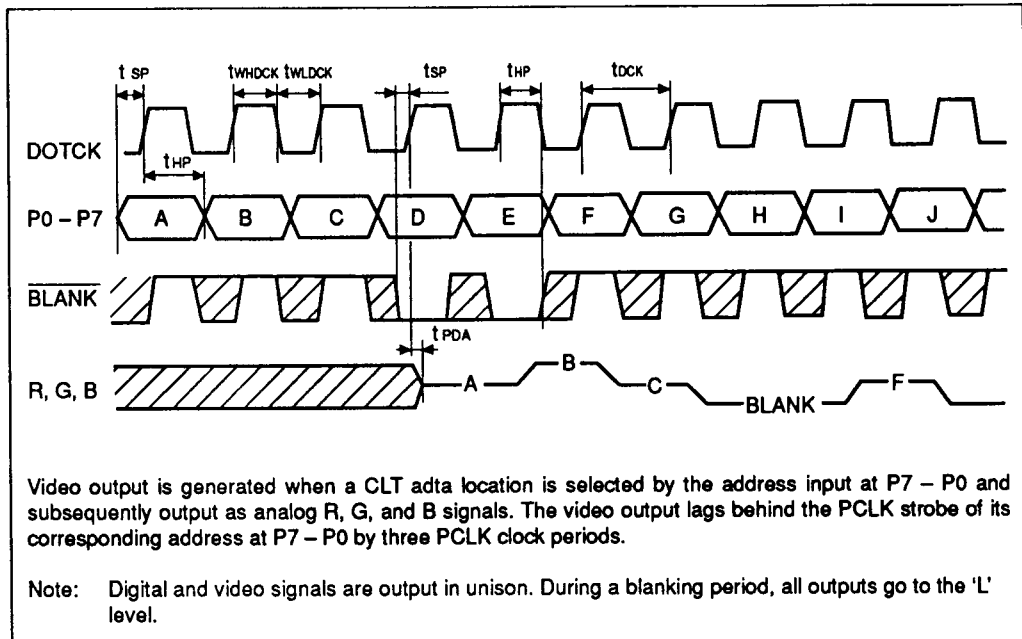


Figure 9 Video Output



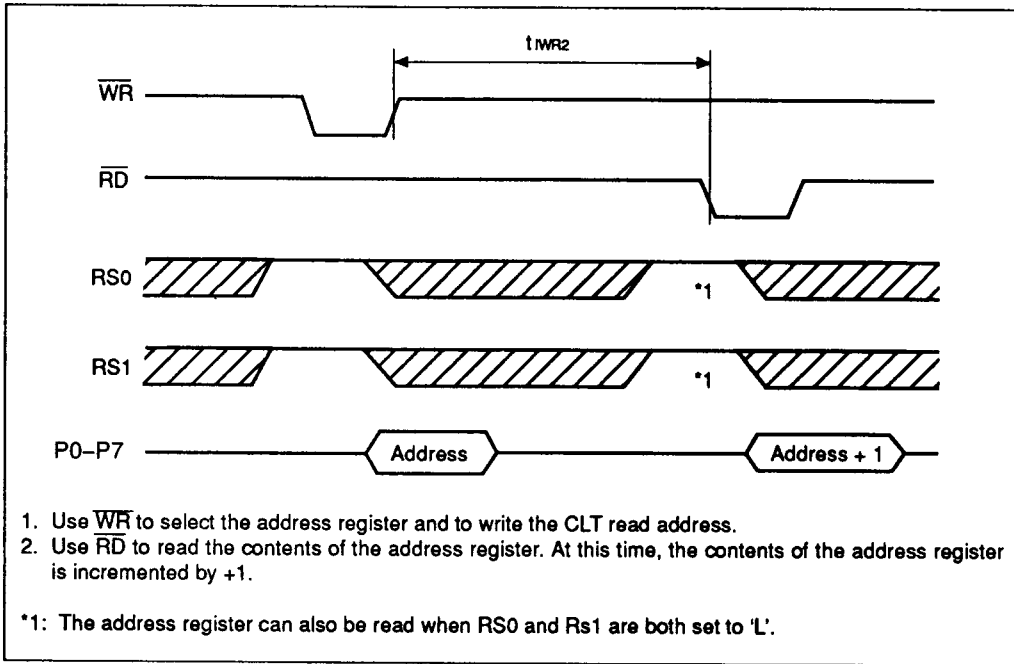


Figure 10 Address Register Read (1)

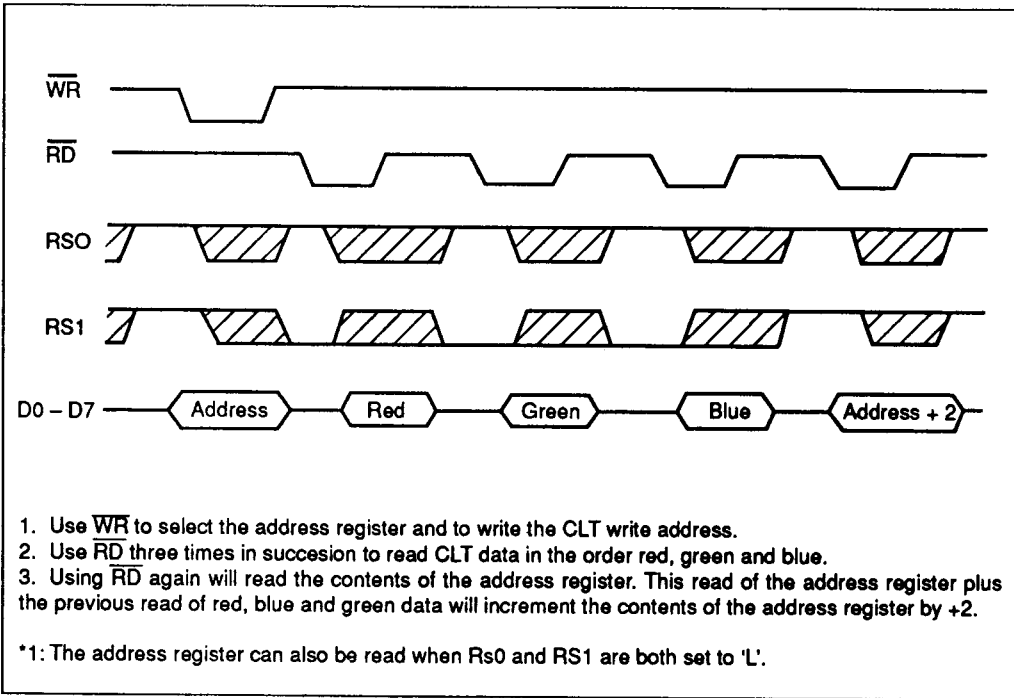


Figure 11 Address Register Read (2)



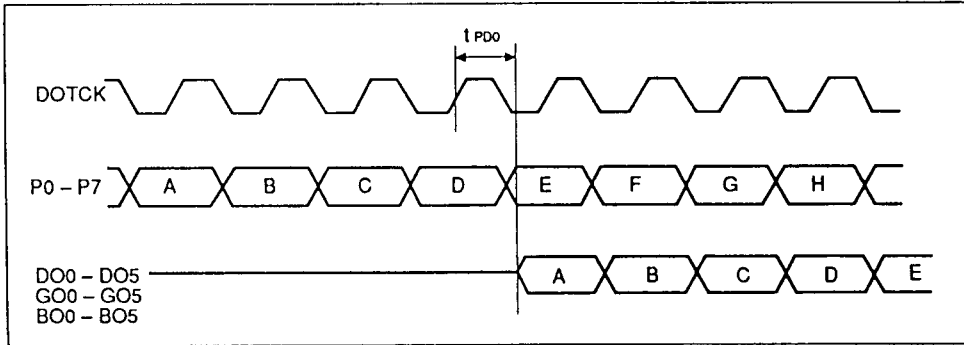


Figure 12 Digital Output

2

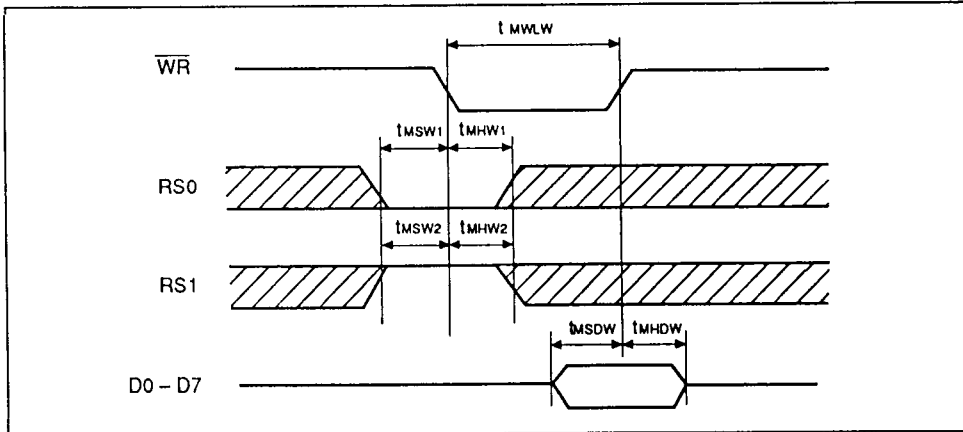


Figure 13 Pixel Mask Register Write

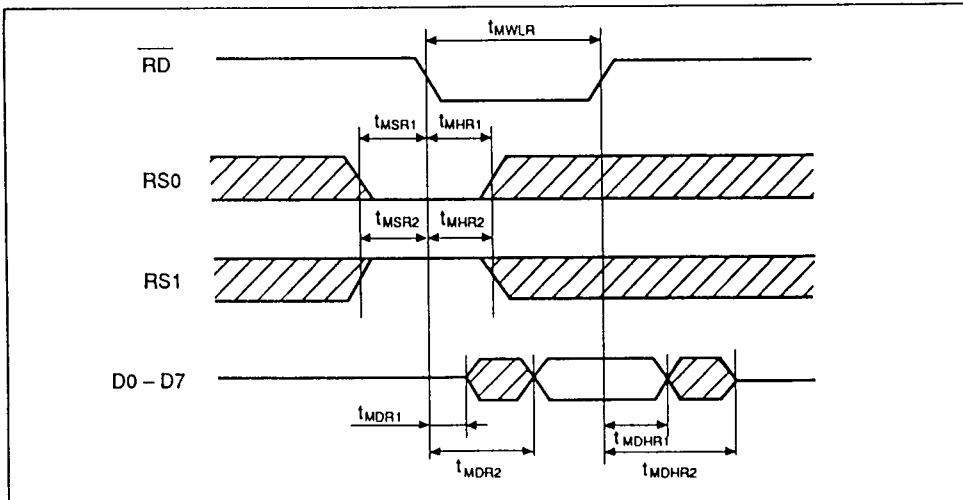
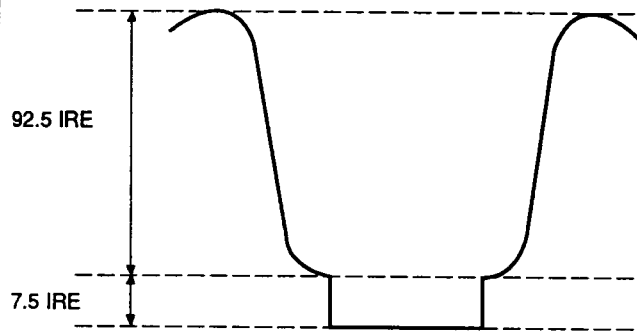


Figure 14 Pixel Mask Register Read

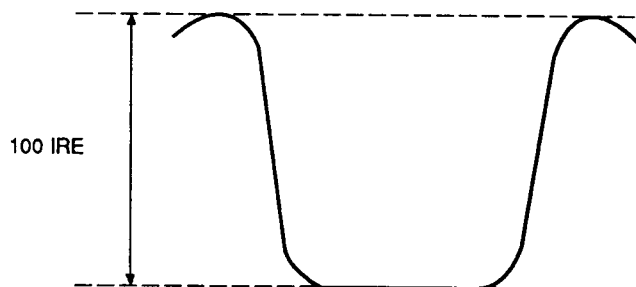
Video Output Waveforms

White level	0.698 V
Black level	0.054 V
Blank level	0.000 V



(SSEL = 'L', $\overline{\text{BSEL}}$ = 'L', $R_{\text{VREF}} = 13 \text{ k}\Omega$)

White level	0.698 V
Black/blank level	0.000 V



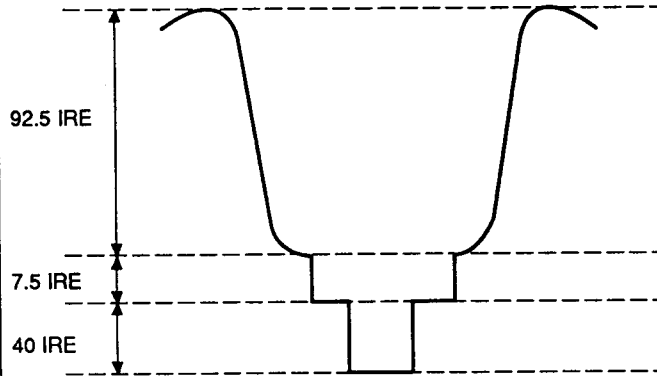
(SSEL = 'L', $\overline{\text{BSEL}}$ = 'H', $R_{\text{VREF}} = 12 \text{ k}\Omega$)

Figure 15 Video Output Waveforms

Video Output Waveforms (for composite SYNC signal)

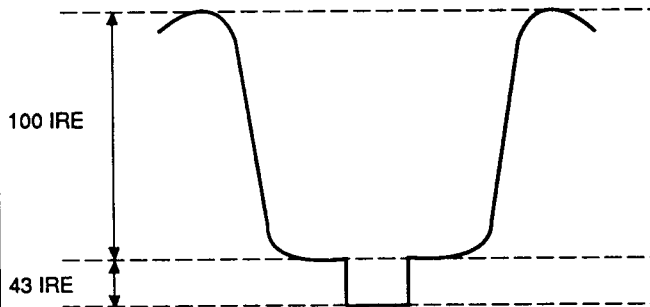
2

White level	1.000 V
Black level	0.340 V
Blank level	0.286 V
Sync level	0.000 V



(SSEL = 'H', $\overline{\text{BSEL}}$ = 'L', $R_{VREF} = 13 \text{ k}\Omega$)

White level	1.000 V
Black/blank level	0.302 V
Sync level	0.000 V



(SSEL = 'H', $\overline{\text{BSEL}}$ = 'H', $R_{VREF} = 12 \text{ k}\Omega$)

Figure 16 Video Output Waveforms (for composite SYNC signal)

Mode Switching

HD153110 operating mode is switched as shown table 3.

Table 3 Mode Switching

OSL2	OSL1	OSL0	Operating mode	Note
L	L	L	DAC output mode	1
L	L	H	DAC direct input (262,144-color simultaneous display mode)	1
L	H	L	Digital output 12-bit mode (R, G and B are output on upper 4 bits)	2
L	H	H	Prohibited (Digital output 18-bit mode)	3
H	L	L	Digital output 6-bit mode (Green output only)	2
H	L	H	Prohibited	
H	H	L	Digital output 18-bit mode	2
H	H	h	Prohibited	

- Notes:
1. Digital output is Hi-Z.
 2. DAC outputs are off.
 3. Both digital and DAC outputs are active.

Register Correspondence with CLT

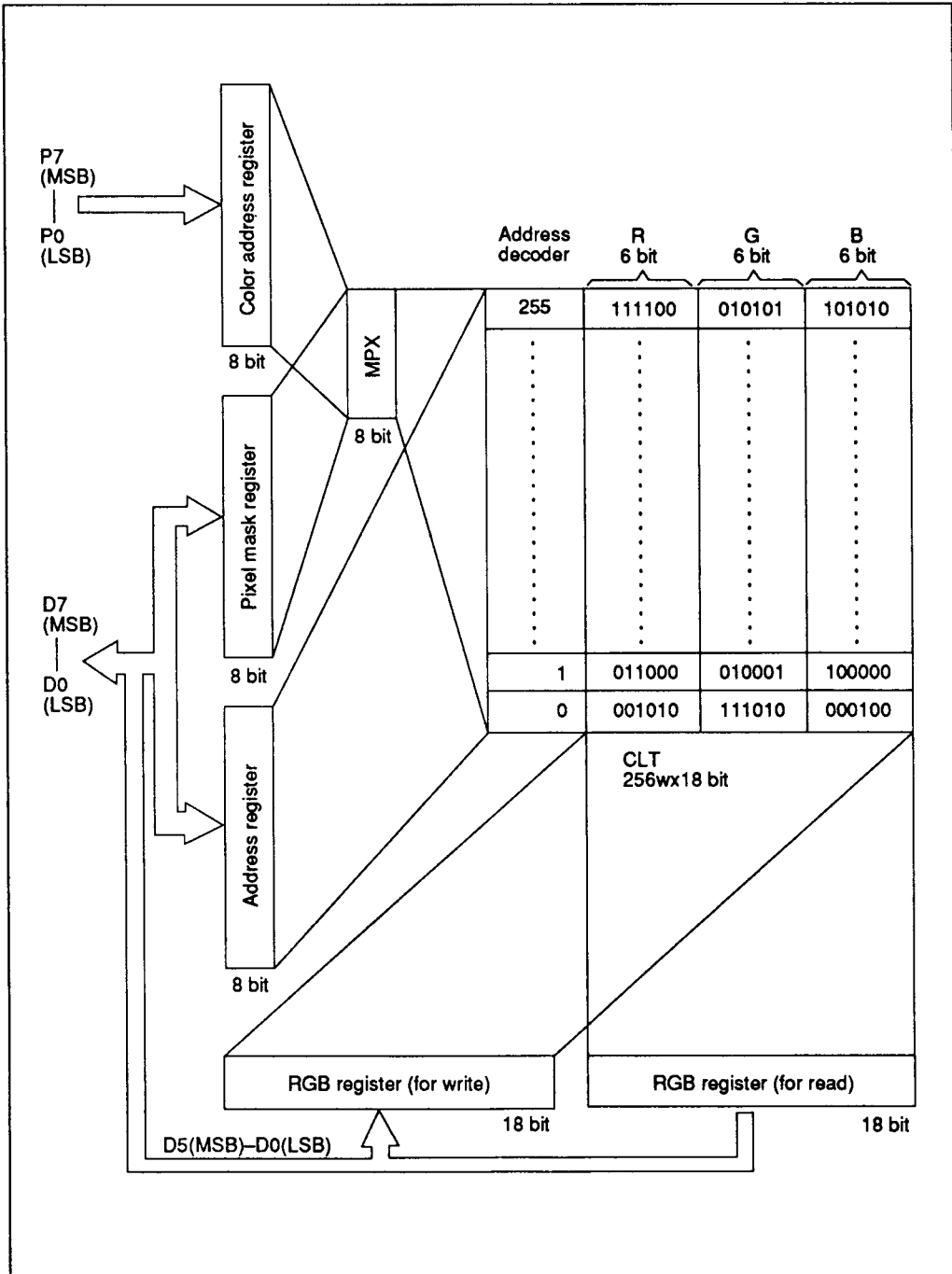


Figure 17 Register Correspondence with CLT

System Configuration Example

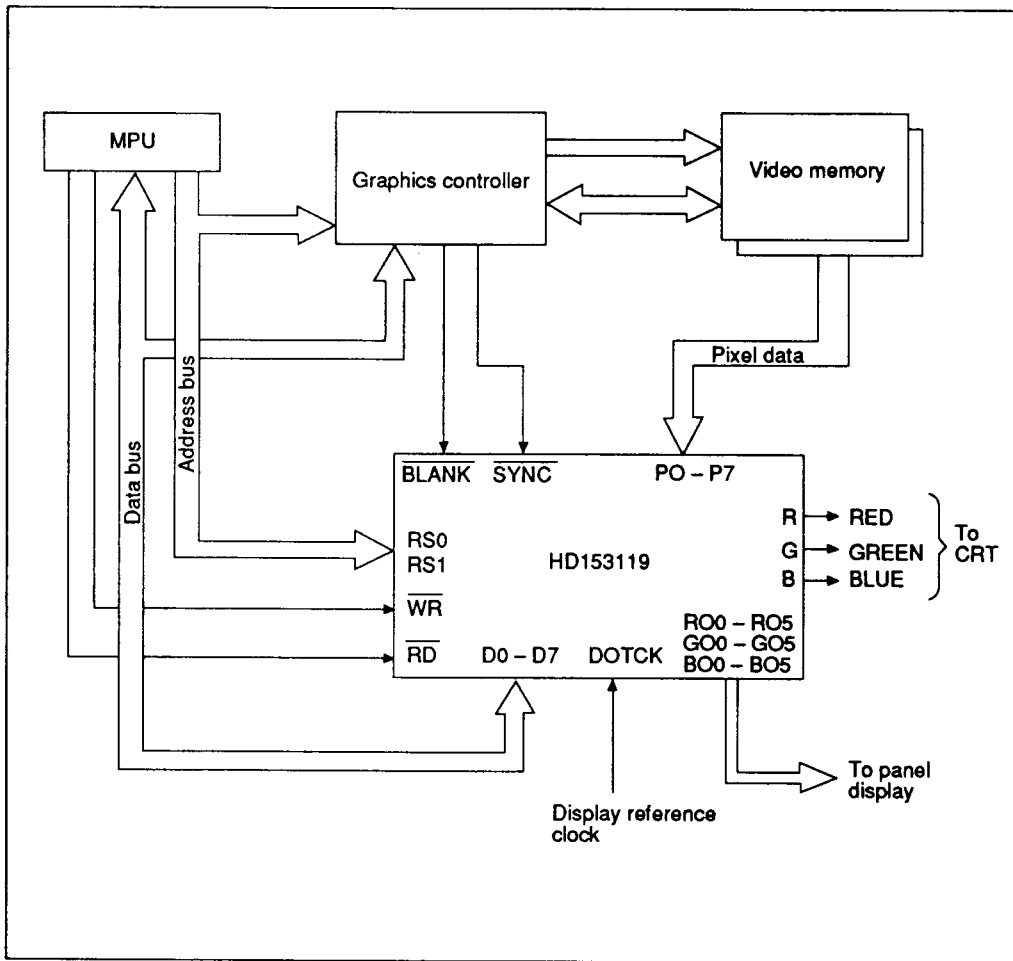


Figure 18 System Configuration Example

Table 4 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	7.0	V
Input voltage	V_{in}	0 to V_{CC}	V
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +150	°C

Electrical Characteristics

Table 5 DAC Section Electrical Characteristics ($V_{CC} = 5\text{ V}$, $T_a = 25\text{ }^\circ\text{C}$)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Resolution		6	6	6	bits	
Maximum operating frequency	f_{CLK}	—	—	50/65	MHz	
Analog output voltage	V_A (Full)	-15	—	15	% of FSR	
($R_{VREF} = 12\text{ k}\Omega$)	V_A (Zero)	-2	—	2	% of FSR	
Differential linearity	DLE	-1	—	+1	LSB	
Integral linearity	ILE	-1	—	+1	LSB	
Output rise time (20 to 80 %)	t_r	—	—	10	ns	$C_L = 15\text{ pF}$
Output fall time (80 to 20 %)	t_f	—	—	10	ns	$C_L = 15\text{ pF}$
Settling time	t_s	—	—	30	ns	$C_L = 15\text{ pF}$
Glitch energy	E_G	—	90	—	PVS	

Table 6 Digital section DC Characteristics (unless otherwise specified $V_{CC} = 5\text{ V} \pm 5\%$, $T_a = 0 \sim 70\text{ }^\circ\text{C}$)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input "High" level voltage	V_{IH}	2.0	—	V_{CC}	V	
Input "Low" level voltage	V_{IL}	-0.3	—	0.8	V	
Input clamp voltage	V_I	—	—	-1.5	V	$V_{CC} = 4.75\text{ V}$ $I_{IN} = -18\text{ mA}$
Output "High" level voltage	V_{OH}	2.7	—	—	V	$V_{CC} = 4.75\text{ V}$ $I_{OH} = -400\text{ }\mu\text{A}$
Output "Low" level voltage	V_{OL}	—	—	0.5	V	$V_{CC} = 4.75\text{ V}$ $I_{OL} = 8\text{ mA}$
Input current	I_I	—	—	1	mA	$V_{CC} = 5.25\text{ V}$ $V_I = 5.5\text{ V}$
"High" level input current	I_{IH}	—	—	20	μA	$V_{CC} = 5.25\text{ V}$ $V_I = 2.7\text{ V}$
"Low" level input current	I_{IL}	—	—	-400	μA	$V_{CC} = 5.25\text{ V}$ $V_I = 0.4\text{ V}$
Supply current (1) *1	$I_{CC} (1)$	—	130	190	mA	$V_{CC} = 5.25\text{ V}$
Supply current (2) *2	$I_{CC} (2)$	—	110	160	mA	$V_{CC} = 5.25\text{ V}$

Notes: 1. OSL0 = 'L', OSL1 = 'L', OSL2 = 'L'
2. OSL0 = 'L', OSL1 = 'H', OSL2 = 'H'

Table 7 Digital Section AC Characteristics ($V_{CC} = 5\text{ V}$, $T_a = 25\text{ }^\circ\text{C}$)

Item	Symbol	50 MHz		65 MHz		Unit	Test conditions	Reference figure
		Min	Max	Min	Max			
DOTCK cycle time	t_{DCK}	20	—	15.3	—	ns		9
DOTCK low level time	t_{WLDCK}	8	—	6	—	ns		9
DOTCK high level time	t_{WHDCK}	8	—	6	—	ns		9
Data setup time	t_{SP}	6	—	5	—	ns		9
Data hold time	t_{HP}	6	—	5	—	ns		9
Data output delay time	t_{PDA}	—	30	—	30	ns	$C_L = 15\text{ pF}$	9
\overline{WR} low level time	t_{WLW}	50	—	50	—	ns		3, 7, 8
\overline{WR} high level time	t_{WHW}	$3 \times t_{DCK}$	—	$3 \times t_{DCK}$	—	ns		4, 8
\overline{RD} low level time	t_{WLR}	50	—	50	—	ns		8
\overline{RD} high level time (1)	t_{WHR1}	$3 \times t_{DCK}$	—	$3 \times t_{DCK}$	—	ns		8
\overline{RD} high level time (2)	t_{WHR2}	$6 \times t_{DCK}$	—	$6 \times t_{DCK}$	—	ns		8
$\overline{WR}/\overline{RD}$ interval time (1)	t_{WR1}	$3 \times t_{DCK}$	—	$3 \times t_{DCK}$	—	ns		5, 6
$\overline{WR}/\overline{RD}$ interval time (2)	t_{WR2}	$6 \times t_{DCK}$	—	$6 \times t_{DCK}$	—	ns		5, 6, 8, 9
$\overline{WR}/RS0$, RS1 setup time	t_{SW}	10	—	10	—	ns		3
$\overline{WR}/RS0$, RS1 hold time	t_{HW}	10	—	10	—	ns		3
$\overline{RD}/RS0$, RS1 setup time	t_{SRR}	10	—	10	—	ns		4
$\overline{RD}/RS0$, RS1 hold time	t_{HRR}	10	—	10	—	ns		4
\overline{WR} data setup time	t_{SDW}	10	—	10	—	ns		3
\overline{WR} data hold time	t_{HDW}	10	—	10	—	ns		3
\overline{RD} data output delay time (1)	t_{DDR1}	5	—	5	—	ns	$C_L = 15\text{ pF}$	4
\overline{RD} data output delay time (2)	t_{DDR2}	—	40	—	40	ns	$C_L = 15\text{ pF}$	4
\overline{RD} data output hold time (1)	t_{HDR1}	5	—	5	—	ns	$C_L = 15\text{ pF}$	4
\overline{RD} data output hold time (2)	t_{HDR2}	—	20	—	20	ns	$C_L = 15\text{ pF}$	4
Digital output delay time	t_{PDO}	—	19	—	19	ns	$C_L = 15\text{ pF}$	12
\overline{WR} low level time	t_{MWLW}	50	—	50	—	ns		13
\overline{RD} low level time	t_{MWLR}	50	—	50	—	ns		14

Digital Section AC Characteristics ($V_{CC} = 5\text{ V}$, $T_a = 25\text{ }^\circ\text{C}$) (cont)

Item	Symbol	50 MHz		65 MHz		Unit	Test conditions	Reference figure
		Min	Max	Min	Max			
$\overline{WR}/RS0$, RS1 setup time	t_{MSW1}	10	—	10	—	ns		13
	t_{MSW2}	10	—	10	—	ns		13
$\overline{WR}/RS0$, RS1 hold time	t_{MHW1}	10	—	10	—	ns		13
	t_{MHW2}	10	—	10	—	ns		13
$\overline{RD}/RS0$, RS1 setup time	t_{MSR1}	10	—	10	—	ns		14
	t_{MSR2}	10	—	10	—	ns		14
$\overline{RD}/RS0$, RS1 hold time	t_{MHR1}	10	—	10	—	ns		14
	t_{MHR2}	10	—	10	—	ns		14
\overline{WR} data setup time	t_{MSDW}	10	—	10	—	ns		13
\overline{WR} data hold time	t_{MHDW}	10	—	10	—	ns		13
\overline{RD} data output delay time	t_{MDR1}	5	—	5	—	ns	$C_L = 15\text{ pF}$	14
	t_{MDR2}	—	40	—	40	ns	$C_L = 15\text{ pF}$	14
RD data output hold time	t_{MDHR1}	5	—	5	—	ns	$C_L = 15\text{ pF}$	14
	t_{MDHR2}	—	20	—	20	ns	$C_L = 15\text{ pF}$	14

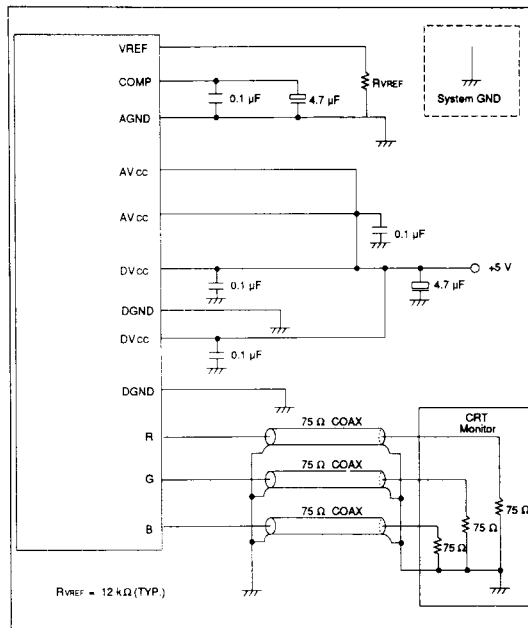


Figure 19 Connection Example

