

Data Sheet July 1999 File Number 2875.2

2A, 200V, 3.500 Ohm, Logic Level, N-Channel Power MOSFET

The RFP2N20L N-Channel enhancement mode silicon gate power field effect transistor is specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

Formerly developmental type TA09532.

Ordering Information

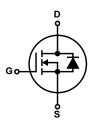
PART NUMBER	PACKAGE	BRAND
RFP2N20L	TO-220AB	RFP2N20L

NOTE: When ordering, include the entire part number.

Features

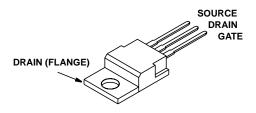
- 2A, 200V
- $r_{DS(ON)} = 3.500\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power Dissipation Limited
- · Nanosecond Switching Speeds
- · Linear Transfer Characteristics
- · High Input Impedance
- Majority Carrier Device
- · Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC TO-220AB



RFP2N20L

Absolute Maximum Ratings $T_C = 25^{\circ}C$, Unless Otherwise Specified

	RFP2N20L	UNITS
Drain to Source Voltage (Note 1)V _{DSS}	200	V
Drain to Gate Voltage R_{GS} = 20K Ω (Note 1)	200	V
Gate to Source Voltage	±10	V
Drain Current, RMS Continuous	2	Α
Pulsed (Note 3) I _{DM}	4	Α
Maximum Power Dissipation	25	W
Derate Linearly Above T _C = 25 ^o C	0.2	W/ °C
Operating and Storage Temperature	-55 to 150	°C
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10s	300 260	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}C$ to $125^{\circ}C$.

Electrical Specifications $T_C = 25^{\circ}C$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV _{DSS}	$I_D = 250\mu A, V_{GS} = 0V$	200	-	-	V
Gate to Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA	1	-	2	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = Rated BV _{DSS} , V _{GS} = 0V	-	-	1	μА
		V_{DS} = 0.8 x Rated BV _{DSS} , V_{GS} = 0V, T_C = 125°C	-	-	25	μА
Gate to Source Leakage Current	I _{GSS}	$V_{GS} = \pm 10V, V_{DS} = 0$	-	-	±100	nA
Drain to Source On Voltage (Note 2)	V _{DS(ON)}	I _D = 2A, V _{GS} = 5V	-	-	7	V
Drain to Source On Resistance (Note 2)	r _{DS(ON)}	I _D = 2A, V _{GS} = 5V (Figures 6, 7)	-	-	3.500	Ω
Turn-On Delay Time	t _{d(ON)}	I_D = 2A, V_{DD} = 100V, R_G = 6.25 Ω , V_{GS} = 5V R_L = 50 Ω (Figures 10, 11, 12)	-	10	25	ns
Rise Time	t _r		-	10	30	ns
Turn-Off Delay Time	t _d (OFF)		-	25	40	ns
Fall Time	t _f		-	20	25	ns
Input Capacitance	C _{ISS}	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1MHz$ (Figure 9)	-	-	200	pF
Output Capacitance	Coss		-	-	60	pF
Reverse Transfer Capacitance	C _{RSS}	_	-	-	35	pF
Thermal Resistance Junction to Case	$R_{ heta JC}$		-	-	5	°C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V _{SD}	I _{SD} = 2A	-	-	1.4	V
Reverse Recovery Time	t _{rr}	$I_{SD} = 2A$, $dI_{SD}/dt = 50A/\mu s$	-	200	-	ns

NOTES:

- 2. Pulsed: pulse duration = $300\mu s$ max, duty cycle = 2%.
- 3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

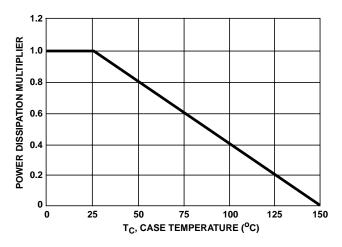


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

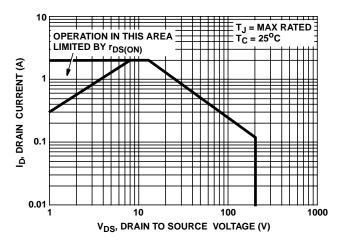


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

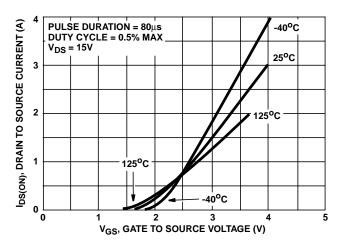


FIGURE 5. TRANSFER CHARACTERISTICS

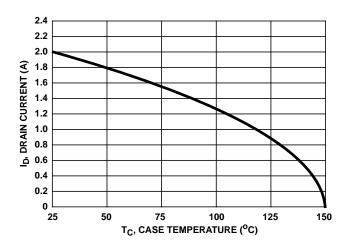


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

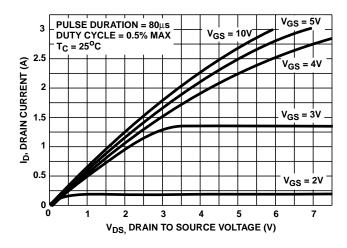


FIGURE 4. SATURATION CHARACTERISTICS

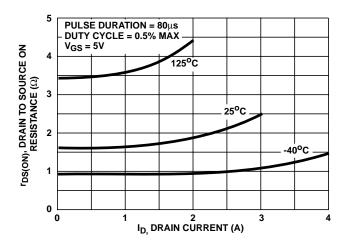


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE VS DRAIN CURRENT

Typical Performance Curves Unless Otherwise Specified (Continued)

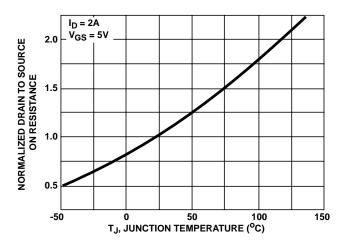


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

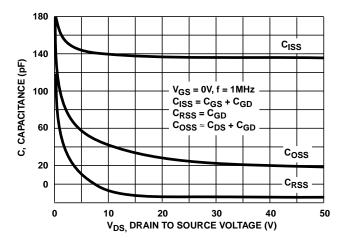


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

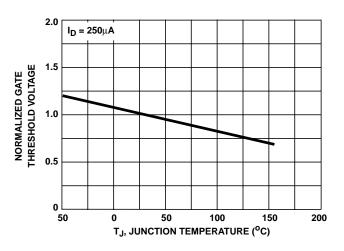
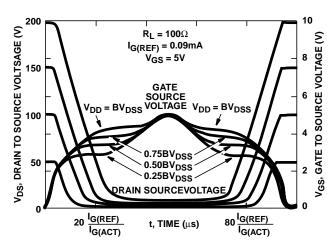


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE



NOTE: Refer to Intersil Applications Notes AN7254 and AN7260
FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR
CONSTANT GATE CURRENT

Test Circuits and Waveforms

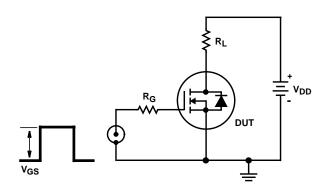


FIGURE 11. SWITCHING TIME TEST CIRCUIT

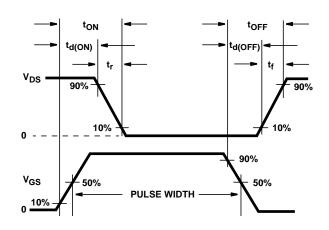


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS

RFP2N20L

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