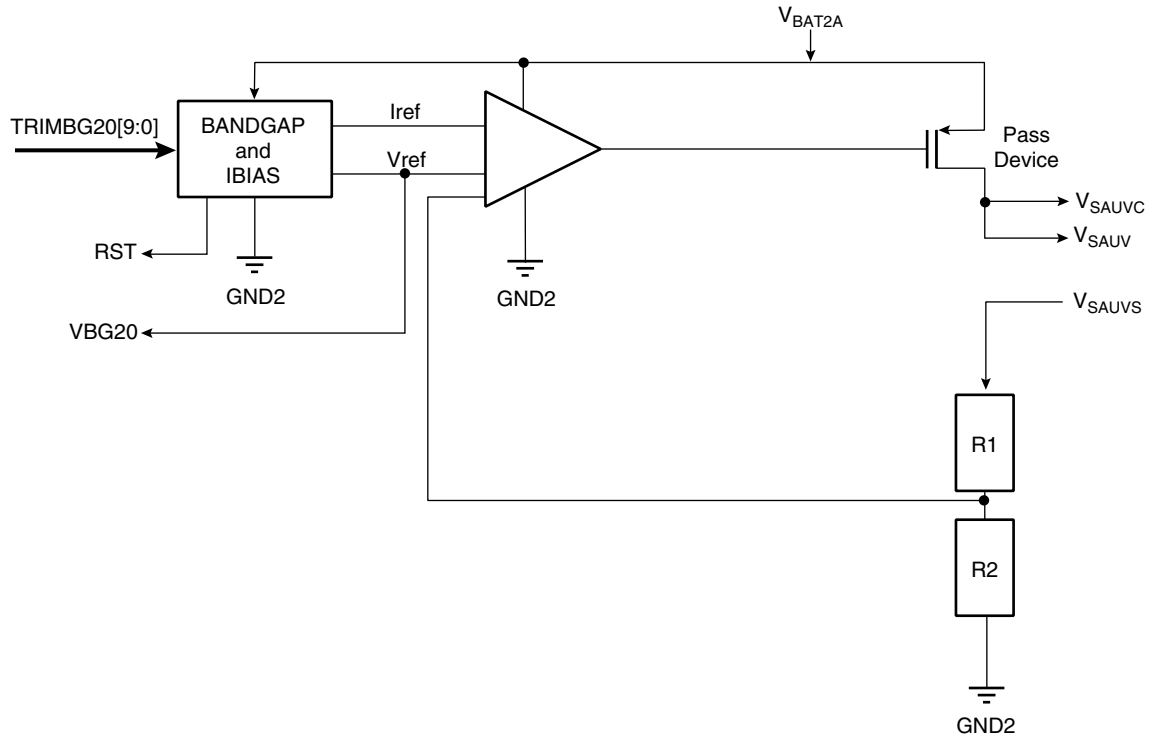


Functional Diagram

Figure 2. Functional Diagram



Pin Description

Pin Name	I/O	Type	Function	Value
V_{BAT2A}	Power supply	External pad	Power supply	3V to 5.5V
V_{SAUV}	Analog output	External pad	Output voltage	2.4V to 2.6V
V_{SAUVS}	Analog input	External pad	Sense voltage	2.4V to 2.6V
V_{SAUVC}	Analog output	Internal pin	Output voltage	2.4V to 2.6V
GND2	Ground	Internal pin	Ground	0
TRIMBG20	Digital bus	Internal pin	Bandgap Reference Trimming	0 to V_{SAUV}
RST	Digital output	Internal pin	POR signal	0 to V_{SAUV}
VBG20	Analog output	Internal pin	Voltage reference	1.231V

RE031 2.5V 5 mA LDO Voltage Regulator

Absolute Maximum Ratings*

V_{IN}	-0.3V to 6.5V
Digital Signals.....	-0.3V to 5.5V
Output Current.....	Internally Limited
Junction Temperature	-20°C to 150°C

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Specifications⁽¹⁾

T_A = -20°C to +85°C, supply voltage = 3V to 5.5V unless otherwise specified, output capacitance = 2.2 μ F.

Table 1. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	
V_{SAUVC}	Auxiliary Operating Supply Voltage		2.4	2.5	2.6	V	
V_{SAUV}	Output Voltage		2.4	2.5	2.6	V	
I_{SAUV}	Output Current				5	mA	
I_{QQ}	Quiescent Current				10	μ A	
ΔV_{DC}	Line Regulation	$V_{BAT2} = 3V$ to 3.4V $I_{SAUV} = 5$ mA		12		mV	
ΔV_{TRAN}	Transient Line Regulation	$V_{BAT2} = 3V$ to 3.4V $I_{SAUV} = 5$ mA rise time = fall time = 5 μ s		37		mV	
ΔV_{DC}	Load Regulation	10% - 90% of max I_{SAUV}		10.3		mV	
ΔV_{TRAN}	Transient Load Regulation	10% - 90% of max I_{SAUV} rise time = fall time = 5 μ s		5		mV	
PSRR	Power Supply Rejection Ratio at Full Load	$V_{BAT} = 3V$	@ 100 Hz	-54		-55	dB
			@ 1 kHz	-34		-35	dB
			@ 20 kHz	-12		-12	dB
			@ 100 kHz	-12		-16	dB
		$V_{BAT} = 4.25V$	@ 100 Hz	-43		-55	dB
			@ 1 kHz	-33		-35	dB
			@ 20 kHz	-12		-14	dB
			@ 100 kHz	-10		-15	dB
		$V_{BAT} = 5.5V$	@ 100 Hz	-35		-45	dB
			@ 1 kHz	-32		-36	dB
			@ 20 kHz	-13		-14	dB
			@ 100 kHz	-9		-14	dB
V_N	Output Noise	Bandwidth = 10 Hz to 100 kHz; output current = 5 mA		1051		μ V _{RMS}	
I_{SD}	Shut Down Current				1	μ A	

Note: 1. Obtained by considering the parasitics of a TFBGA100 Package.

Control Modes

Trimming

The bandgap inside RE031 has trimming capability, i.e., it is possible to compensate the bandgap resistance variations due to process gradients through the TRIMBG20[9:0] signal. In order to reduce the sensitivity of the bandgap voltage to resistance variations, the trimming has been designed to compensate up to $\pm 40\%$ of resistance variations.

Table 2. Truth Table

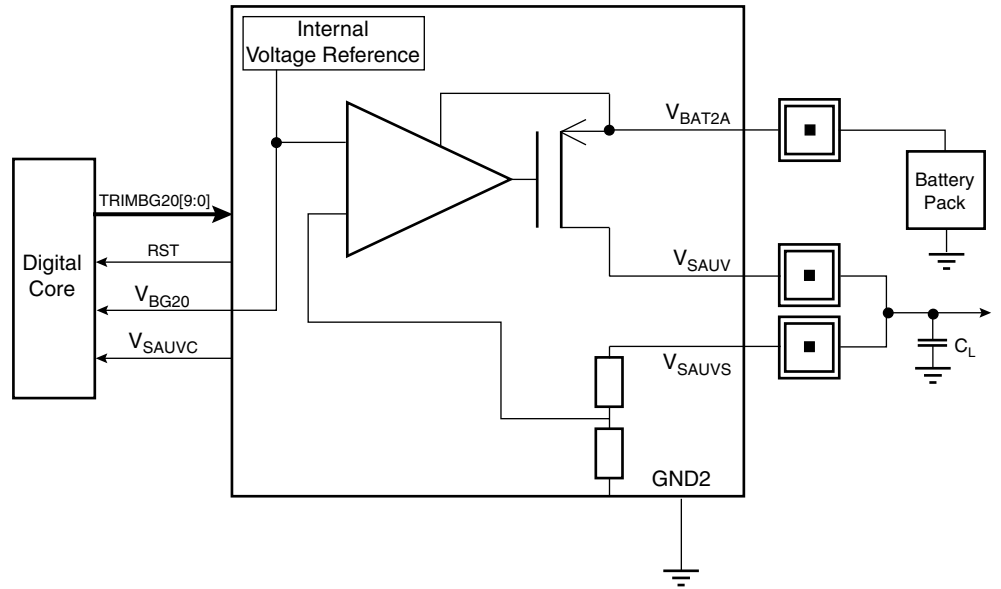
Resistance Variation	TRIMBG20[9:0]
+35% to +40%	1001000000
+20% to +35%	0101000000
+5% to +25%	0011000000
-5% to +5%	0000000000
-15% to -5%	0001100000
-22.5% to -15%	0001010000
-27.5% to -22.5%	0001001000
-32.5% to -27.5%	0001000100
-35% to -32.5%	0001000010
-37.5% to -35%	0001000001
-40% to -37.5%	0001000000

Application Example

A ceramic capacitor of 2.2 μF with ESR between 20 $\text{m}\Omega$ and 250 $\text{m}\Omega$ connected from V_{SAUV} to ground is needed for external compensation.

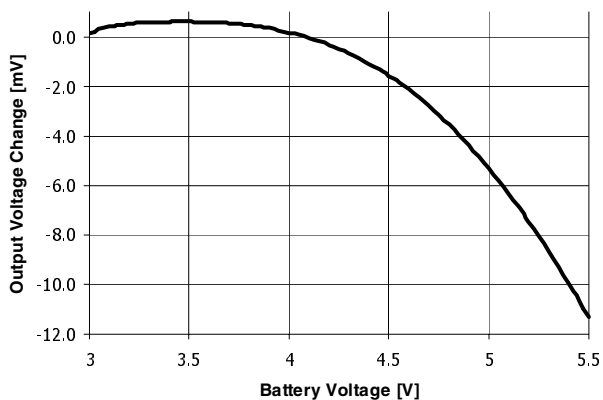
Description	Min	Typ	Max	Units
Capacitor (C_L)	1.8	2.2	2.6	μF

Figure 3. Application Example

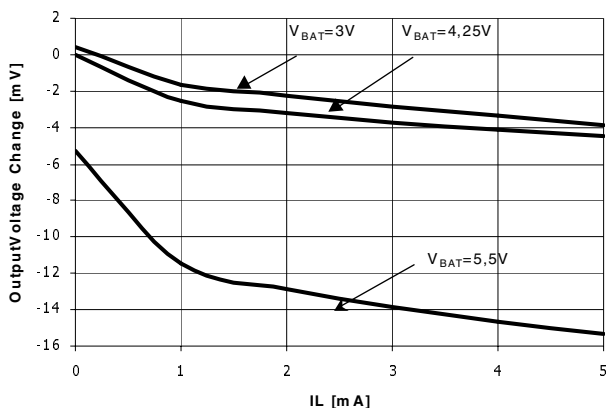


Typical Performance Characteristics (Conditions specified on page 8.)

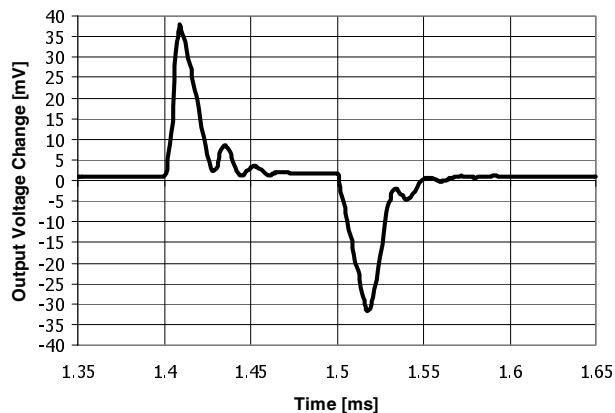
Static Line Regulation at Full Load



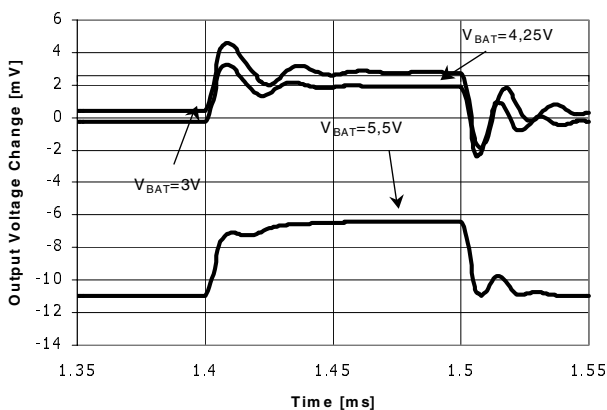
Static Load Regulation



Transient Line Regulation at Full Load



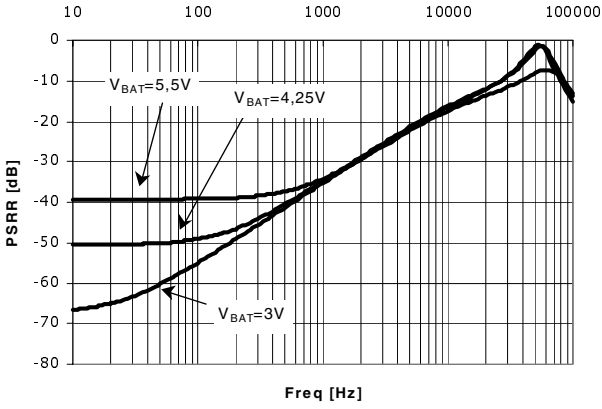
Transient Load Regulation



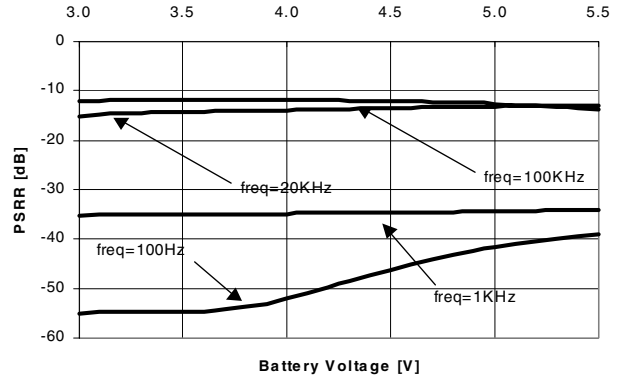
RE031 2.5V 5 mA LDO Voltage Regulator

Typical Performance Characteristics (Conditions specified on page 8.)

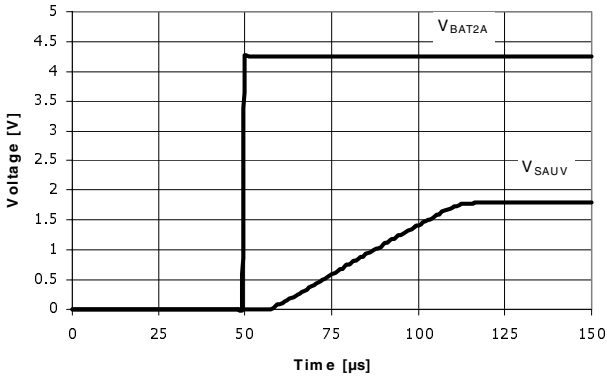
Power Supply Rejection Ratio at Full Load



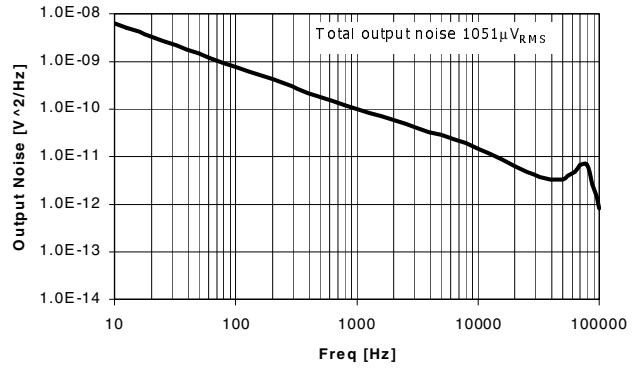
Power Supply Rejection Ratio at Full Load Versus Battery Voltage in Low Power Mode



LDO Startup at Full Load for Vbat = 4.25V in Low Power Mode



Output Noise Spectrum at Full Load and Vbat=4.25V

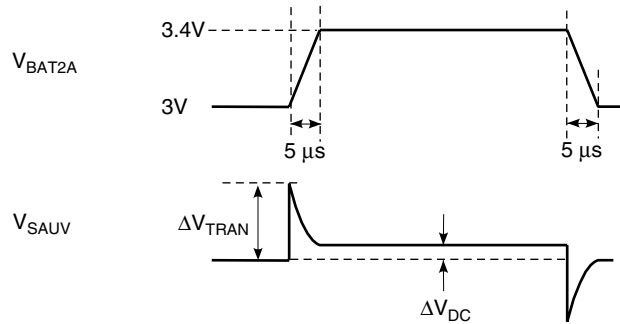


Terminology

Line Regulation

Measures the maximum transient and DC variations of the output voltage of the LDO when the supply changes between two specified values with fixed load current; minimum rise time and fall time is 5 μ s.

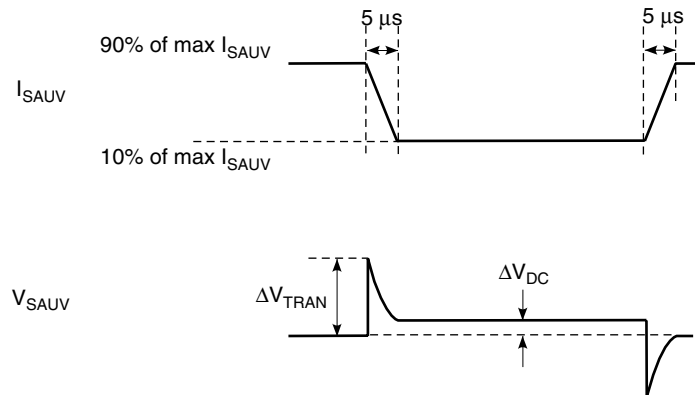
Figure 4. Line Regulation



Load Regulation

Measures the maximum transient and DC variations of the output voltage of the LDO when the load current changes between two specified values with fixed power supply; minimum rise time and fall time is 5 μ s.

Figure 5. Load Regulation



Document Details

Title RE031 Fixed 2.5V 5 mA Low-noise LDO Voltage Regulator

Literature Number 2707

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