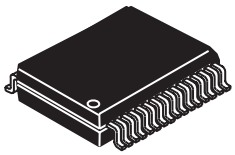
1.5 A Switch-Mode Power Supply with Linear Regulator

34701

POWER SUPPLY INTEGRATED CIRCUIT



EK (Pb-FREE) SUFFIX
98AARH99137A
32-TERMINAL SOICW

The 34701 provides the means to efficiently supply the Freescale Power QUICC™ I, II, and other families of Freescale microprocessors and DSPs. The 34701 incorporates a high-performance switching regulator, providing the direct supply for the microprocessor's core, and a low dropout (LDO) linear regulator control circuit providing the microprocessor I/O and bus voltage.

The switching regulator is a high-efficiency synchronous buck regulator with integrated N-channel power MOSFETs to provide protection features and to allow space-efficient, compact design.

The 34701 incorporates many advanced features; e.g., precisely maintained up/down power sequencing, ensuring the proper operation and protection of the CPU and power system.

Features

- Operating Voltage from 2.8 V to 6.0 V
- High-Accuracy Output Voltages
- Fast Transient Response
- Switcher Output Current Up to 1.5 A
- Undervoltage Lockout and Overcurrent Protection
- Enable Inputs and Programmable Watchdog Timer
- Voltage Margining via I²C™ Bus
- Reset with Programmable Power-ON Delay
- Pb-Free Packaging Designated by Suffix Code EK

I²C is a trademark of Philips Corporation.

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC34701EK/R2	-40 to 85°C	32 SOICW

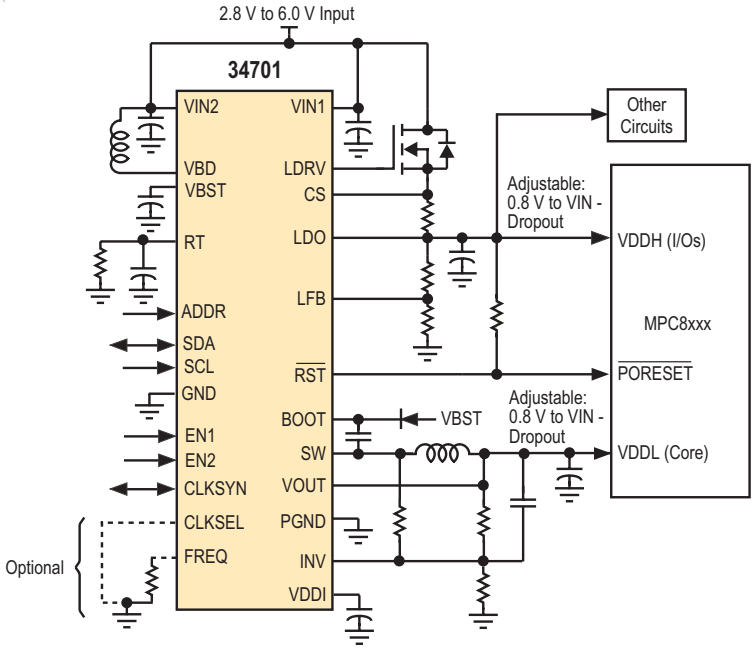


Figure 1. 34701 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

INTERNAL BLOCK DIAGRAM

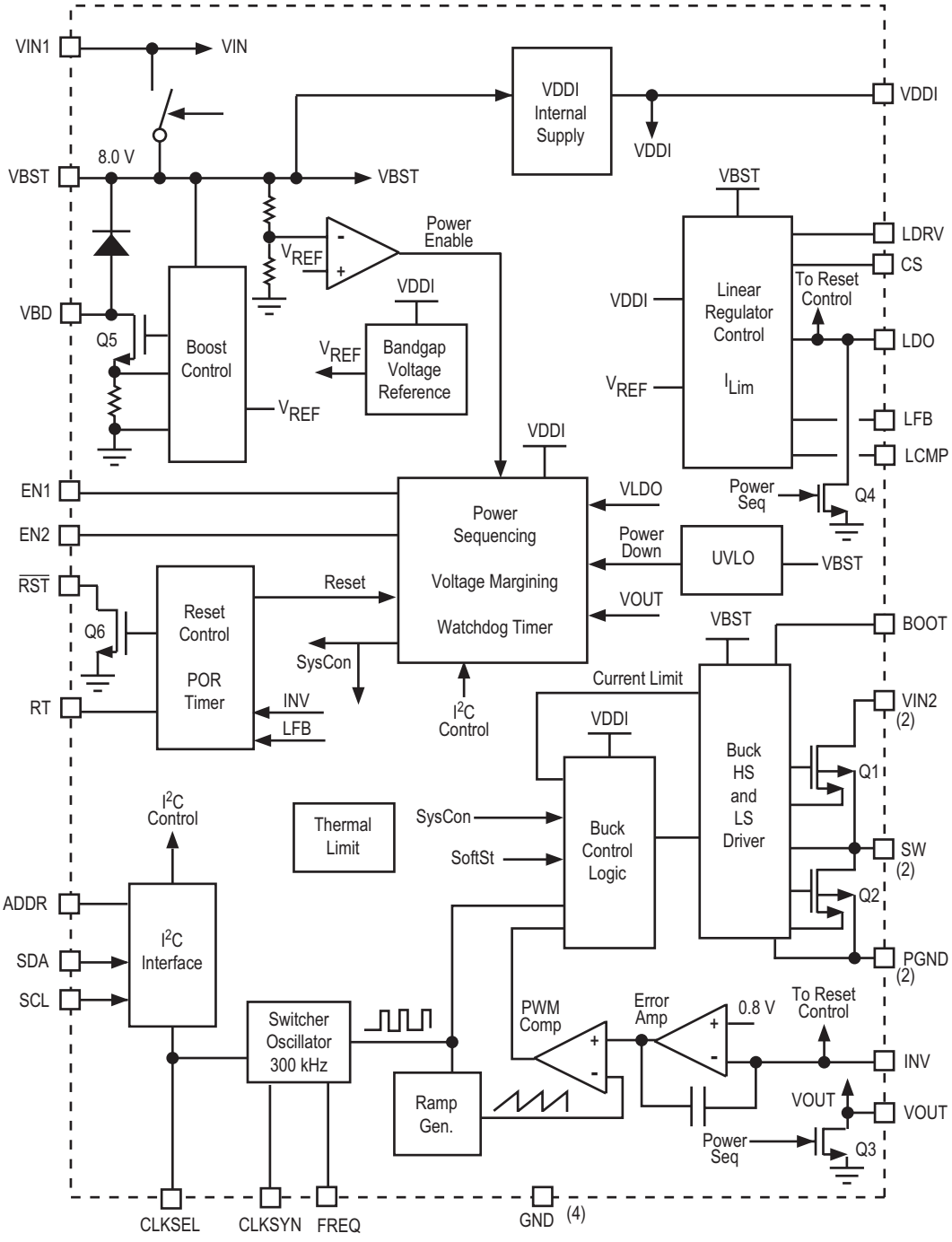


Figure 2. 34701 Simplified Internal Block Diagram

TERMINAL CONNECTIONS

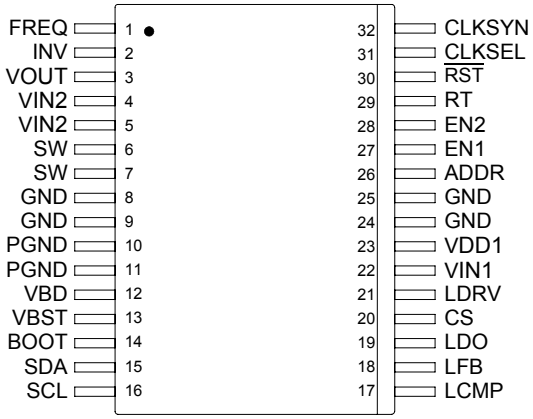


Figure 3. Terminal Connections

Table 1. Terminal Function Description

A functional description of each terminal can be found in the FUNCTIONAL TERMINAL DESCRIPTION section beginning on page 15.

Terminal	Terminal Name	Formal Name	Definition
1	FREQ	Oscillator Frequency	This switcher frequency selection terminal can be adjusted by connecting external resistor RF to the FREQ terminal. The default switching frequency (FREQ terminal left open or tied to VDDI) is set to 300 kHz.
2	INV	Inverting Input	Buck Controller Error Amplifier inverting input.
3	VOUT	Output Voltage	Output voltage of the buck converter. Input terminal of the switching regulator power sequence control circuit.
4, 5	VIN2	Input Voltage 2	Buck regulator power input. Drain of the high-side power MOSFET.
6, 7	SW	Switch	Buck regulator switching node. This terminal is connected to the inductor.
8, 9 24, 25	GND	Ground	Analog ground of the IC, thermal heatsinking.
10, 11	PGND	Power Ground	Buck regulator power ground.
12	VBD	Boost Drain	Drain of the internal boost regulator power MOSFET.
13	VBST	Boost Voltage	Internal boost regulator output voltage. The internal boost regulator provides a 20 mA output current to supply the drive circuits for the integrated power MOSFETs and the external N-channel power MOSFET of the linear regulator. The voltage at the VBST terminal is 7.75V nominal.
14	BOOT	Bootstrap	Bootstrap capacitor input.
15	SDA	Serial Data	I^2C bus terminal. Serial data.
16	SCL	Serial Clock	I^2C bus terminal. Serial clock.
17	LCMP	Linear Compensation	Linear regulator compensation terminal.
18	LFB	Linear Feedback	Linear regulator feedback terminal.
19	LDO	Linear Regulator	Input terminal of the linear regulator power sequence control circuit.

Table 1. Terminal Function Description (continued)

A functional description of each terminal can be found in the FUNCTIONAL TERMINAL DESCRIPTION section beginning on page 15.

Terminal	Terminal Name	Formal Name	Definition
20	CS	Current Sense	Current sense terminal of the LDO. Overcurrent protection of the linear regulator external power MOSFET. The voltage drop over the LDO current sense resistor RS is sensed between the CS and LDO terminals. The LDO current limit can be adjusted by selecting the proper value of the current sensing resistor RS.
21	LDRV	Linear Drive	LDO gate drive of the external pass N-channel MOSFET.
22	VIN1	Input Voltage 1	The input supply terminal for the integrated circuit. The internal circuits of the IC are supplied through this terminal.
23	VDDI	Power Supply	Internal supply voltage. A ceramic low ESR 1uF 6V X5R or X7R capacitor is recommended.
26	ADDR	Address	I^2C address selection. This terminal can either be left open, tied to VDDI, or grounded through a 10 kΩ resistor.
27	EN1	Enable 1	Enable 1 Input. The combination of the logic state of the Enable 1 and Enable 2 inputs determines operation mode and type of power sequencing of the IC.
28	EN2	Enable 2	Enable 2 Input. The combination of the logic state of the Enable 1 and Enable 2 inputs determines operation mode and type of power sequencing of the IC.
29	RT	Reset Timer	This terminal allows programming of the Power-ON Reset delay by means of an external RC network.
30	$\overline{RST}$	Reset Output (Active LOW)	The Reset Control circuit monitors both the switching regulator and the LDO feedback voltages. It is an open drain output and has to be pulled up to some supply voltage (e.g., the output of the LDO) by an external resistor.
31	CLKSEL	Clock Selection	This terminal sets the CLKSYN terminal as either an oscillator output or a synchronization input terminal. The CLKSEL terminal is also used for the I^2C address selection.
32	CLKSYN	Clock Synchronization	Oscillator output/synchronization input terminal.

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
Electrical Ratings			
Supply Voltage	V_{IN1}, V_{IN2}	-0.3 to 7.0	V
Switching Node Voltage	V_{SW}	-1.0 to 7.0	V
Buck Regulator Bootstrap Input Voltage (BOOT - SW)	$V_{IN(BOOT)}$	-0.3 to 8.5	V
Boost Regulator Output Voltage	V_{BST}	-0.3 to 8.5	V
Boost Regulator Drain Voltage	V_{BD}	-0.3 to 9.5	V
$\overline{RST}$ Drain Voltage	$V_{\overline{RST}}$	-0.3 to 7.0	V
Enable Terminal Voltage at EN1, EN2	V_{EN}	-0.3 to 7.0	V
Logic Terminal Voltage at SDA, SCL	V_{LOG}	-0.3 to 7.0	V
Analog Terminal Voltage LDO, VOUT, $\overline{RST}$ LDRV, LCMP, CS	 V_{OUT} V_{LIN}	 -0.3 to 7.0 -0.3 to 8.5	V
Terminal Voltage at CLKSEL, ADDR, RT, FREQ, VDDI, CLKSYN, INV, LFB	V_{LOGIC}	-0.3 to 3.6	V
ESD Voltage [1] Human Body Model Machine Model	 V_{ESD}	 ±2000 ±200	V
Thermal Ratings			
Storage Temperature	T_{STG}	-65 to 150	°C
Lead Soldering Temperature [2]	T_{SOLDER}	260	°C
Maximum Junction Temperature	T_{JMAX}	125	°C
Thermal Resistance Junction to Ambient (Single Layer) [3], [4] Junction to Ambient (Four Layers) [3], [4]	$R_{\theta JA}$	 70 55	°C/W
Thermal Resistance, Junction to Base [5]	$R_{\theta JB}$	18	°C/W
Operational Package Temperature (Ambient Temperature)	T_A	-40 to 85	°C

Notes

1. ESD1 testing is performed in accordance with the Human Body Model (CZAP=100 pF, RZAP=1500 Ω), ESD2 testing is performed in accordance with the Machine Model (CZAP=200 pF, RZAP=0 Ω), and the Charge Device Model.
2. Lead soldering temperature limit is for 10 seconds maximum duration.
3. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board and board thermal resistance.
4. Per JEDEC JESD51-6 with the board horizontal
5. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions -40°C ≤ T_A ≤ 85°C unless otherwise noted. Input voltages VIN1 = VIN2 = 3.3 V using the typical application circuit (see Figure 33) unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
General					
Operating Voltage Range (VIN1, VIN2)	V_{IN}	2.8	–	6.0	V
Start-Up Voltage Threshold (Boost Switching)	V_{ST}	–	1.6	1.8	V
VBST Undervoltage Lockout (VBST rising)	V_{BST_UVLO}	5.5	–	6.5	V
VBST Undervoltage Lockout Hysteresis	$V_{BST\_UVLO\_HYS}$	0.5	–	1.5	V
Input DC Supply Current (Normal Operation Mode, Enabled), Unloaded Outputs	I_{IN}	–	60	–	mA
VIN1 Terminal Input Supply Current (EN1 = EN2 = 0)	I_{IN1}	–	10	–	mA
VIN2 Terminal Input Leakage Current (EN1 = EN2 = 0)	I_{IN2}	–	100	–	µA
VDDI Internal Supply Voltage	V_{DDI}	2.9	–	3.3	V
VDDI Maximum Output Current (Externally Loaded)	I_{DDI}	–	–	-10	mA
Buck Converter					
Buck Converter Feedback Voltage (6), (7) IVOUT = 15 mA to 1.5 A. Includes Load Regulation Error	V_{INV}	0.784	0.800	0.816	V
Buck Converter Voltage Margining Step Size	V_{MVO}	–	1.0	–	%
Buck Converter Voltage Margining Highest Positive Value	V_{MP}	5.9	–	7.9	%
Buck Converter Voltage Margining Lowest Negative Value	V_{MN}	-7.9	–	-5.9	%
Buck Converter Line Regulation (6), (7) VIN1 = VIN2 = 2.8 V to 6.0 V, IVOUT = 15 mA to 1.5 A	REG_{LNVO}	-1.0	–	1.0	%
Buck Converter Load Regulation (6), (7) VIN1 = VIN2 = 2.8 V to 6.0 V, IVOUT = 15 mA to 1.5 A	REG_{LDVO}	-1.0	–	1.0	%
VOUT Input Leakage Current VOUT = 5.25 V	I_{INVOUT}	–	3.5	–	mA
INV Input Leakage Current INV = 0.8 V	I_{ININV}	-1.0	–	1.0	µA

Notes
6. Design information only. This parameter is not production tested.
7. IVOUT refers to load current on output switcher.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions -40°C ≤ T_A ≤ 85°C unless otherwise noted. Input voltages VIN1 = VIN2 = 3.3 V using the typical application circuit (see Figure 33) unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Buck Converter (continued)					
High-Side Power MOSFET Q1 RDS(ON) [8], [9] ID = 500 mA, T_A = 25°C, VBST = 8.0 V	$R_{DS(ON)Q1}$	–	60	–	mΩ
Low-Side Power MOSFET Q2 RDS(ON) [8], [9] ID = 500 mA, T_A = 25°C, VBST = 8.0 V	$R_{DS(ON)Q2}$	–	65	–	mΩ
Buck Converter Peak Current Limit (High Level)	I_{LIMH}	-4.0	-2.7	-1.5	A
VOUT Pulldown MOSFET Q3 Current Limit T_A = 25°C, VBST = 8.0 V	I_{LIMPQ3}	0.75	–	2.0	A
VOUT Pulldown MOSFET Q3 $R_{DS(ON)}$ [9] ID = 1.0 A, VBST = 8.0 V	$R_{DS(ON)PQ3}$	–	–	1.9	Ω
Thermal Shutdown (VOUT Pulldown MOSFET Q3) [8]	T_{SD}	150	170	190	°C
Thermal Shutdown Hysteresis [8]	T_{HYS}	–	10	–	°C

Notes

8. Design information only. This parameter is not production tested.
9. ID is the MOSFET drain current.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions -40°C ≤ T_A ≤ 85°C unless otherwise noted. Input voltages VIN1 = VIN2 = 3.3 V using the typical application circuit (see Figure 33) unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Error Amplifier (Buck Converter)					
Input Impedance (10)	R_{IN}	–	500	–	kΩ
Output Impedance (10)	R_{OUT}	–	150	–	Ω
DC Open Loop Gain (10)	A_{VOL}	–	80	–	dB
Gain Bandwidth Product (10)	G_{BW}	–	35	–	MHz
Slew Rate (10)	v_{SR}	–	200	–	V/μs
Output Voltage – High Level VIN1 > 3.3 V, IOEA = -1.0 mA (10), (11)	V_{EA_OH}	–	2.0	–	V
Output Voltage – Low Level IOEA = -1.0 mA (10), (11)	V_{EA_OL}	–	0.4	–	V
Oscillator Ramp (10)	V_{SCRamp}	–	0.5	–	V
Oscillator					
CLKSYN Terminal (open) Low Level Output Voltage IOL = +1.0 mA (12)	V_{OSC_OL}	–	–	0.4	V
CLKSYN Terminal (open) High Level Output Voltage IOH = -1.0 mA (13)	V_{OSC_OH}	V_{DDI} - 0.4 V	–	–	V
CLKSYN Terminal (grounded) Input Voltage Threshold	V_{OSC_IH}	1.2	–	2.0	V
CLKSYN Terminal Pullup Resistance	R_{PU}	60	–	240	kΩ
Frequency Adjusting Reference Voltage	V_{FREQ}	–	1.26	–	V
Boost Regulator					
Regulator Output Voltage IBST = 20 mA, VIN1 = VIN2 = 2.8 V to 6.0 V	V_{BST}	7.3	7.7	8.3	V
Power MOSFET Q5 RDS(ON)(10) IBD = 500 mA, T_A = 25°C	$R_{DS(ON)Q5}$	–	650	1000	mΩ
Regulator Recommended Output Capacitor	C_{BST}	–	10	–	μF
Regulator Recommended Output Capacitor Maximum ESR	$ESRC_{BST}$	–	100	–	mΩ

Notes
10. Design information only. This parameter is not production tested.
11. IOEA Refers to Error Amplifier Output Current.
12. IOL Refers to I/O Low Level
13. IOH Refers to I/O High Level

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions -40°C ≤ T_A ≤ 85°C unless otherwise noted. Input voltages VIN1 = VIN2 = 3.3 V using the typical application circuit (see Figure 33) unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Linear Regulator (LDO)					
LDO Feedback Voltage (15) VIN1 = VIN2 = 2.8 V to 6.0 V, ILDO = 10 mA to 1000 mA. Includes Load Regulation Error	V_{LFB}	0.784	0.800	0.816	V
LDO Voltage Margining Step Size	V_{MLDO}	–	1.0	–	%
LDO Voltage Margining Highest Positive Value	V_{MP}	5.9	–	7.9	%
LDO Voltage Margining Lowest Negative Value	V_{MN}	-7.9	–	-5.9	%
LDO Line Regulation (15) VIN1 = VIN2 = 2.8 V to 6.0 V, ILDO = 1000 mA	REG_{LNVLDO}	-1.0	–	1.0	%
LDO Load Regulation (15) ILDO = 10 mA to 1000 mA	REG_{LDVLDO}	-1.0	–	1.0	%
LDO Ripple Rejection, Dropout Voltage (15) VDO = 1.0 V, VRIPPLE = +1.0 V p-p Sinusoidal, f = 300 kHz, ILDO = 500 mA (14)	V_{LDO_RR}	–	40	–	**dB**
LDO Maximum Dropout Voltage (VIN - VLDO), using IRL2703 (15) VLDO = 2.5 V, ILDO = 1000 mA	V_{DO}	–	50	75	mV
LDO Current Sense Comparator Threshold Voltage (VCS - VLDO)	V_{CSTH}	35	50	65	mV
LDO Terminal Input Current, VLDO = 5.25 V	I_{LDO}	1.0	1.9	4.0	mA
LDO Feedback Input Current (LFB Terminal), VLFB = 0.8 V	I_{LFB}	-1.0	–	1.0	µA
LDO Drive Output Current (LDRV Terminal), VLDRV = 0 V	I_{LDRV}	-5.0	-3.3	-2.0	mA
CS Terminal Input Leakage Current VCS = 5.25 V	I_{CSLK}	50	–	200	µA
LDO Pulldown MOSFET Q4 Current Limit T_A = 25°C, VBST = 8.0 V (LDO Terminal)	I_{LIMQ4}	0.75	–	2.0	A
LDO Pulldown MOSFET Q4 RDS(ON) ID = 1.0 A, VBST = 8.0 V	$R_{DS(ON)Q4}$	–	–	1.9	Ω
LDO Recommended Output Capacitance	C_{LDO}	–	10	–	µF
LDO Recommended Output Capacitor ESR	R_{LDO}	–	5.0	–	mΩ
Thermal Shutdown (LDO Pulldown MOSFET Q4) (14)	T_{SD}	150	170	190	°C
Thermal Shutdown Hysteresis (14)	T_{SDHYS}	–	10	–	°C

Notes
14. Design information only. This parameter is not production tested.
15. IDO refers to Load Current on External LDOFET - IRL2703 is the Intersil MOSFET.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions -40°C ≤ T_A ≤ 85°C unless otherwise noted. Input voltages VIN1 = VIN2 = 3.3 V using the typical application circuit (see Figure 33) unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Control and Supervisory Circuits					
Enable (EN1, EN2) Input Voltage Threshold	V_{EN-TH}	1.0	1.5	2.0	V
Enable (EN1, EN2) Pulldown Resistance	R_{EN-PD}	30	55	90	kΩ
$\overline{RST}$ Low-Level Output Voltage, IOL = 5.0 mA	V_{OL}	–	–	0.4	V
$\overline{RST}$ Leakage Current, OFF State, Pulled Up to 5.25 V	$I_{LKG-\overline{RST}}$	–	–	10	µA
$\overline{RST}$ Undervoltage Threshold on VOUT (ΔVOUT/VOUT) (16)	V_{OUTITh}	-14	–	-0.5	%
$\overline{RST}$ Overvoltage Threshold on VOUT (ΔVOUT/VOUT) (16)	V_{OUTITh}	0.5	–	14	%
$\overline{RST}$ Undervoltage Threshold on VLDO (ΔVLDO/VLDO) (16)	V_{LDOITh}	-12	–	-4.0	%
$\overline{RST}$ Overvoltage Threshold on VLDO (ΔVLDO/VLDO) (16)	V_{LDOITh}	4.0	–	12	%
$\overline{RST}$ Timer Voltage Threshold	V_{TH-RT}	1.0	1.2	1.5	V
$\overline{RST}$ Timer Source Current (RT terminal at 0 V)	I_{S-RT}	-17	–	-34	mA
$\overline{RST}$ Timer Leakage Current	I_{LKG-RT}	-1.0	–	1.0	µA
$\overline{RST}$ Timer Saturation Voltage, Reset Timer Current = 300 µA	V_{SAT-RT}	–	35	100	mV
Maximum Recommended Value of the Reset Timer Capacitor	C_t	–	–	47	µF
CLKSEL Threshold Voltage	V_{THCLKS}	1.2	1.6	2.0	V
CLKSEL Pullup Resistance	$R_{PU-CLK}S$	60	120	240	kΩ
ADDR Threshold Voltage (16)	V_{THADDR}	1.2	1.6	2.0	V
ADDR Pullup Resistance	$R_{PU-ADDR}$	60	120	240	kΩ
Thermal Shutdown (IC sensor) (16)	T_{LIM}	150	170	190	°C
Thermal Shutdown Hysteresis (16)	T_{LIMHYS}	–	10	–	°C
SDA, SCL Terminals I^2C Bus (Standard)					
Input Threshold Voltage (Terminal SCL), Rising Edge (16)	V_{LTH}	1.3	–	1.7	V
Input Threshold Voltage (Terminal SDA)	V_{LTH}	1.3	–	1.7	V
SDA, SCL Input Current, Input Voltage = 5.25 V (VIN1)	I_{IN}	–	1.0	10	µA
SDA Low-Level Output Voltage, 3.0 mA Sink Current	V_{OL}	–	–	0.4	V
SDA, SCL Capacitance (16)	C_{Input}	–	7.0	10	pF

Notes

16. Design information only. This parameter is not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions -40°C ≤ T_A ≤ 85°C unless otherwise noted. Input voltages VIN1 = VIN2 = 3.3 V using the typical application circuit (see Figures 33) unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Buck Converter					
Duty Cycle Range (Normal Operation) (17)	t_D	0	–	95	%
Switching Node SW Rise Time (17) VIN = 5.0 V, ILOAD = 1.0 A	t_{RISE}	–	7.0	–	ns
Switching Node SW Fall Time (17) VIN = 5.0 V, ILOAD = 1.0 A	t_{FALL}	–	17	–	ns
Maximum Deadtime (17)	t_D	–	35	–	ns
Buck Control Loop Propagation Delay (17) VINV < 0.8 V to VSW > 90% of High Level or VINV > 0.8 V to VSW < 10% of Low Level	t_{PD}	–	50	–	ns
Soft Start Duration (Power Sequencing Disabled, EN1 = 1, EN2 = 1) (17)	t_{SS}	200	350	800	µs
Fault Condition Time-Out (17)	t_{FAULT}	7.0	10	15	ms
Retry Timer Cycle (17)	t_{RET}	70	100	150	ms
Oscillator					
Oscillator Center Frequency(19) RF = 11.3 kΩ	f_{OSC}	270	300	330	kHz
Oscillator Frequency Range	f_{OSC}	200	–	400	kHz
Oscillator Frequency Adjusting Resistor Range	R_{FREQ}	7.0	–	22	kΩ
Oscillator Frequency Adjustment (18), (19) RF = 7.0 kΩ	f_{OSC}	400	–	–	kHz
Oscillator Frequency Adjustment (18), (19) RF = 22 kΩ	f_{OSC}	–	–	200	kHz
Oscillator Default Frequency (Switching Frequency), FREQ Terminal Open	f_{OSC}	–	300	–	kHz
Oscillator Output Signal Duty Cycle (Square Wave, 180° Out-of-Phase with the Internal Suitable Oscillator)	D_{OSC}	40	50	60	%
Synchronization Pulse Minimum Duration (17)	t_{SYNC}	1.0	–	–	µs

Notes
17. Design information only. This parameter is not production tested.
18. see Figure 4 for more details
19. RF is RFREQ

Table 4. DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions -40°C ≤ T_A ≤ 85°C unless otherwise noted. Input voltages VIN1 = VIN2 = 3.3 V using the typical application circuit (see Figures 33) unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Boost Regulator					
Boost Regulator MOSFET Maximum ON Time (20)	t_{ON}	–	24	–	µs
Boost Regulator Control Loop Propagation Delay (20)	t_{BST_PD}	–	50	–	ns
Boost Switching Node VBD Rise Time (20) IBST = 20 mA	t_{B_RISE}	–	5.0		ns
Boost Switching Node VBD Fall Time (20) IBST = 20 mA	t_{B_FALL}	–	3.0	–	ns
Linear Regulator (LDO)					
Fault Condition Time-Out	t_{FAULT}	7.0	10	15	ms
Retry Timer Cycle	t_{Ret}	70	100	150	ms
Reset Monitor ($\overline{RST}$)					
Monitoring LFB Terminal Delay	$t_{D\_RST\_LFB}$	12	–	28	µs
Monitoring INV Terminal Delay	$t_{D\_RST\_INV}$	12	–	28	µs
SCA, SCL Terminal, I²C Bus (Standard)					
SCL Clock Frequency (20)	f_{SCL}	–	–	100	kHz
Bus Free Time Between a STOP and a START Condition (20)	t_{BUF}	4.7	–	–	µs
Hold Time (Repeated) START Condition (After this period, the first clock pulse is generated.) (20)	$t_{HD\text{-}STA}$	4.0	–	–	µs
Low Period of the SCL Clock (20)	t_{LOW}	4.7	–	–	µs
High Period of the SCL Clock (20)	t_{HIGH}	4.0	–	–	µs
SDA Fall Time from VIH_MAX to VIL_MIN, Bus Capacitance 10 pF to 400 pF, 3.0 mA Sink Current (20), (22)	t_F	–	–	250	ns
Setup Time for a Repeated START Condition (20)	$t_{SU\text{-}STA}$	4.7	–	–	µs
Data Hold Time for I²C Bus Devices (20), (21)	$t_{HD\text{-}DAT}$	0.0	–	–	µs
Data Setup Time (20)	$t_{SU\text{-}DAT}$	250	–	–	ns
Setup Time for STOP Condition (20)	$t_{SU\text{-}STO}$	4.0	–	–	µs
Capacitive Load for Each Bus Line (20)	C_B	–	–	400	pF

Notes

20. Design information only. This parameter is not production tested.
21. The device provides an internal hold time of at least 300 ns for the SDA signal (refer to the VIH_MIN of the SCL signal) to bridge the undefined region of the falling edge of SCL.
22. VIH is High Level Voltage on I²C bus lines and VIL is Low Level Voltage on I²C bus lines

TIMING DIAGRAM

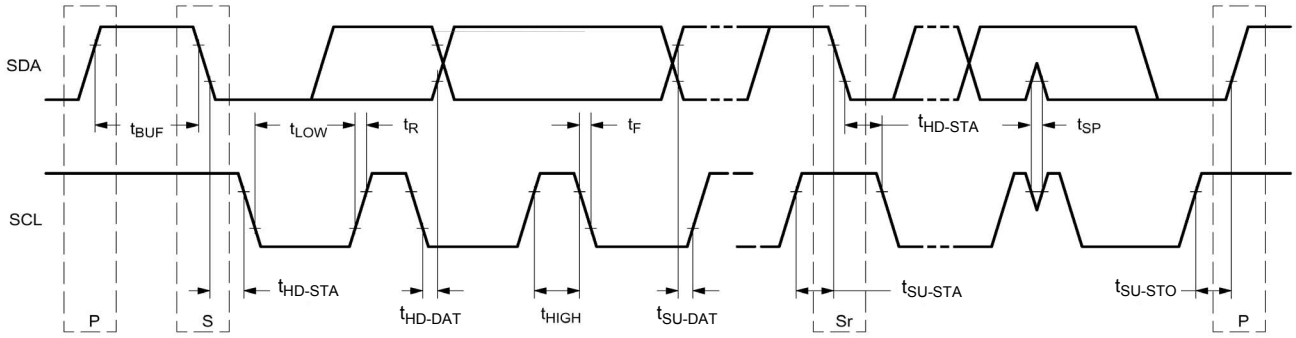


Figure 4. Definition of Time on the I^2C Bus

ELECTRICAL PERFORMANCE CURVES

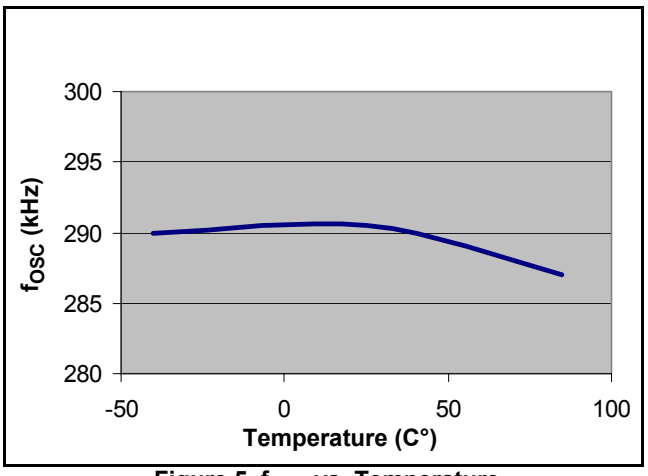


Figure 5. f_{OSC} vs. Temperature

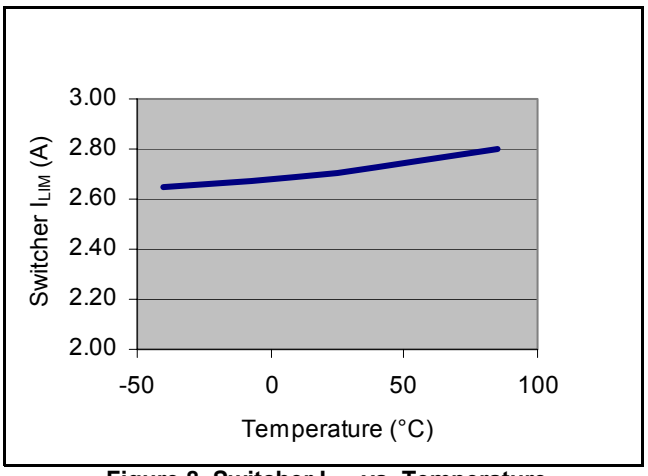


Figure 8. Switcher I_{Lim} vs. Temperature

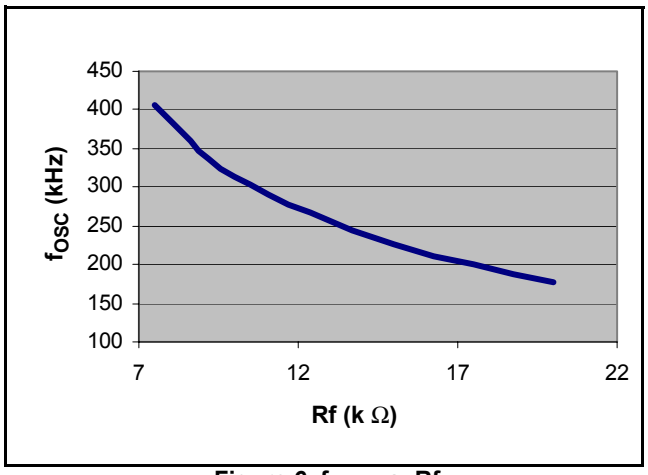


Figure 6. f_{OSC} vs. Rf

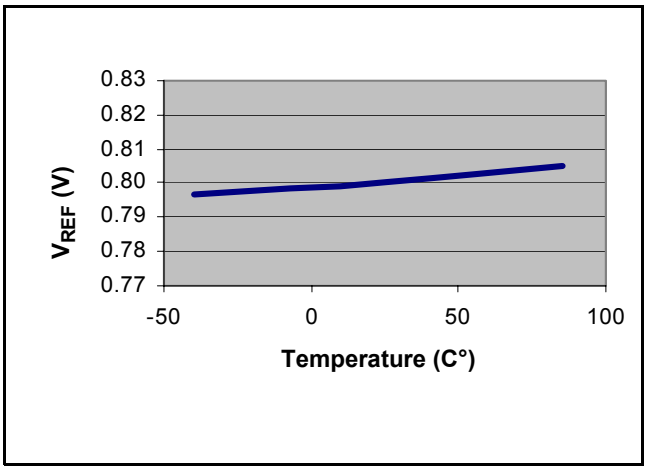


Figure 9. V_{REF} vs. Temperature

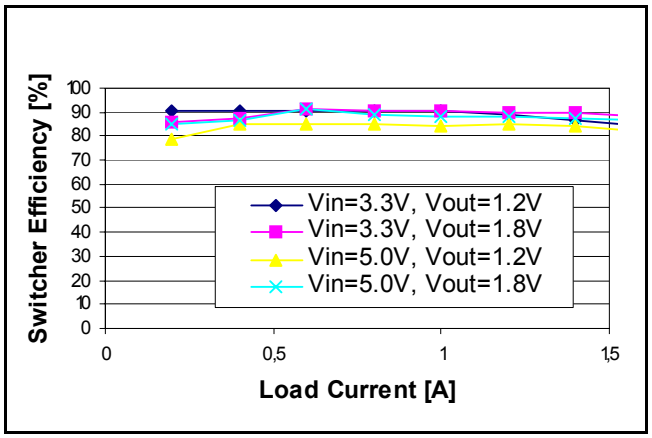


Figure 7. Switcher Efficiency vs. Load Current

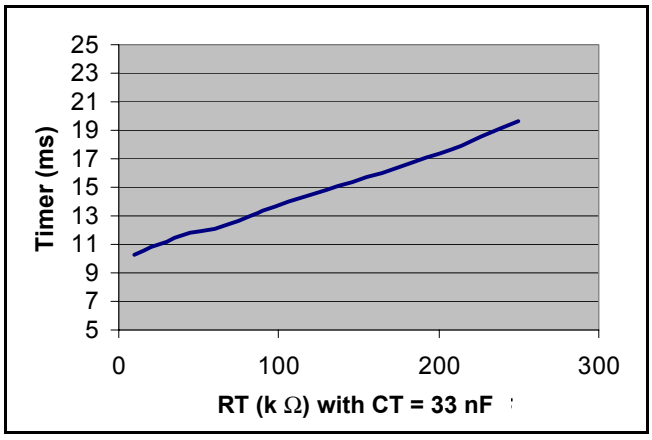


Figure 10. Timer (ms) vs. RT

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 34701 power supply integrated circuit provides the means to efficiently supply the Freescale Power QUICC and other families of Freescale microprocessors. It incorporates a high-performance synchronous buck regulator, supplying the microprocessor's core, and a low dropout (LDO) linear regulator providing the microprocessor I/O and bus voltages.

This device incorporates many advanced features; e.g., precisely maintained up/down power sequencing, ensuring the proper operation and protection of the CPU and power system. At the same time, it provides high flexibility of configuration, allowing the maximum optimization of the power supply system.

FUNCTIONAL TERMINAL DESCRIPTION

OSCILLATOR FREQUENCY TERMINAL (FREQ)

This switcher frequency selection terminal can be adjusted by connecting external resistor RF to the FREQ terminal. The default switching frequency (FREQ terminal left open or tied to VDDI) is set to 300 kHz.

INVERTING INPUT TERMINAL (INV)

Buck Controller Error Amplifier inverting input.

OUTPUT VOLTAGE TERMINAL (VOUT)

Output voltage of the buck converter. Input terminal of the switching regulator power sequence control circuit.

INPUT VOLTAGE 2 TERMINALS (VIN2)

Buck regulator power input. Drain of the high-side power MOSFET.

SWITCH TERMINALS (SW)

Buck regulator switching node. This terminal is connected to the inductor.

GROUND TERMINALS (GND)

Analog ground of the IC, thermal heatsinking.

POWER GROUND TERMINALS (PGND)

Buck regulator power ground.

BOOST DRAIN TERMINAL (VBD)

Drain of the internal boost regulator power MOSFET.

BOOST VOLTAGE TERMINAL (VBST)

Internal boost regulator output voltage. The internal boost regulator provides a 20 mA output current to supply the drive circuits for the integrated power MOSFETs and the external N-channel power MOSFET of the linear regulator. The voltage at the VBST terminal is 7.75V nominal.

BOOTSTRAP TERMINAL (BOOT)

Bootstrap capacitor input.

SERIAL DATA TERMINAL (SDA)

I^2C bus terminal. Serial data.

SERIAL CLOCK TERMINAL (SCL)

I^2C bus terminal. Serial clock.

LINEAR COMPENSATION TERMINAL (LCMP)

Linear regulator compensation terminal.

LINEAR FEEDBACK TERMINAL (LFB)

Linear regulator feedback terminal.

LINEAR REGULATOR TERMINAL (LDO)

Input terminal of the linear regulator power sequence control circuit.

CURRENT SENSE TERMINAL (CS)

Current sense terminal of the LDO. Overcurrent protection of the linear regulator external power MOSFET. The voltage drop over the LDO current sense resistor RS is sensed between the CS and LDO terminals. The LDO current limit can be adjusted by selecting the proper value of the current sensing resistor RS.

LINEAR DRIVE TERMINAL (LDRV)

LDO gate drive of the external pass N-channel MOSFET.

INPUT VOLTAGE 1 TERMINAL (VIN1)

The input supply terminal for the integrated circuit. The internal circuits of the IC are supplied through this terminal.

POWER SUPPLY TERMINAL (VDDI)

Internal supply voltage. A ceramic low ESR 1uF 6V X5R or X7R capacitor is recommended.

ADDRESS TERMINAL (ADDR)

The ADDR terminal is used to set the address of the device when used in an I^2C communication. This terminal can either be tied to VDDI or grounded through a 10 kΩ resistor. Refer to I^2C Bus Operation on page 26 for more information on this terminal.

ENABLE 1 AND 2 TERMINALS (EN1 AND EN2)

These two terminals permit positive logic control of the Enable function and selection of the Power Sequencing mode concurrently. Table 5 depicts the EN1 and EN2 function and Power Sequencing mode selection.

Both EN1 and EN2 terminals have internal pulldown resistors and both can withstand a short circuit to the supply voltage, 6.0 V.

Table 5. Operating Mode Selection

EN1	EN2	Operating Mode
0	0	Regulators Disabled
0	1	Standard Power Sequencing
1	0	Inverted Power Sequencing
1	1	No Power Sequencing, Regulators Enabled

RESET TIMER TERMINAL (RT)

The Reset Timer power-up delay (RT) terminal is used to set the delay between the time when the LDO and switcher outputs are active and stable and the $\overline{RST}$ output is released. An external resistor and capacitor are used to program the timer. The power-up delay can be obtained by using the following formula:

$$t_D = 10\ ms + R_tC_t$$

Where R_t is the Reset Timer programming resistor and C_t is the Reset Timer programming capacitor, both connected in parallel from RT to ground.

Note Observe the maximum C_t value and expect reduced accuracy if R_t is less than 10 kΩ.

RESET OUTPUT TERMINAL ($\overline{RST}$)

The Reset Control circuit monitors both the switching regulator and the LDO feedback voltages. It is an open drain output and has to be pulled up to some supply voltage (e.g., the output of the LDO) by an external resistor.

The Reset Control circuit supervises both output voltages—the linear regulator output VLDO and the switching regulator output VOUT. When either of these two regulators is out of regulation (high or low), the $\overline{RST}$ terminal is pulled low. There is a 20 μs delay filter preventing erroneous resets. During power-up sequencing, $\overline{RST}$ is held low until the Reset Timer times out.

CLOCK SELECTION TERMINAL (CLKSEL)

This terminal sets the CLKSYN terminal as either an oscillator output or a synchronization input terminal. The CLKSEL terminal is also used for the I^2C address selection.

CLOCK SYNCHRONIZATION TERMINAL (CLKSYN)

Oscillator output/synchronization input terminal.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

INTRODUCTION

The 34701 incorporates a high-performance synchronous buck regulator, supplying the microprocessor's core, and a low dropout (LDO) linear regulator providing the microprocessor I/O and bus voltages. This device incorporates many advanced features; e.g., precisely maintained up/down power sequencing, ensuring the proper operation and protection of the CPU and power system.

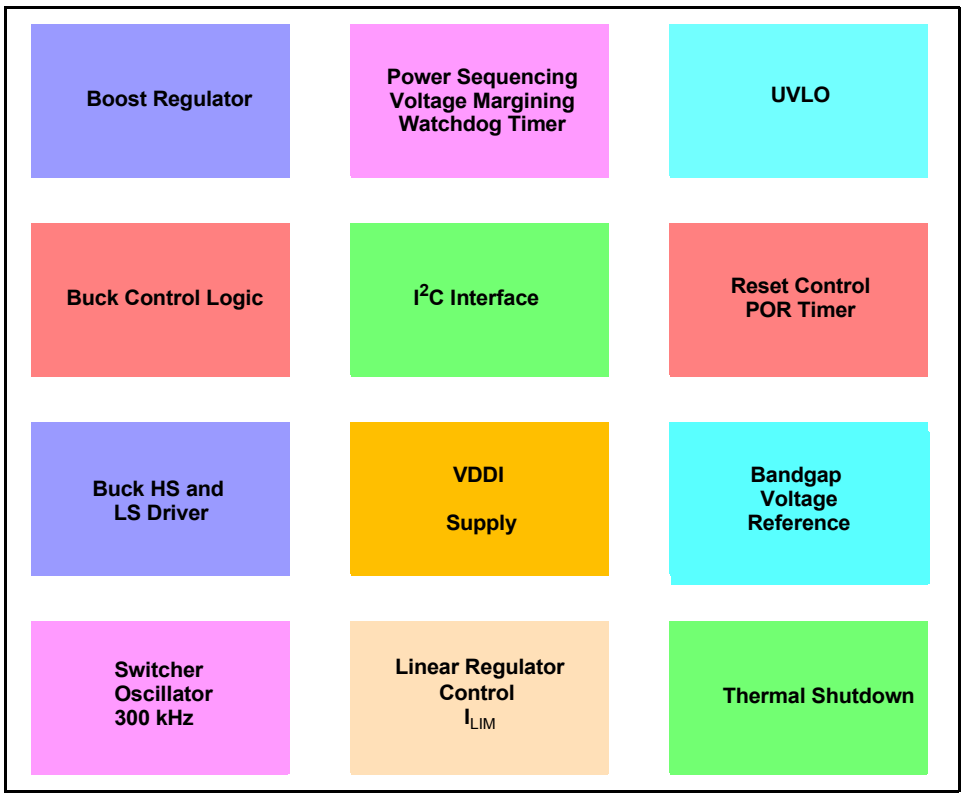


Figure 11. 34701 Functional Internal Block Diagram

BOOST REGULATOR

A boost regulator provides a high voltage necessary to properly drive the buck regulator power MOSFETs, especially during the low input voltage condition. The LDO regulator external N-channel MOSFET gate is also powered from the boost regulator. In order to properly enhance the high-side MOSFETs when only a +3.3 V supply rail powers the integrated circuit, the boost regulator provides an output voltage of 7.75 V nominal value.

The 34701 boost regulator uses a simple hysteretic current control technique, which allows fast power-up and does not require any compensation. When the boost regulator main power switch (low side) is turned on, the current in the inductor starts to ramp up. After the inductor current reaches the upper current limit (nominally set at 1.0 A), the low-side switch is turned off and the current charges the output capacitor through the internal rectifier. When the inductor current falls below the valley current limit value (nominally 600 mA), the low-side switch is turned on again, starting the next switching cycle. After the boost regulator output capacitor reaches approximately 6.0 volts, the peak and valley current limit levels are proportionally scaled down to approximately one fifth of their original values. When the boost regulator reaches its regulation limit (7.75 V typical), the low-side switch is turned off until the output voltage falls below the regulation limit again.

The higher current limit values in the beginning of the boost regulator start-up sequence allow fast power up of the whole IC, while the normal operation with reduced current limit greatly reduces the switching noise and therefore improves the overall EMC performance. See Figure 12 for the boost regulator output voltage and inductor current waveforms (picture not to scale).

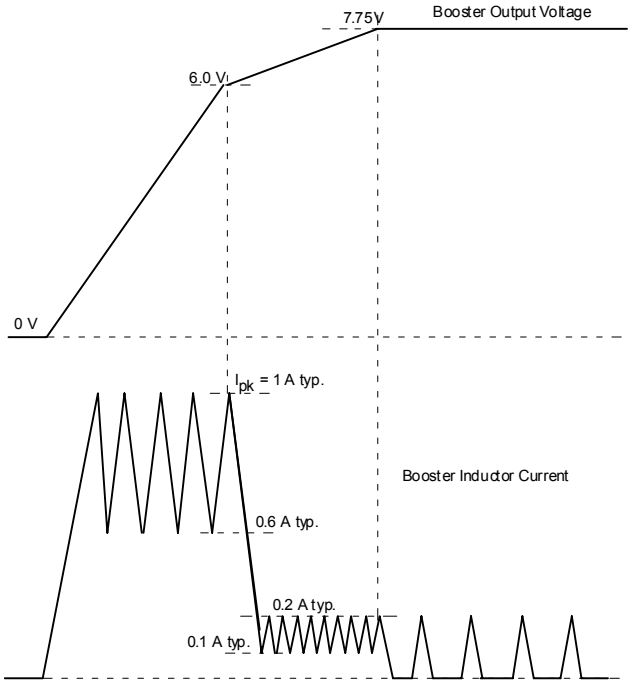


Figure 12. Boost Regulator Startup (Not To Scale)

SWITCHING REGULATOR

The switching regulator is a high-frequency (300 kHz default, adjustable in the range from 200 kHz to 400 kHz), synchronous buck converter driving integrated high-side and low-side N-channel power MOSFETs. The switching regulator output voltage is adjustable by means of an external resistor divider to provide the required output voltage within ±2.0% accuracy, and is intended to directly power the core of the microprocessor. The buck controller uses a PWM Voltage Mode Control topology with Feed-Forward to achieve excellent line and load regulation.

The 34702 integrated boost regulator provides a **7.75** V rail which is used to properly bias the switcher's MOSFET. In addition, the boost structure has a very low start up voltage (Typically 1.6 V), hence ensuring very low input voltage functionality. A typical bootstrap technique is used to provide voltage necessary to properly enhance the high-side MOSFET gate. When the regulator is supplied only from low-input voltage (e.g., single +3.3 V supply rail), the bootstrap capacitor is charged from the internal boost regulator output VBST through an external diode. This arrangement allows the 34701 to operate from very low input voltage and also comply with the power sequencing requirements of the supplied microcontroller.

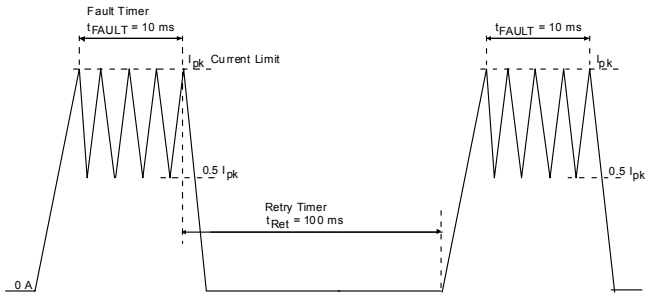


Figure 13. Switching Regulator Current Limit (Not To Scale)

To avoid destruction of the supplied circuits, the switching regulator has a current limit with retry capability. When an overcurrent condition occurs and the switch current reaches the peak current limit value, the main (high-side) switch is turned off until the inductor current decays to the valley value, which is one-half of the peak current limit. If an overcurrent condition exists for 10 ms, the buck regulator control circuit shuts the switcher OFF and the switcher retry timer starts to time out. When the timer expires after 100 ms, the switcher engages the start-up sequence and runs for 10 ms, repeatedly checking for the overcurrent condition. Figure 13 describes the switching regulator overcurrent condition and current limit. During the current limited operation (e.g., in case of short circuit on the switching regulator output), the switching regulator operation is not synchronized to the oscillator frequency. Figure 14 (respectively Figure 15) depicts the current limit with a retry capability feature of the switcher (respectively LDO).

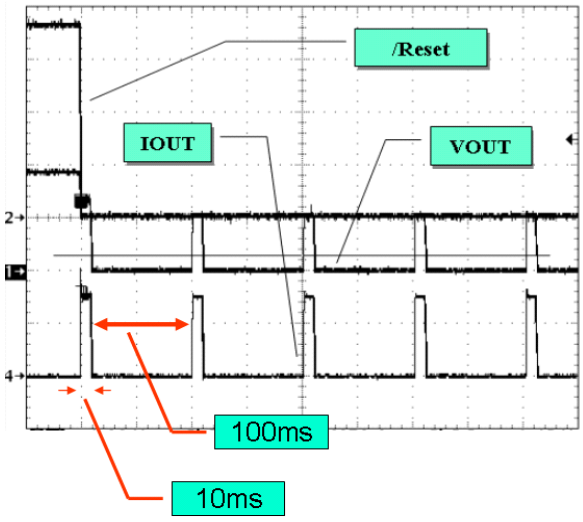


Figure 14. Switching Converter Overcurrent Protection

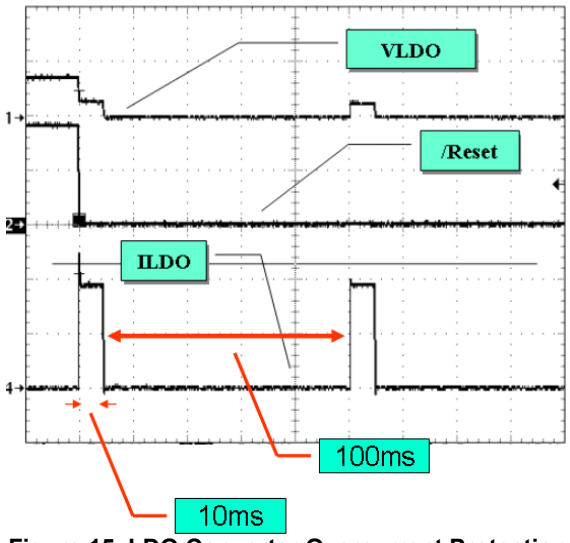


Figure 15. LDO Converter Overcurrent Protection

The output voltage VOUT can be adjusted by means of an external resistor divider connected to the feedback control terminal INV. The switching regulator output voltage can be adjusted in the range of 0.8 V to VIN - buck dropout voltage. Power-up, power-down, and fault management are coordinated with the linear regulator.

SWITCHER OSCILLATOR

A 300 kHz (default) oscillator sets the switching frequency of the buck regulator. The frequency of the oscillator can be adjusted between 200 kHz and 400 kHz by an optional external resistor RF connected from the FREQ terminal of the integrated circuit to ground. See Figure 6 on page 14 for frequency resistor selection.

The CLKSYN terminal can be configured as either an oscillator output when the CLKSEL terminal is left open or as a synchronization input when the CLKSEL terminal is grounded. The oscillator output signal is a square wave logic signal with 50% duty cycle, 180 degrees out-of-phase with the internal clock signal. This allows opposite phase synchronization of two 34702 devices.

When the CLKSYN terminal is used as a synchronization input (CLKSEL terminal grounded), the external resistor RF chosen from the chart in Figure 6 should be used to synchronize the internal slope compensation ramp to the external clock. Operation is only recommended between 200 kHz and 400 kHz. The supplied synchronization signal does not need to be 50% duty cycle. Minimum pulse width is 1.0 µs.

LOW DROPOUT LINEAR REGULATOR (LDO)

The adjustable low dropout linear regulator (LDO) is capable of supplying a 1.0 A output current. It has a current limit with retry capability. When the voltage measured across the current sense resistor reaches the 50 mV threshold, the control circuit limits the current for 10 ms. If the overcurrent condition still exists, the linear regulator is turned off and the retry timer starts to time out. When the timer expires after 100 ms, the LDO tries to power up again for 10 ms, repeatedly checking for the overcurrent condition. The current limit of the LDO can be set by using the following formula:

$$I_{LIM} = 50\ mV/RS$$

Where RS is the LDO current sense resistor, connected between the CS terminal and the LDO terminal output (see Figure 33 on page 32), and 50 mV is the typical value of the LDO current sense comparator threshold voltage.

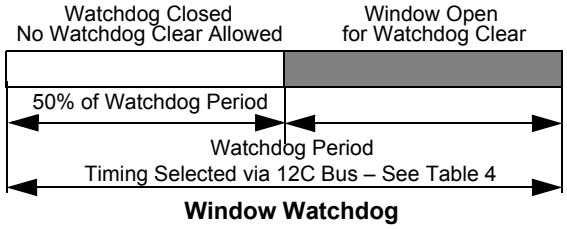
When no current sense resistor is used, it is still possible to detect the overcurrent condition by tying the current sense terminal CS to the VBST voltage. In this case, the overcurrent condition is sensed by saturation of the linear regulator driver buffer.

The output voltage of the LDO can be adjusted by means of an external resistor divider connected to the feedback control terminal LFB. The linear regulator output voltage can be adjusted in the range of 0.8 V to VIN - LDO dropout voltage. Power-up, power-down, and fault management are coordinated with the switching regulator.

POWER SEQUENCING VOLTAGE MARGINING WATCHDOG TIMER

A watchdog function is available via I^2C bus communication. It is possible to select either window watchdog or time-out watchdog operation, as illustrated in Figure 16.

Watchdog time-out starts when the watchdog function is activated via I^2C bus sending a Watchdog Programming command byte, thus determining watchdog operation (window or time-out) and period duration (refer to Table 8, page 27). If the watchdog is cleared by receiving a new Watchdog Programming command through the I^2C bus, the watchdog timer is reset and the new time-out period begins. If the watchdog time expires, the $\overline{RST}$ will become active (LOW) for a time determined by the RC components of the RT timer plus 10 ms. After a watchdog time-out, the function is no longer active.



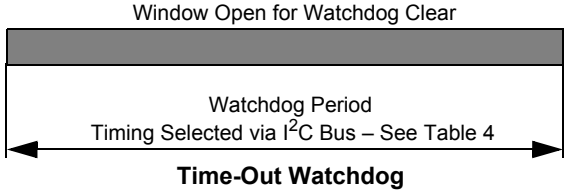


Figure 16. Watchdog Operation

When the Window Watchdog function is selected, the timer cannot be cleared during the Closed Window time, which is 50% of the total watchdog period. When the watchdog is cleared, the timer is reset and starts a new time-out period. If the watchdog is not cleared during the Open Window time, the $\overline{\text{RST}}$ will become active (LOW) for a time determined by the RC components of the RT timer plus 10 ms.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

THERMAL SHUTDOWN

To increase the overall safety of the system designed with the 34701, an internal Thermal Shutdown function has been incorporated into the switching regulator circuit. The 34701 senses the temperature of the buck regulator main switching MOSFET (high-side MOSFET M1; see Figure 2 on page 2), the low-side (synchronous MOSFET M2), and control circuit. If the temperature of any of the monitored components exceeds the limit of safe operation (Thermal Shutdown), the switching regulator and the LDO shut down. After the temperature falls below the value given by the Thermal Shutdown hysteresis window, the switcher tries again to operate.

The VOUT pulldown MOSFET M3 has an independent Thermal Shutdown control. If the M3 temperature exceeds the Thermal Shutdown, the M3 is turned off without affecting the switcher operation.

The LDO pulldown MOSFET M4 has an independent Thermal Shutdown control. If the M4 temperature exceeds the Thermal Shutdown, the M4 will be turned off without affecting the LDO operation.

SOFT START

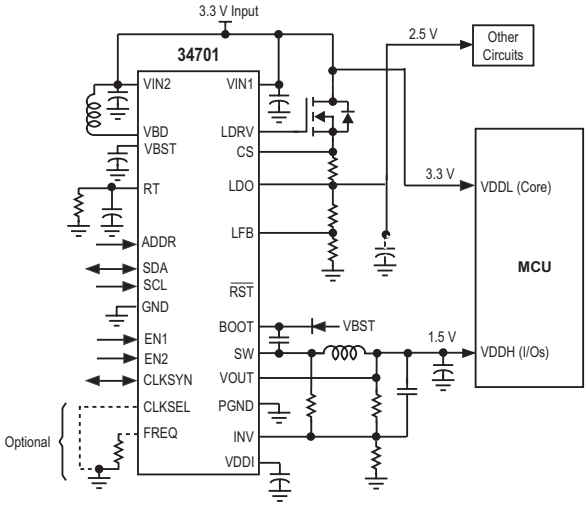
A switching regulator soft start feature is incorporated in the 34701. The soft start is active each time the IC is enabled, VIN is reapplied, or after a fault retry. Other transient events do not activate the soft start.

VOLTAGE MARGINING

The 34701 includes a voltage margining feature accessed through the I^2C bus. Voltage margining allows for independent adjustment of the Switcher VOUT voltage and the linear output VLDO. Each can be adjusted up and down in 1.0% steps to a range of ±7.0%. This feature allows for worst case system validation; i.e., determining the design margin. Margining details are described in the section entitled I^2C Bus Operation, beginning on page 26 of this datasheet.

POWER SEQUENCING MODES

The power sequencing of the two outputs of this power supply IC is in compliance with the Freescale Power QUICC and other 32-bit microprocessor requirements. When the input voltage is applied, the switcher and linear regulator outputs follow the supply rail voltage during power-up and power-down in the limits given by the microcontroller power sequencing specification, illustrated in Figures 17 through 19. There are two possible power sequencing modes, Standard and Inverted, as explained in more detail below. The third mode of operation is Power Sequencing Disabled.



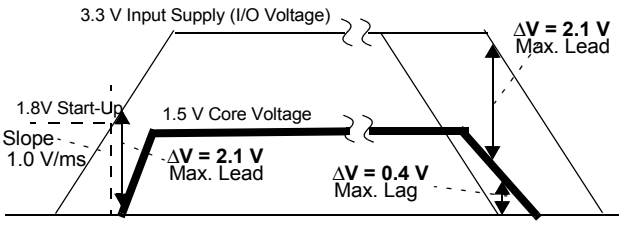


Figure 17. Standard Power Up/Down Sequence in +3.3 V Supply System

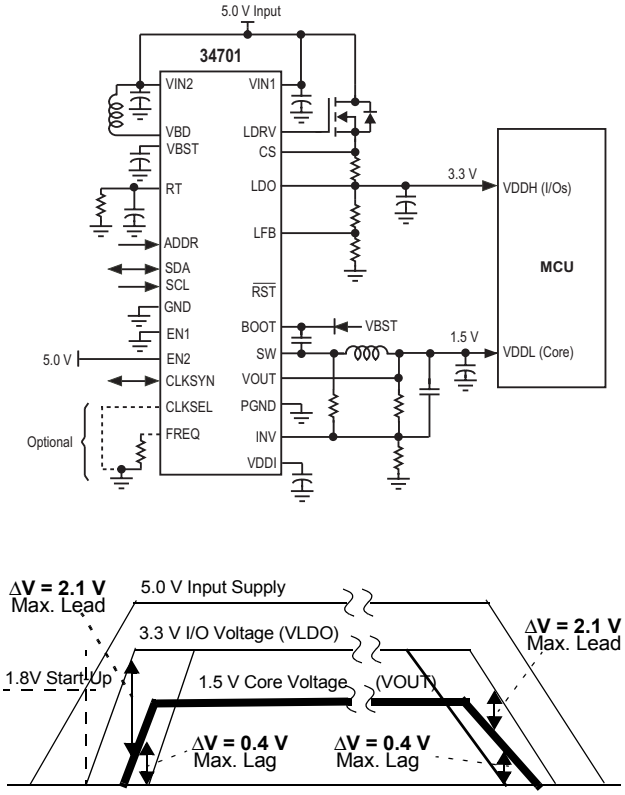


Figure 18. Standard Power Up/Down Sequence in +5.0 V Supply System

STANDARD POWER SEQUENCING

When the power supply IC operates in the Standard Power Sequencing mode, the switcher output provides the core voltage for the microprocessor. This situation and operating conditions are illustrated in Figures 17 and 18. Table 5, page 16, shows the Power Sequencing mode selection.

INVERTED POWER SEQUENCING

When the power supply IC is operating in the Inverted Power Sequencing mode, the linear regulator (LDO) output provides the core voltage for the microprocessor, as illustrated in Figure 19. Table 5 shows the Power Sequencing mode selection.

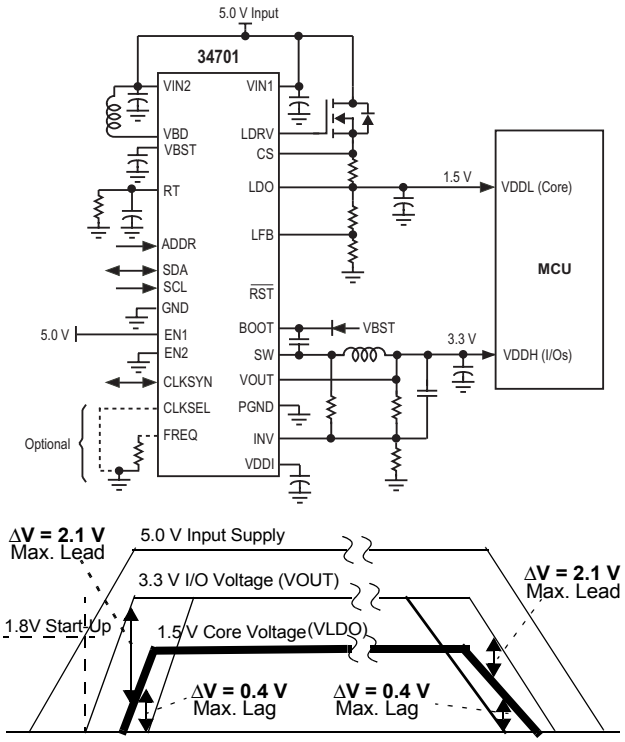


Figure 19. Inverted Power Up/Down Sequence in +5.0 V Supply System

ASSUMED REQUIREMENTS

1. I/O supply voltage not to exceed core voltage by more than 2.0 V.
2. Core supply voltage not to exceed I/O voltage by more than 0.4 V.

Methods of Control

The 34701 has several methods of monitoring and controlling the regulator output voltages, as described in the paragraphs below. Power sequencing control is also achieved through the intrinsic operation of the regulators. The EN1 and EN2 terminals can be used to select the proper power sequencing mode required by the powered system or to disable the power sequencing (refer to Table 5).

Intrinsic Operation

For both the LDO and switcher, whenever the output voltage is below the regulation point, the LDO external Pass MOSFET is on, or the Buck High-Side MOSFET is on at a duty cycle controlled by the switcher. Because these devices are MOSFETs, current can flow in either direction, balancing the voltages via the common supply terminal. The ability to maintain the MOSFETs on is dependent on the available gate voltage, and thus the size of the boost regulator storage capacitor.

Standard Power Sequencing Control

Comparators monitor voltage differences between the LDO (LDO terminal) and the switcher (VOUT terminal) outputs as follows:

1. *LDO > VOUT + 1.9 V, turn off LDO.* The LDO can be forced off. This occurs whenever the LDO output voltage exceeds the switcher output voltage by more than 1.9 V.
2. *LDO > VOUT + 2.0 V, shunt LDO to ground.* If turning off the LDO is insufficient and the LDO output voltage exceeds the switcher output voltage by more than 2.0 V, a 1.5 Ω shunt MOSFET is turned on that discharges the LDO load capacitor to ground. The shunt MOSFET is used for switcher output shorts to ground and for power down in case of VIN1 ≠ VIN2 with the switcher output falling faster than the LDO.
3. LDO < VOUT + 1.9 V cancel (2).
4. *LDO < VOUT + 1.8 V, cancel (1) above, re-enable LDO.* Normal operation resumes when the LDO output voltage is less than 1.8 V above the switcher output voltage.
5. *LDO < VOUT - 0.1 V, turn off switcher.* The switcher can be forced off. This occurs whenever the LDO is less than VOUT - 0.1 V.
6. *LDO < VOUT - 0.3 V, turn on Sync (LS) MOSFET and 1.5 Ω VOUT sink MOSFET.* The Buck High-Side MOSFET is forced off and the Sync MOSFET is forced on. This occurs when the switcher output voltage exceeds the LDO output by more than 300 mV.
7. LDO > VOUT - 0.3 *V, cancel (6).*
8. *LDO > VOUT - 0.1 V, cancel (5).* Normal operation resumes when LDO < VOUT - 0.1 *V.*

Inverted Power Sequencing Control

Comparators monitor voltage differences between the switcher (VOUT terminal) and LDO (LDO terminal) outputs as follows:

1. *VOUT > LDO + 1.8 V, turn off VOUT .* The switcher VOUT can be forced off. This occurs whenever the VOUT output voltage exceeds the LDO output voltage by more than 1.8 V.
2. *VOUT > LDO + 2.0 V, shunt VOUT to ground.* If turning off the switcher VOUT is insufficient and the VOUT output voltage exceeds the LDO output voltage by more than 2.0 V, a 1.5 Ω shunt MOSFET and the switcher synchronous MOSFET are turned on to discharge the VOUT load capacitor to ground. The shunt MOSFET and synchronous MOSFET are used for LDO output shorts to ground and for power-down in case of VIN1 ≠ VIN2 with LDO output falling faster than the VOUT.
3. *VOUT < LDO + 1.8 V, cancel (1) and (2) above, re-enable VOUT .* Normal operation resumes when the VOUT output voltage is less than 1.8 V above the LDO output voltage.
4. VOUT < LDO + 2.0 *V, cancel (2)*
5. *VOUT < LDO - 0.2 V, turn off LDO.* The LDO can be forced off. This occurs whenever the VOUT is less than VLDO - 0.2 V.
6. *VOUT < LDO - 0.3 V, turn on the 1.5 Ω LDO sink MOSFET.* This occurs when the LDO output voltage exceeds the VOUT output by more than 300 mV.
7. VOUT < LDO - 0.2 *V, cancel (6).*
8. *VOUT < LDO - 0.1 V, cancel (5).* Normal operation resumes when VOUT > LDO - 0.1 *V.*

STANDARD OPERATING MODE

Single 3.3 V Supply, VIN = VIN1 = VIN2 = 3.3 V

The 3.3 V supplies the microprocessor I/O voltage, the switcher supplies core voltage (e.g., 1.5 V nominal), and the LDO operates independently (see Figure 17, page 21). Power sequencing depends only on the normal switcher intrinsic operation to control the Buck High-Side MOSFET.

Power-Up

When VIN is rising, initially VOUT is below the regulation point and the Buck High-Side MOSFET is on. In order not to exceed the 2.1 V differential requirement between the I/O (VIN) and the core (VOUT), the switcher must start up at 2.1 V or less and be able to maintain the 2.1 V or less differential. The maximum slew rate for VIN is 1.0 V/ms.

Power-Down

When VIN is falling, VOUT falls below the regulation point; therefore, the Buck High-Side MOSFET is on. In the case where VOUT is falling faster than VIN, the Buck High-Side MOSFET attempts to maintain VOUT. In the case where VIN is falling faster than VOUT, the Buck High-Side MOSFET is also on, and the VOUT load capacitor is discharged through the Buck High-Side MOSFET to VIN. Thus, provided VIN does not fall too fast, the core voltage (VOUT) does not exceed the I/O voltage (VIN) by more than a maximum of 0.4 V.

Shorted Load

1. *VOUT shorted to ground.* This causes the I/O voltage to exceed the core voltage by more than 2.1 V. No load protection.
2. *VIN shorted to ground.* Until the switcher load capacitance is discharged, the core voltage exceeds the I/O voltage by more than 0.4 V. By the intrinsic operation of the switcher, the load capacitor is discharged rapidly through the Buck High-Side MOSFET to VIN.
3. *VOUT shorted to supply.* No load protection. 34701 is protected by current limit and Thermal Shutdown.

Single 5.0 V Supply, VIN1 = VIN2, or Dual Supply VIN1 ≠ VIN2

The LDO supplies the microprocessor I/O voltage. The switcher supplies the core (e.g., 1.5 V nominal) (see Figure 18, page 22).

Power-Up

This condition depends upon the regulator current limit, load current and capacitance, and the relative rise times of the VIN1 and VIN2 supplies. There are two cases:

1. *LDO rises faster than VOUT*. The LDO uses control methods (1) and (2) described in the section Methods of Control on page 22.
2. *VOUT rises faster than LDO.* The switcher uses control methods (5) and (6) described in the section Methods of Control on page 22.

Power-Down

This condition depends upon the regulator load current and capacitance and the relative fall times of the VIN1 and VIN2 supplies. There are two cases:

1. *VOUT falls faster than LDO.* The LDO uses control methods (1) and (2) described in the section Methods of Control on page 22.

   In the case VIN1 = VIN2, the intrinsic operation turns on both the Buck High-Side MOSFET and the LDO external Pass MOSFET, and discharges the LDO load capacitor into the VIN supply.
2. *LDO falls faster than VOUT .* The switcher uses control methods (5) and (6) described in the section Methods of Control on page 22.

Shorted Load

1. *VOUT shorted to ground.* The LDO uses method (1) and (2) described in the section Methods of Control on page 22.
2. *LDO shorted to ground.* The switcher uses control methods (5) and (6) described in the section Methods of Control on page 22.
3. *VIN1 shorted to ground.* Device is not working.
4. *VIN2 shorted to ground with VIN1 and VIN2 different.* This is equivalent to the switcher output shorted to ground.
5. *VOUT shorted to supply.* No load protection. 34701 is protected by current limit and Thermal Shutdown.
6. *LDO shorted to supply.* No load protection. 34701 is protected by current limit and Thermal Shutdown.

INVERTED OPERATING MODE

Single 3.3 V Supply, VIN = VIN1 = VIN2 = 3.3 V

The 3.3 V supplies the microprocessor I/O voltage, the LDO supplies core voltage (e.g., 1.5 V nominal), and the switcher VOUT operates independently. Power sequencing depends only on the normal LDO intrinsic operation to control the Pass MOSFET.

Power-Up

When VIN is rising, initially LDO is below the regulation point and the Pass MOSFET is on. In order not to exceed the 2.1 V differential requirement between the I/O (VIN) and the core (LDO), the LDO must start up at 2.1 V or less and be able to maintain the 2.1 V or less differential. The maximum slew rate for VIN is 1.0 V/ms.

Power-Down

When VIN is falling, LDO falls below the regulation point; therefore, the Pass MOSFET is on. In the case where LDO is falling faster than VIN, the Pass MOSFET attempts to maintain LDO. In the case where VIN is falling faster than LDO, the Pass MOSFET is also on, and the LDO load capacitor is discharged through the Pass MOSFET to VIN. Thus, provided VIN does not fall too fast, the core voltage (LDO) does not exceed the I/O voltage (VIN) by more than maximum of 0.4 V.

Shorted Load

1. *LDO shorted to ground.* This will cause the I/O voltage to exceed the core voltage by more than 2.1 V. No load protection.
2. *VIN shorted to ground.* Until the LDO load capacitance is discharged, the core voltage exceeds the I/O voltage by more than 0.4 V. By the intrinsic operation of the LDO, the load capacitor is discharged rapidly through the Pass MOSFET to VIN.
3. *LDO shorted to supply.* No load protection.

Single 5.0 V Supply, VIN1 = VIN2, or Dual Supply VIN1 ≠ VIN2

The switcher VOUT supplies the microprocessor I/O voltage. The LDO supplies the core (e.g., 1.5 V nominal) (see Figure 19, page 22).

Power-Up

This condition depends upon the regulator current limit, load current and capacitance, and the relative rise times of the VIN1 and VIN2 supplies. There are two cases:

1. *VOUT rises faster than LDO.* The switcher VOUT uses control methods (1) and (2) described in the section Methods of Control on page 22.
2. *LDO rises faster than VOUT .* The LDO uses control methods (5) and (6) described in the section Methods of Control on page 22.

Power-Down

This condition depends upon the regulator load current and capacitance and the relative fall times of the VIN1 and VIN2 supplies. There are two cases:

1. *LDO falls faster than VOUT .* The VOUT uses control methods (4) and (5) described in the section Methods of Control on page 22.

   In the case VIN1 = VIN2, the intrinsic operation turns on both the Buck High-Side MOSFET and the LDO external Pass MOSFET, and discharges the VOUT load capacitor into the VIN supply.
2. *VOUT falls faster than LDO.* The LDO uses control methods (5) and (6) described in the section Methods of Control on page 22.

Shorted Load

1. *LDO shorted to ground.* The VOUT uses methods (1) and (2) described in the section Methods of Control on page 22.
2. *VOUT shorted to ground.* The LDO uses control methods (5) and (6) described in the section Methods of Control on page 22.
3. VIN1 shorted to ground. Device is not working.
4. *VIN2 shorted to ground.* This is equivalent to the switcher VOUT output shorted to ground.
5. *LDO shorted to supply.* No load protection. 34701 is protected by current limit and Thermal Shutdown.
6. *VOUT shorted to supply.* No load protection. 34701 is protected by current limit and Thermal Shutdown.

LOGIC COMMANDS AND REGISTERS

I²C BUS OPERATION

The 34701 device is compatible with the I²C interface standard. SDA and SCL terminals are the Serial Data and Serial Clock terminals of the I²C bus.

I²C COMMAND AND DATA FORMATS

Communication Start

Communication starts with a START condition, followed by the slave device unique address. The Read/Write (R/W) bit defines whether the data should be read from or written to the device (the 34701 operates only as a slave device; therefore, the R/W bit should always be set to 0). The 34701 responds by sending the Acknowledge bit (Ack) to the master device. Figure 20 illustrates the beginning of an I²C communication for a 7-bit slave address.

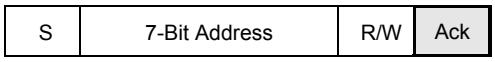


Figure 20. Communication Start Using 7-Bit Address

Slave Address Definition

34701 has the two least significant address bits (LSB) defined by the state of the CLKSEL terminal (A1) and the ADDR terminal (A0).

Note The state of the CLKSEL terminal also defines the configuration of the oscillator synchronization CLKSYN terminal. Leaving the CLKSEL terminal open or pulling it high defines the CLKSYN terminal as an oscillator output. When the CLKSEL terminal is pulled low, the CLKSYN terminal is configured as a synchronization input for the external clock signal.

This feature allows up to four 34701 ICs to communicate in the same I²C bus, all of them sharing the same high-order address bits. A different combination of the two LSB address bits A1 and A0 can be assigned to each individual part to assure its unique address. Figure 21 illustrates the flexible addressing feature for a 7-bit address. Table 6 provides the definition of the selectable portion of the device address.

When the ADDR terminal is used and put to low level, pull the ADDR terminal to ground through a 10 kΩ resistor.

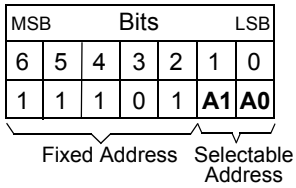


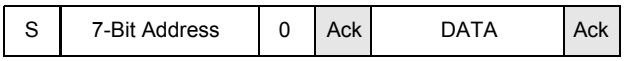
Figure 21. Address Bit Definition for 7-Bit Address

Table 6. Definition of Selectable Portion of Device Address

CLKSEL Terminal	ADDR Terminal	A1	A0
Low	Low	0	0
Low	High (Open)	0	1
High (Open)	Low	1	0
High (Open)	High (Open)	1	1

Writing Data Into the Slave Device

After the address acknowledgment by the slave, DATA can be written into the slave registers. The R/W bit must be set to 0 to allow DATA to be written into the 34702. Figure 22 shows the data write sequence. Actions performed by the slave device are grayed.



(Write)

Figure 22. Data Transfer for Write Operations

DATA Definition

The DATA field in the single Data Transfer contains one or several Command Bytes. The Command Byte identifies the kind of operation required by the master to be performed and has two fields, as illustrated in Figure 23:

1. Address field
2. Value field

The address field is selected from the list in Table 7.

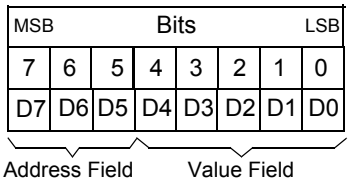


Figure 23. Command Byte

Table 7. Address Field Definitions

Address Field	Operation	Write
001	Voltage Margining	W
011	Watchdog	W

Refer to Table 8, page 27, which summarizes the value field definitions for the entire set of operation options.

Table 8. Command Byte Definitions

Operation	Address			Value					Action
Voltage Margining (As a 2nd Command Byte)	0	0	1	0	0	0	0	0	1st Command
	0	0	1	x	0	0	0	0	Output Nominal
	0	0	1	x	0	0	0	1	+ 1.0%
	0	0	1	x	0	0	1	0	+ 2.0%
	0	0	1	x	0	0	1	1	+ 3.0%
	0	0	1	x	0	1	0	0	+ 4.0%
LDO Output: x=0	0	0	1	x	0	1	0	1	+ 5.0%
Switcher Output x=1	0	0	1	x	0	1	1	0	+ 6.0%
	0	0	1	x	0	1	1	1	+ 7.0%
	0	0	1	x	1	0	0	0	- 1.0%
	0	0	1	x	1	0	0	1	- 2.0%
	0	0	1	x	1	0	1	0	- 3.0%
	0	0	1	x	1	0	1	1	- 4.0%
	0	0	1	x	1	1	0	0	- 5.0%
	0	0	1	x	1	1	0	1	- 6.0%
	0	0	1	x	1	1	1	0	- 7.0%
Watchdog Programming (As a 2nd Command Byte)	0	1	1	0	0	0	0	0	1st Command
	0	1	1	0	0	0	0	0	WD OFF (23)
	0	1	1	0	1	0	0	0	WD 1280 ms Wind. OFF
	0	1	1	0	1	0	0	1	WD 320 ms Wind. OFF
	0	1	1	0	1	0	1	0	WD 80 ms Wind. OFF
	0	1	1	0	1	0	1	1	WD 20 ms Wind. OFF
	0	1	1	0	1	1	0	0	WD 1280 ms Wind. ON
	0	1	1	0	1	1	0	1	WD 320 ms Wind. ON
	0	1	1	0	1	1	1	0	WD 80 ms Wind. ON
	0	1	1	0	1	1	1	1	WD 20 ms Wind. ON

Notes

23. The Watchdog timer is turned ON automatically after receiving any other valid command byte changing watchdog time.

Security in Writing Commands

To improve the security level, a so-called *first command* is defined to initiate each write communications. The first command identifies the operation, which is executed by the following Command Byte.

A first command has the address field equal to the related operation one, followed by a null value field (all zeros). Table 9 summarizes first command definitions. The master sends the first command before the Command Byte for the intended operation.

Table 9. First Command Definitions

First Command	Operation
001 00000	Voltage Margining
011 00000	Watchdog Programming

VOLTAGE MARGINING OPERATION

After starting the communication in Writing mode, the master sends the first command followed by the specific Command Byte to set the required voltage margining for either the LDO or the switcher (see Figure 24). To achieve a simultaneous set for both LDO and switcher, two specific commands must be issued in sequence after the first command, one for each supply.

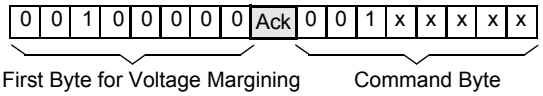


Figure 24. Voltage Margining Programming (One Supply Only)

Note: x bits, which set the voltage margining value are defined in Table 8.

WATCHDOG PROGRAMMING OPERATION

For watchdog operation control, the master periodically sends a watchdog first command followed by a command byte selecting, or confirming, the watchdog period according to the options listed in Table 8. See Figure 25 for the watchdog timer programming command example.

The internal watchdog timer is turned ON by receiving a valid Watchdog Programming command (after receiving the Watchdog Programming First Command), and it is cleared each time the next Watchdog Programming command is written into the device, provided it arrives during the window open time. Thus, the Watchdog Programming command clears the timer and sets the new timing conditions at the same time. The Watchdog Programming First Command 01100000 sent twice shuts the timer OFF, and the watchdog function is disabled. Any other valid watchdog command turns the timer ON again.

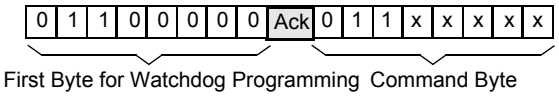


Figure 25. Watchdog Timer Programming

Note: x bits, which set the watchdog timer value are defined in Table 8, page 27.

Communication Stop

Only the master can terminate the data transfer by issuing a STOP condition. The slave waits for this condition to resume its initial state waiting for the next START condition (see Figure 26).

COMPLETE DATA TRANSFER EXAMPLES

The master device controlling the I^2C bus always starts addressing a 34701 slave IC in writing mode (R/W = 0) to enable it to write a Command Byte just after receiving the address acknowledge sent by 34702. I^2C bus protocol defines this circumstance as a master-transmitter and slave-receiver configuration.

Figure 27 illustrates a communication beginning with the slave address, the *first command* for voltage margining, and a third byte containing the address field *001* and the value field *00101* corresponding with the LDO fifth setting (LDO output voltage = +5% above its nominal value). If a simultaneous setting for switcher is needed, a fourth byte should be included before the STOP condition (P); for instance, *001 11100* to set the switcher in its twelfth setting (switcher output voltage = -5% below its nominal value) - see Figure 28.

The example of data transfer setting the Watchdog timer is shown in the Figure 26.

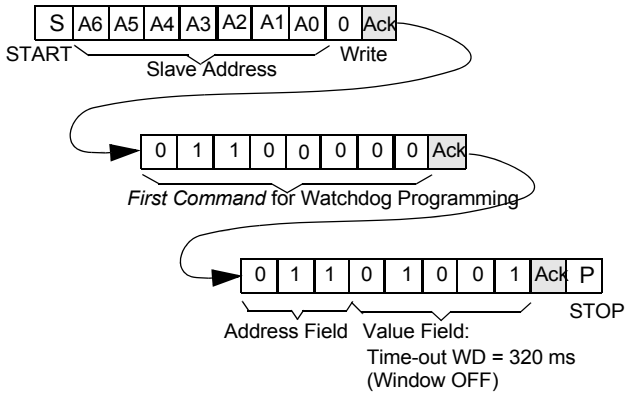


Figure 26. Data Transfer Example - Watch Dog Timer Setting.

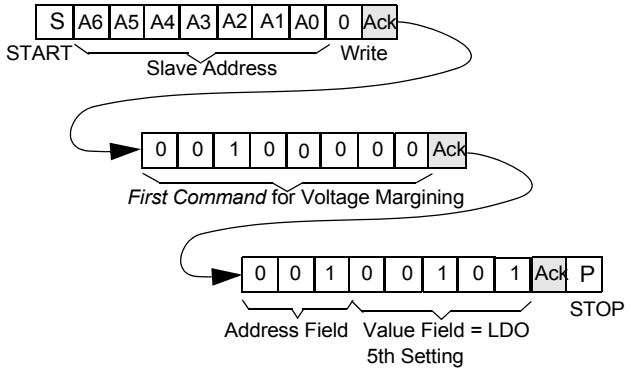


Figure 27. Data Transfer Example - LDO Voltage Margining

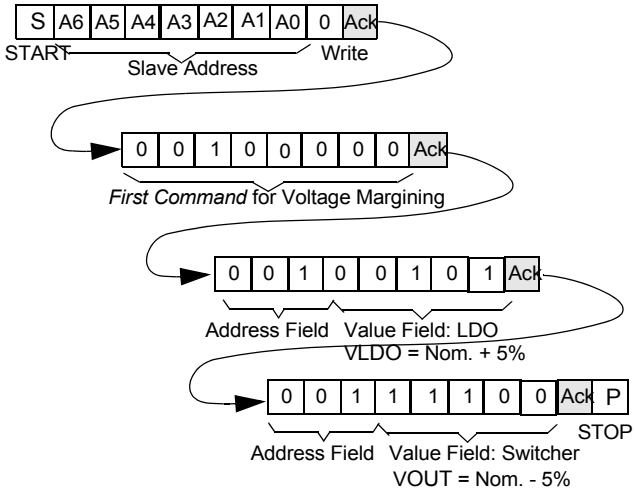


Figure 28. Data Transfer Example - LDO and Switcher Voltage Margining

TYPICAL APPLICATION

BUCK REGULATOR CONTROL CIRCUIT

The 34701 buck regulator utilizes a PWM Voltage Mode topology with Feed-Forward to achieve an excellent line and load regulation. The control circuit block diagram is shown in Figure 29.

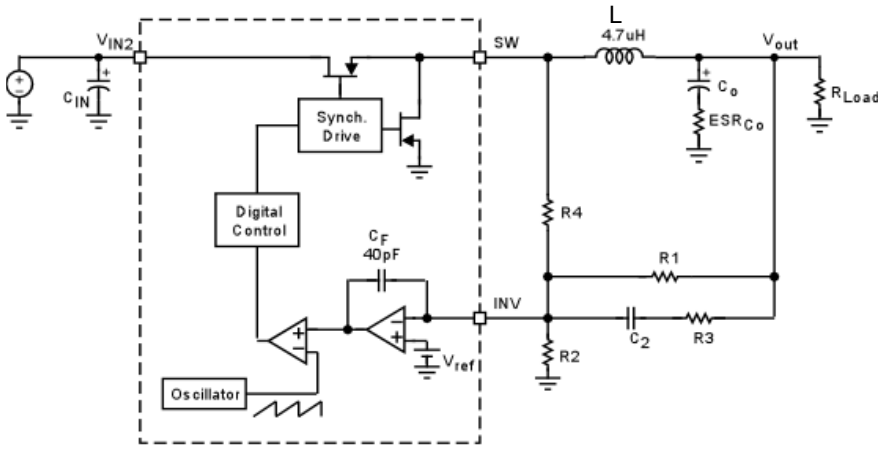


Figure 29. Buck Regulator Control Circuit

The integrated 40 pF capacitor CF charged through the external resistor R4 provides the feed-forward ramp waveform, the amplitude of which is proportional to the input voltage, thus providing the feed-forward function.

Figure 30 shows the Bode plot of the 34701 buck regulator control loop gain and phase versus frequency.

The first double pole on the Bode plot is created by the buck regulator output L-C filter, and its frequency can be calculated as:

$$f_{LC} = \frac{1}{2\pi\sqrt{C_O L}}$$

Where CO is the value of the buck output capacitor and L is the inductance value of the output filter inductor L.

The frequency of the compensating zero can be calculated as follows.

$$f_{z(c)} = \frac{1}{2\pi C2(R1 + R3)}$$

The Feed-Forward implemented by resistor R4 and integrated capacitor CF creates a pole in the overall loop transfer function, the frequency of which can be calculated from the following formula.

$$f_{p(FF)} = \frac{V_{IN}}{\frac{1}{f_{sw}} \times \frac{(V_{IN} - V_{Ref})}{R4C_F} + V_{m1}} \times \frac{1}{2\pi R4C_F}$$

Where VRef is the buck regulator reference voltage (VRef = 0.8 V typ.) at the INV terminal,
VIN is the buck regulator input voltage,
Vm1 is the ramp generated by the internal ramp generator (Vm1 = 0.5 V typ.).

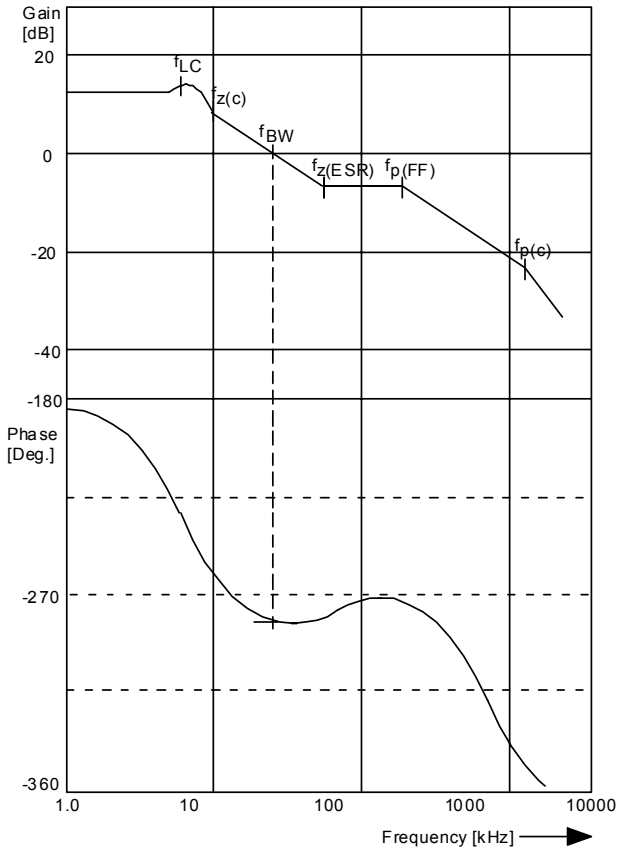


Figure 30. Buck Control Loop Bode Plot

The frequency of the zero created by the ESR of the output capacitor CO is calculated as:

$$f_{z(ESR)} = \frac{1}{2\pi C_O ESR}$$

Where CO is the value of the buck regulator output capacitor, and ESR is the equivalent series resistance of the output capacitor.

The frequency of the compensating network pole can be calculated as follows:

$$f_{p(c)} = \frac{1}{2\pi C2 \frac{R1R3}{(R1+R3)}}$$

The well designed and compensated buck regulator should yield at least 45 deg. phase margin Φm of its overall loop as depicted in the Figure 30, page 29.

Selecting Buck Regulator Output Voltage

The 34701 buck regulator output voltage can be set by selecting the right value of the resistors R1, R2 and R4, and can be determined from the following formula (see Figure 29, page 29 for the component references):

$$R2 = V_{Ref} \times \frac{1}{\frac{(V_O + I_O \times R_L) - V_{Ref}}{R4} + \frac{V_O - V_{Ref}}{R1}}$$

Where VRef is the buck regulator reference voltage (VRef = 0.8 V typ.) at the INV terminal,
VO is the selected output voltage,
IO is the output load current,
RL is the DC resistance of the inductor L.

It is apparent that the buck regulator output voltage is affected by the voltage drop caused by the inductor serial resistance and the regulator output current. In those applications which do not require precise output voltage, setting the formula for calculating selected output voltage can be simplified as follows:

$$R2 = V_{Ref} \times \frac{1}{(V_O - V_{Ref}) \times \frac{(R1+R4)}{R1 \times R4}}$$

Linear Regulator Output Voltage

The output voltage of the linear regulator (LDO) can be set by a simple resistor divider according to the following formula:

$$V_{LDO} = V_{Ref} \times \left(1 + \frac{R_U}{R_L}\right)$$

Where VRef is the linear regulator reference voltage (VRef = 0.8 V typ.) at the LFB terminal,
VLDO is the LDO selected output voltage,
RU is the “upper” resistor of the LDO resistor divider,
RL is the “lower” resistor of the LDO resistor divider.

Figure 31 describes the 34701 linear regulator circuit with the resistor divider RU, RL setting the output voltage VLDO.

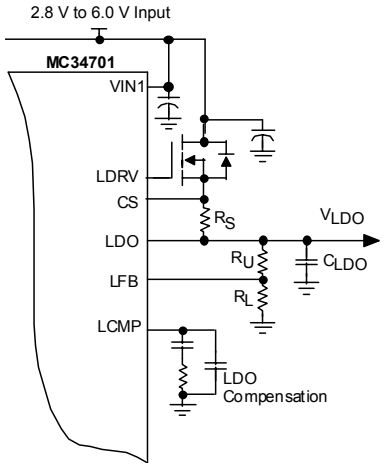


Figure 31. 34701Linear Regulator Circuit

Linear Regulator Current Limit

As described in the Linear Regulator Functional Description section, the current limit of the linear regulator can be adjusted by means of an external current sense resistor RS. The voltage drop caused by the regulator output current flowing through the current sense resistor RS is sensed between the LDO and the CS terminals. When the sensed voltage exceeds 50 mV (typical), the current limit timer starts to time out while the control circuit limits the output current. If the overcurrent condition lasts for more than 10 ms, the linear regulator is shut off and turned on again after 100 ms. This type of operation provides equivalent protection to the analog “current foldback” operation.

It is important to keep in mind that the amount of capacitive load which can be supplied by the by the linear regulator is limited by the setting of the LDO current limit. During the power-up period, the linear regulator operates in the current limit, supplying the current into the load of the LDO, which includes all the capacitors connected to the regulator output. If the total amount load is so large that the regulator could not reach its regulation voltage in 10 ms during the power-up, it turns off and tries to power up again after 100 ms. This situation may lead to the power-up oscillations.

Linear Regulator External MOSFET

The linear regulator uses an external N-channel power MOSFET to provide a pass element for the power path. The selection of the proper type of the external power MOSFET is critical for optimum performance and safe operation of the linear regulator.

The power MOSFET’s threshold voltage, RDS(on), gate charge, capacitances and transconductance are important parameters for the stable operation of the linear regulator while the package of the power MOSFET determines the

maximum power dissipation, and hence the maximum output current for the required input-to-output voltage drop. The power dissipation of the external MOSFET can be calculated from the simple formula:

$$P_{D(Q)} = I_{LDO} \times (V_{IN} - V_{LDO})$$

Where PD(Q) is the power MOSFET power dissipation
VIN is the LDO input voltage,
VLDO is the LDO output voltage,
ILDO is the LDO output load current.

Table 10 shows the recommended power MOSFET types for the 34701 linear regulator, their typical power dissipation, and thermal resistance junction-to-case.

Table 10. Recommended Power MOSFETs

Part No.	Package	Typ. PD	RthJ-C
IRL2703S	D2PAK	2.0 W	3.3 °C/W
MTD20N03HDL	DPAK	1.75 W*	1.67 °C/W

NOTE: Freescale does not assume liability, endorse, or warrant components from external manufacturers referenced in figures or tables. Although Freescale offers component recommendations, it is the customer's responsibility to validate their application.

*When mounted to an FR4 using 0.5 sq.in. drain pad size

The maximum power dissipation is limited by the maximum operating junction temperature TJmax. The allowed power dissipation in the given application can be calculated from the following expression:

$$P_{D(Q)max} \leq \frac{T_{Jmax} - T_A}{R_{thJC} + R_{thCB} + R_{thBA}}$$

Where PD(Q)max is the power MOSFET maximum allowed dissipation,
TJmax is the power MOSFET maximum operating junction temperature,
T_A is the ambient temperature,
RthJC is the power MOSFET thermal resistance junction-to-case,
RthCB is the thermal resistance case-to-board,
RthBA is the thermal resistance board-to-ambient of the PC board.

PCB Layout Considerations

As with any power application, the proper PCB layout plays a critical role in the overall power regulator performance. While good careful printed circuit board layout significantly improves regulation parameters and electromagnetic compatibility (EMC) performance of the switching regulator, poor layout practices can lead not only to significant degradation of regulation and EMC parameters but even to total dysfunction of the whole regulator IC.

Extreme care should be taken when laying out the ground of the regulator circuit. In order to avoid any inductive or capacitive coupling of the switching regulator noise into the sensitive analog control circuits, the noisy power ground and the clean quiet signal ground should be well separated on the printed circuit board, and connected only at one connection point. The power routing should be made by heavy traces or areas of copper. The power path and its return should be placed, if possible, atop each other on the different layers or opposite sides of the PC board. The switching regulator input and output capacitors should be physically placed very close to the power terminals (VIN2, SW, PGND) of the 34701 switching regulator; and their ground terminals, together with the 34701 power ground terminals (PGND), should be connected by a single island of the power ground copper to create the "single-point" grounding. Figure 32 illustrates the 34701 switching regulator grounding concept. The bootstrap capacitor Cb should be tightly connected to the integrated circuit as well.

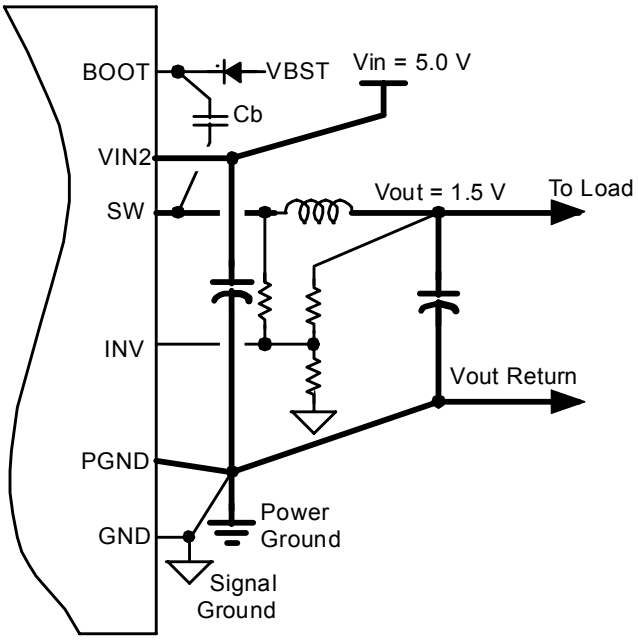


Figure 32. 34701 Buck Regulator Layout

The same guidelines as those for the layout of the main switching buck regulator should be applied to the layout of the low power auxiliary boost regulator and to some extent, the power path of the linear regulator.

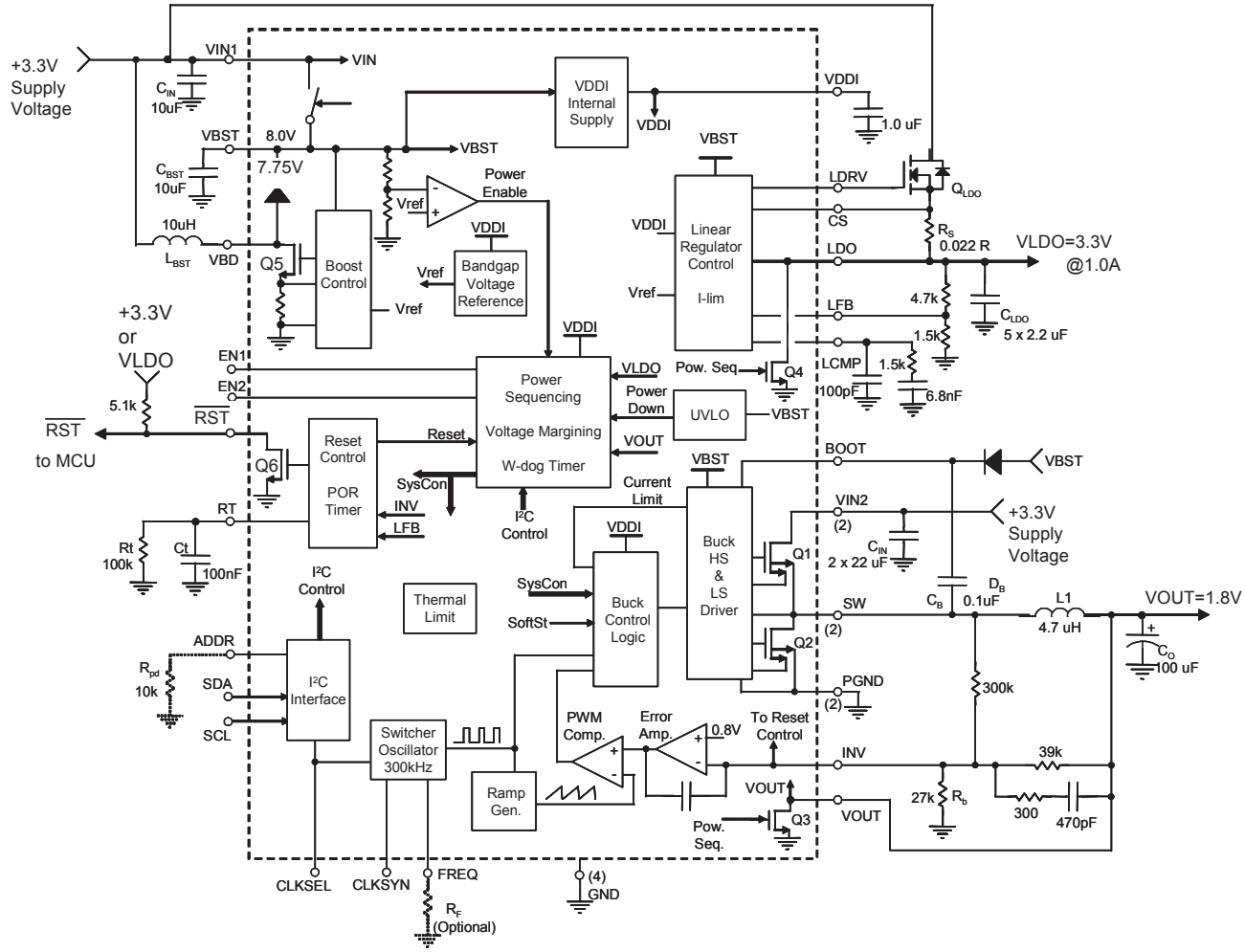


Figure 33. Simplified Block Diagram and Basic Application

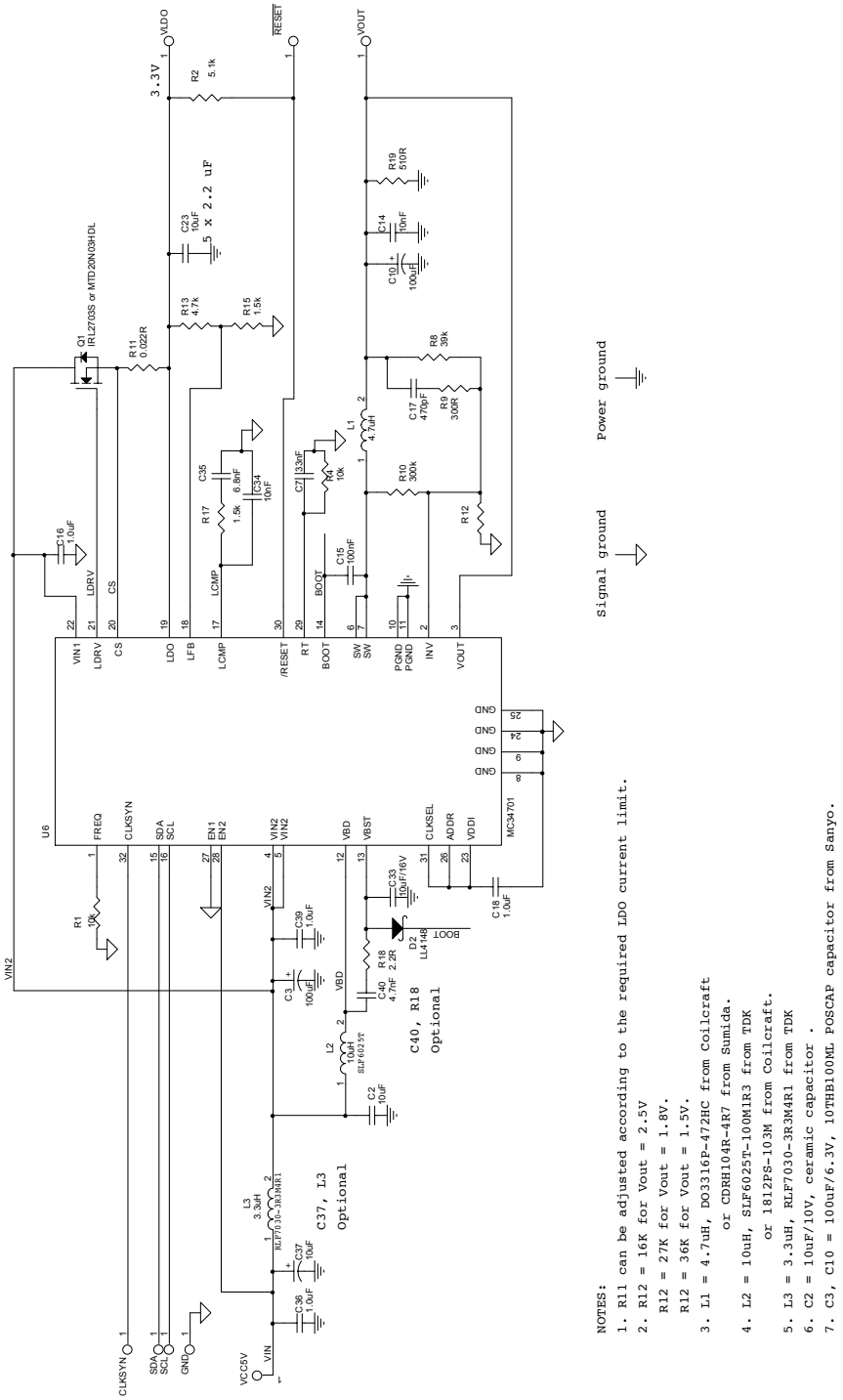


Figure 34. 34701 Typical Application Circuit

PACKAGE DIMENSIONS

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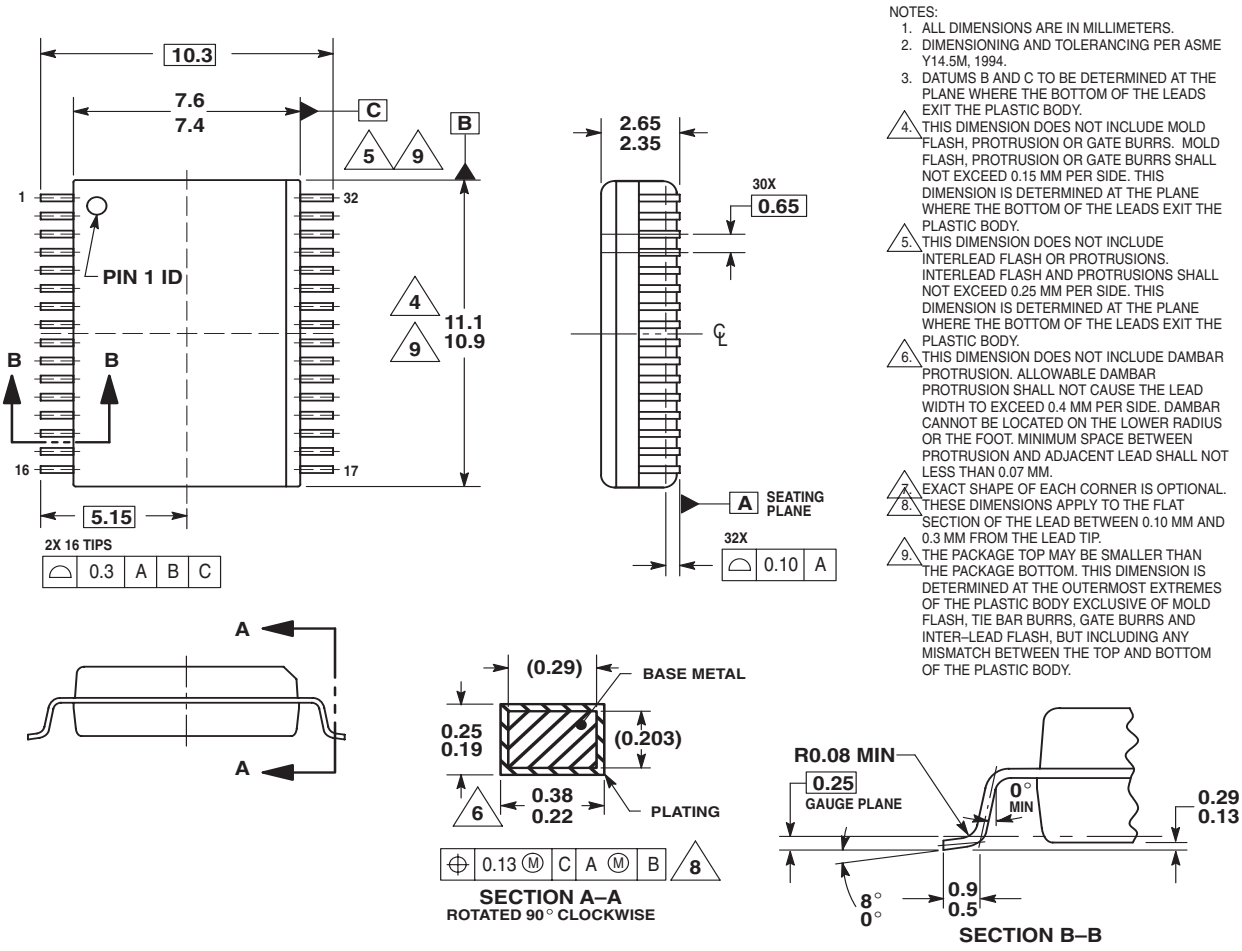

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