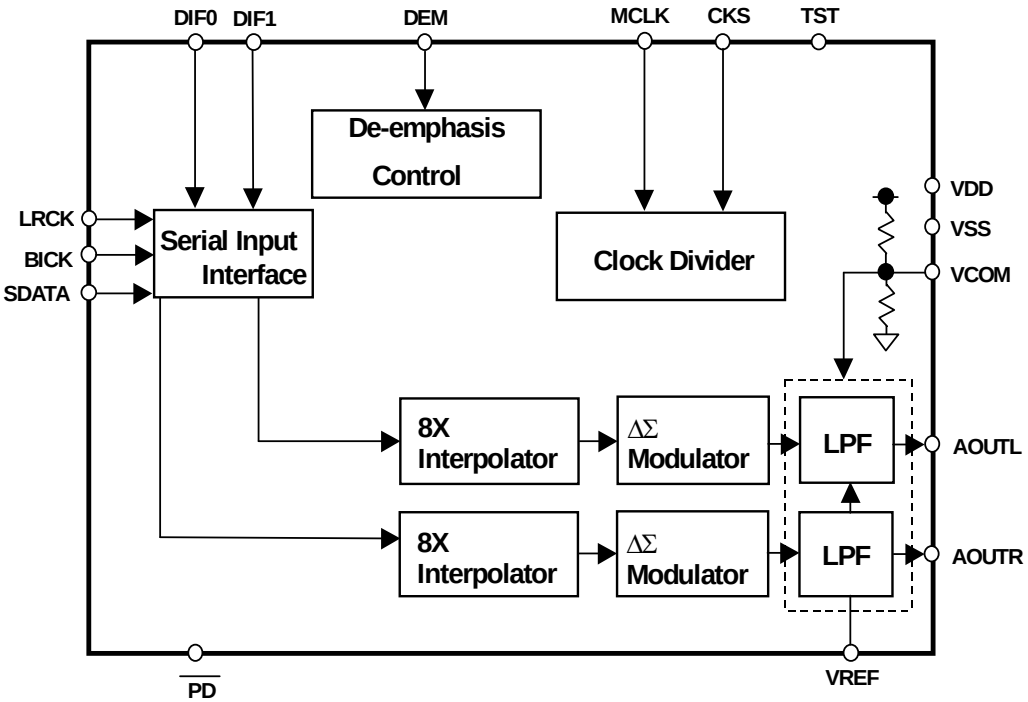
AK4351
18Bit Advanced Multi Bit ΔΣ 2ch DAC

GENERAL DESCRIPTION

The AK4351 is a high cost performance 18bit stereo DAC for low-end digital audio systems. The modulator in the AK4351 uses the new developed Advanced Multi Bit architecture with wide dynamic range. The analog outputs are filtered in the analog domain by a combination of SCF and CTF. Therefore, any external filters are not required. The SCF techniques also improve the loss of accuracy from clock jitter. Therefore, the AK4351 is suitable for the system like STB including PLL circuit. The AK4351 is available in very small 16pin TSSOP package, which reduces system space.

FEATURES

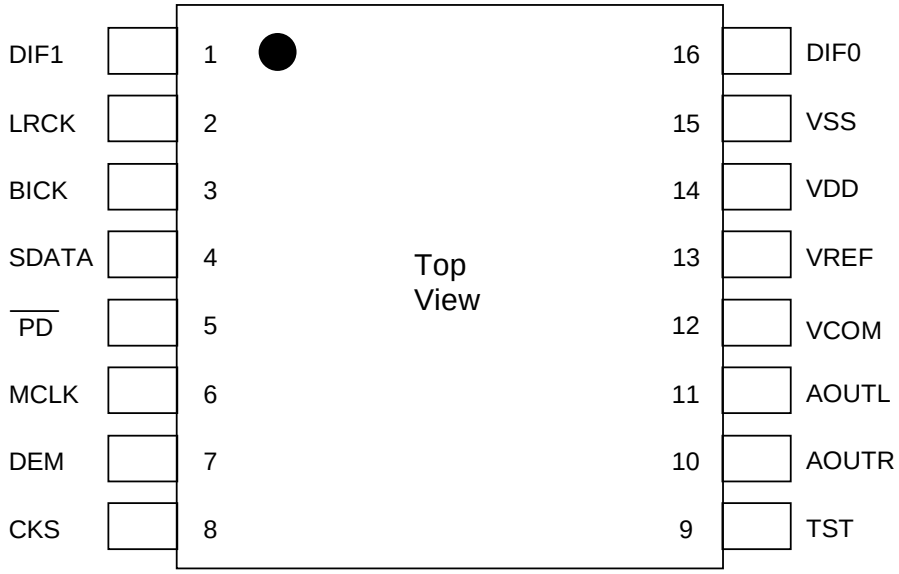
- **Sampling Rate Ranging from 8kHz to 50kHz**
- **128 times Oversampling**
- **Perfect filtering**
  - **18bit 8 times FIR Interpolator with 57dB attenuation**
  - **2nd order LPF**
  - **Total Response: ± 0.2dB at 20kHz**
- **On chip Buffer with Single End Output**
- **Digital de-emphasis for 44.1kHz sampling**
- **I/F format: MSB justified, 16/18bit LSB justified or I^2S**
- **Master clock: 256fs or 384fs**
- **TTL Level Digital Interface**
- **THD+N: -88dB**
- **D-Range: 96dB**
- **High Tolerance to Clock Jitter**
- **Power supply: 4.5 to 5.5V**
- **Very Small Package: 16pin TSSOP (6.4mm x 5.0mm)**



■ Ordering Guide

AK4351VT	-40 ~ +85°C	16pin TSSOP (0.65mm pitch)
AKD4351	Evaluation Board for AK4351	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	DIF1	I	Digital Input Format Pin (Internal Pull-down pin)
2	LRCK	I	L/R Clock Pin
3	BICK	I	Audio Serial Data Clock Pin
4	SDATA	I	Audio Serial Data Input Pin
5	$\overline{PD}$	I	Power-Down Mode Pin When at "L", the AK4351 is in power-down mode and is held in reset. The AK4351 should always be reset upon power-up.
6	MCLK	I	Master Clock Input Pin An external TTL clock should be input on this pin.
7	DEM	I	De-emphasis Enable Pin When at "H", de-emphasis of fs=44.1kHz is enabled.
8	CKS	I	Master Clock Select Pin (Internal Pull-down pin) "L": MCLK=256fs, "H": MCLK=384fs
9	TST	O	Test Pin Must be left floating.
10	AOUTR	O	Rch Analog Output Pin
11	AOUTL	O	Lch Analog Output Pin
12	VCOM	O	Common Voltage Pin, VDD/2 Normally connected to VSS with a 0.1µF ceramic capacitor in parallel with a 10µF electrolytic cap.
13	VREF	I	Voltage Reference Input Pin The differential Voltage between this pin and VSS set the analog output range. Normally connected to VDD.
14	VDD	-	Power Supply Pin
15	VSS	-	Ground Pin
16	DIF0	I	Digital Input Format Pin (Internal Pull-down pin)

Note: All input pins except pull-down pins should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(VSS=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supply	VDD	-0.3	6.0	V
Input Current, Any Pin Except Supplies	IIN	-	±10	mA
Input Voltage	VIND	-0.3	VDD+0.3	V
Ambient Operating Temperature	Ta	-40	85	°C
Storage Temperature	Tstg	-65	150	°C

Note:1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS=0V; Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supply	VDD	4.5	5.0	5.5	V
Voltage Reference (Note 2)	VREF	3.0	-	VDD	V

Note:2. Analog output voltage scales with the voltage of VREF.
AOUT (typ.@0dB)=3.45Vpp*VREF/5.

*AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VDD=5.0V; fs=44.1kHz; BICK=64fs; Signal Frequency=1kHz; 18bit Input Data;
Measurement frequency=10Hz ~ 20kHz; $R_L \geq 5k\Omega$; unless otherwise specified)

Parameter		min	typ	max	Units
Resolution				18	Bits
Dynamic Characteristics	(Note 3)				
THD+N	(0dB Output)		-88	-80	dB
Dynamic Range	(-60dB Output, A-weight)	90	96		dB
S/N	(A-weight)	90	96		dB
Interchannel Isolation (1kHz)		96	100		dB
Interchannel Gain Mismatch			0.2	0.5	dB
DC Accuracy					
Gain Drift			100	-	ppm/°C
Output Voltage	(Note 4)	3.20	3.45	3.70	Vpp
Load Resistance		5			kΩ
Output Current				400	µA
Power Supplies					
Power Supply Current					
Normal Operation ($\overline{PD}$ ="H")					
VDD			14	20	mA
Power-Down Mode ($\overline{PD}$ ="L")					
VDD	(Note 5)		10	50	µA
Power Dissipation (VDD)					
Normal Operation			70	100	mW
Power-Down Mode	(Note 5)		50	250	µW
Power Supply Rejection	(Note 6)		40		dB

Note: 3. Measured by AD725C (SHIBASOKU). Averaging mode. Refer to the evaluation board manual.
4. Full-scale voltage (0dB). Output voltage scales with the voltage of VREF.
AOUT (typ.@0dB)=3.45Vpp*VREF/5.
5. Power Dissipation in the power-down mode is applied with no external clocks
(MCLK, BICK and LRCK held "VDD" or "VSS").
6. PSR is applied to VDD with 1kHz, 100mVpp. VREF pin is held +5V.

FILTER CHARACTERISTICS

(Ta=25°C; VDD=4.5 ~ 5.5V; fs=44.1kHz; DEM="L")

Parameter	Symbol	min	typ	max	Units
Digital filter					
Passband ±0.05dB (Note 7)	PB	0		20.0	kHz
-6.0dB		-	22.05	-	kHz
Stopband (Note 7)	SB	24.1			kHz
Passband Ripple	PR			± 0.02	dB
Stopband Attenuation	SA	54			dB
Group Delay (Note 8)	GD	-	19.1	-	1/fs
Digital Filter + LPF					
Frequency Response 0 ~ 20.0kHz		-	± 0.2	-	dB

Note: 7. The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs (@±0.05dB), SB=0.546*fs.
8. The calculating delay time which occurred by digital filtering. This time is from setting the 16/18bit data of both channels to input register to the output of analog signal.

DIGITAL CHARACTERISTICS

(Ta=25°C; VDD=4.5 ~ 5.5V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	2.2	-	-	V
Low-Level Input Voltage	VIL	-	-	0.8	V
High-Level Output Voltage (Iout=-80μA)	VOH	VDD-0.4	-	-	V
Low-Level Output Voltage (Iout=80μA)	VOL	-		0.4	V
Input Leakage Current (Note 9)	Iin	-	-	± 10	μA

Note: 9. DIF0, DIF1 and CKS pins have internal pull-down devices, normally 100kΩ.

SWITCHING CHARACTERISTICS

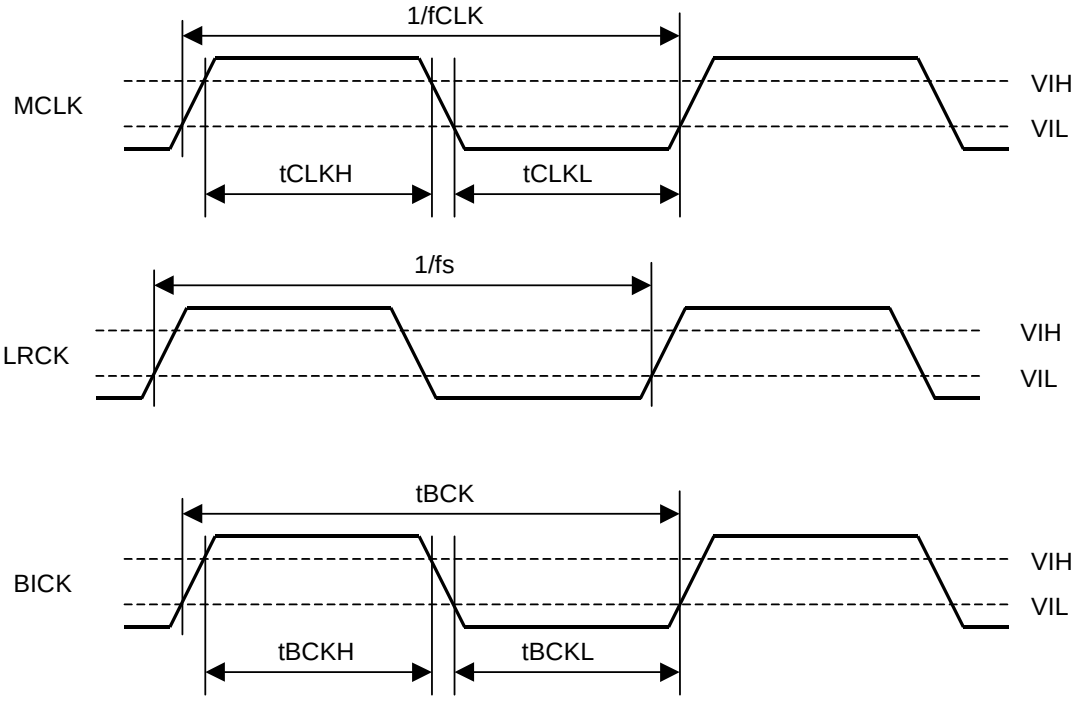
(Ta=25°C; VDD=4.5 ~ 5.5V; C_L=20pF)

Parameter		Symbol	min	typ	max	Units
Master Clock Timing	256fs:	fCLK	2.048	11.2896	12.8	MHz
	Pulse Width Low	tCLKL	28			ns
	Pulse Width High	tCLKH	28			ns
	384fs:	fCLK	3.072	16.9344	19.2	MHz
	Pulse Width Low	tCLKL	20			ns
	Pulse Width High	tCLKH	20			ns
LRCK Frequency		fs	8	44.1	50	kHz
Duty Cycle		Duty	45		55	%
Serial Interface Timing						
BICK Period		tBCK	312.5			ns
BICK Pulse Width Low		tBCKL	100			ns
Pulse Width High		tBCKH	100			ns
BICK rising to LRCK Edge	(Note 10)	tBLR	50			ns
LRCK Edge to BICK rising	(Note 10)	tLRB	50			ns
SDATA Hold Time		tSDH	50			ns
SDATA Setup Time		tSDS	50			ns
Reset Timing						
$\overline{\text{PD}}$ Pulse Width	(Note 11)	tPD	100			ns

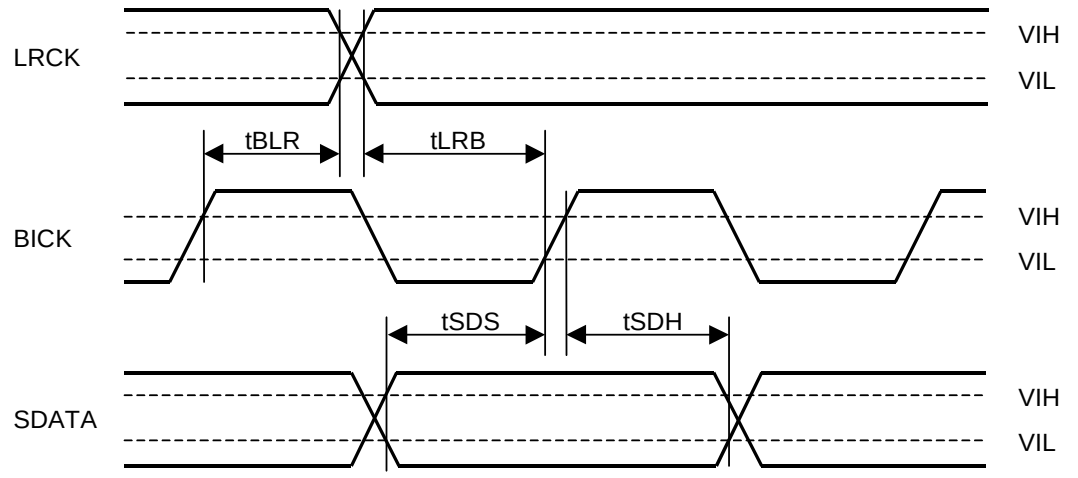
Note: 10. BICK rising edge must not occur at the same time as LRCK edge.

11. The AK4351 can be reset by bringing $\overline{\text{PD}}$ = "L".
When clocks are changed during the operation, please reset the AK4351 at once by $\overline{\text{PD}}$ = "L".

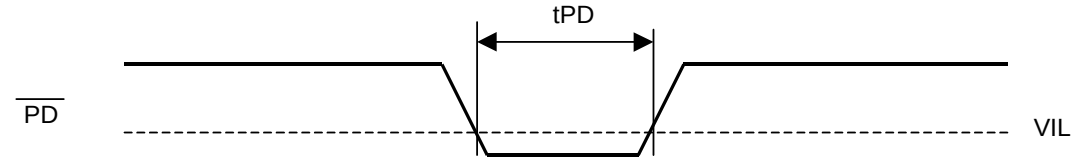
■ **Timing Diagram**



Clock Timing



Serial Interface Timing



Power-down

OPERATION OVERVIEW

■ System Clock

The external clocks, which are required to operate the AK4351, are MCLK, LRCK and BICK. The master clock (MCLK) should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. The frequency of MCLK is determined by the sampling rate (LRCK) and CKS pin. Table 1 illustrates corresponding clock frequencies. When the 384fs is selected, the internal master clock becomes 256fs(=384fs*2/3).

All external clocks (MCLK, BICK and LRCK) should always be present whenever the AK4351 is in normal operation mode ($\overline{PD}$ = "H"). If these clocks are not provided, the AK4351 may draw excess current because the device utilizes dynamic refreshed logic internally. The AK4351 should be reset by $\overline{PD}$ = "L" after these clocks are provided. If the external clocks are not present, the AK4351 should be in the power-down mode($\overline{PD}$ = "L"). After exiting reset at power-up etc., the AK4351 is in power-down mode until MCLK and LRCK are input. When those clocks are changed during the operation, please reset the AK4351 at once by $\overline{PD}$ = "L".

Clock		frequency
LRCK (fs)		8k ~ 50kHz
BICK		~ 64fs
MCLK	CKS = "L"	256fs
	CKS = "H"	384fs

Table 1. System Clocks

■ Audio Serial Interface Format

Data is shifted in via the SDATA pin using BICK and LRCK inputs. The DIF0-1 pins as shown in Table 2 can select four serial data modes. In all modes the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 2 can be used for 16MSB justified formats by zeroing the unused LSBs.

DIF1	DIF0	Mode	BICK	Figure
0	0	0: 16bit LSB Justified	≥32fs	Figure 1
0	1	1: 18bit LSB Justified	≥36fs	Figure 1
1	0	2: 18bit MSB Justified	≥36fs	Figure 2
1	1	3: I^2S Compatible	≥36fs or 32fs	Figure 3

Table 2. Serial Data Modes

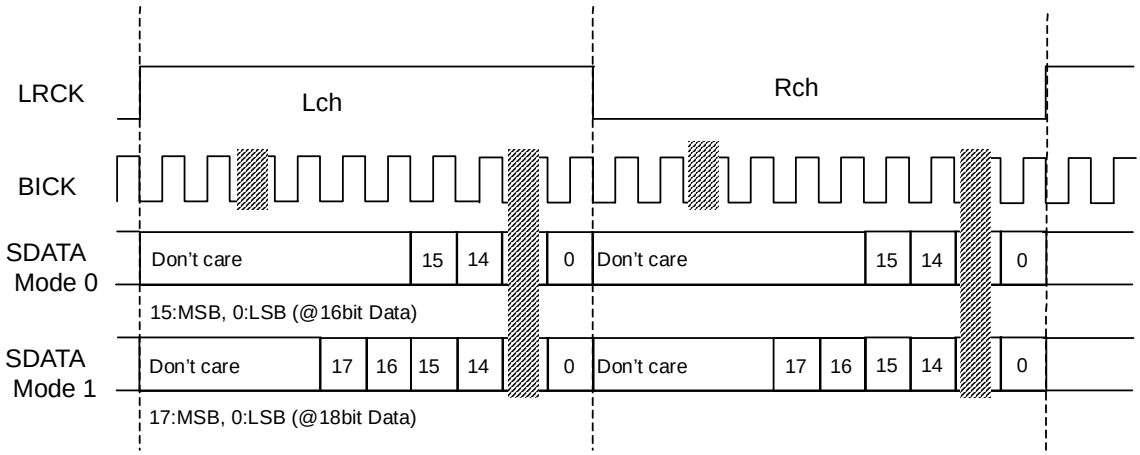


Figure 1. Mode 0,1 Timing

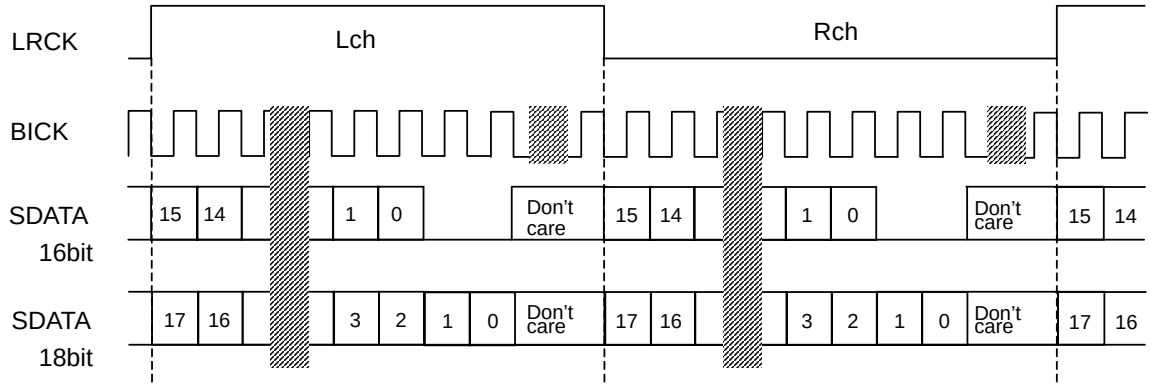


Figure 2. Mode 2 Timing

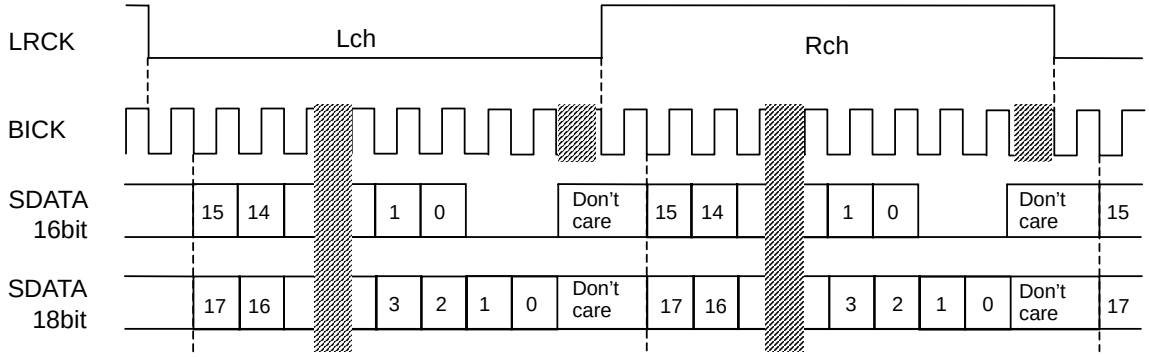


Figure 3. Mode 3 Timing

■ De-emphasis filter

The AK4351 includes the digital de-emphasis filter (tc=50/15µs) by IIR filter. This filter corresponds to 44.1kHz sampling. Setting DEM pin "H" enables the de-emphasis.

■ Power-down

The AK4351 is placed in the power-down mode by bringing $\overline{PD}$ pin "L" and the anlog outputs are floating(Hi-Z). Figure 4 shows an example of the system timing at the power-down and power-up.

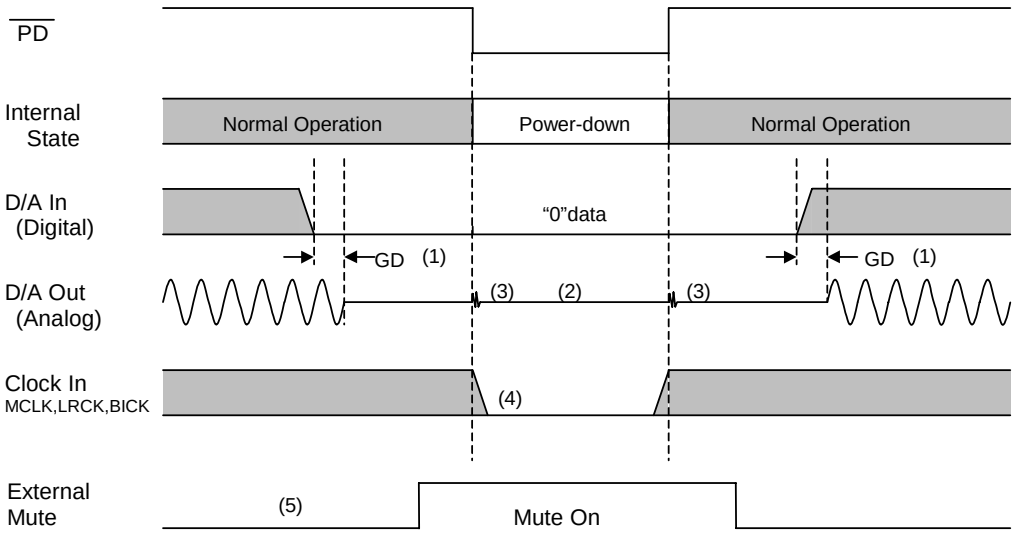


Figure 4. Power-down/up sequence example

Notes:

(1) Analog output corresponding to digital input has the group delay (GD).

(2) Analog outputs are floating (Hi-Z) at the power-down mode.

(3) Click noise occures at the edges("↑ ↓") of the falling edge of $\overline{PD}$ signal.

(4) When the external clocks(MCLK,BICK,LRCK) are stopped, the AK4351 should be in the power-down mode.

(5) Please mute the analog output externally if the click noise(3) influences system application. The timing example is shown in this figure.

■ System Reset

The AK4351 should be reset once by bringing $\overline{PD}$ = "L" upon power-up. The AK4351 is powered up and the internal timing starts clocking by LRCK "↑" after exiting reset and power down state by MCLK. The AK4351 is in power-down mode until MCLK and LRCK are input.

SYSTEM DESIGN

Figure 5 shows the system connection diagram. An evaluation board [AKD4351] is available in order to allow an easy study on the layout of a surrounding circuit.

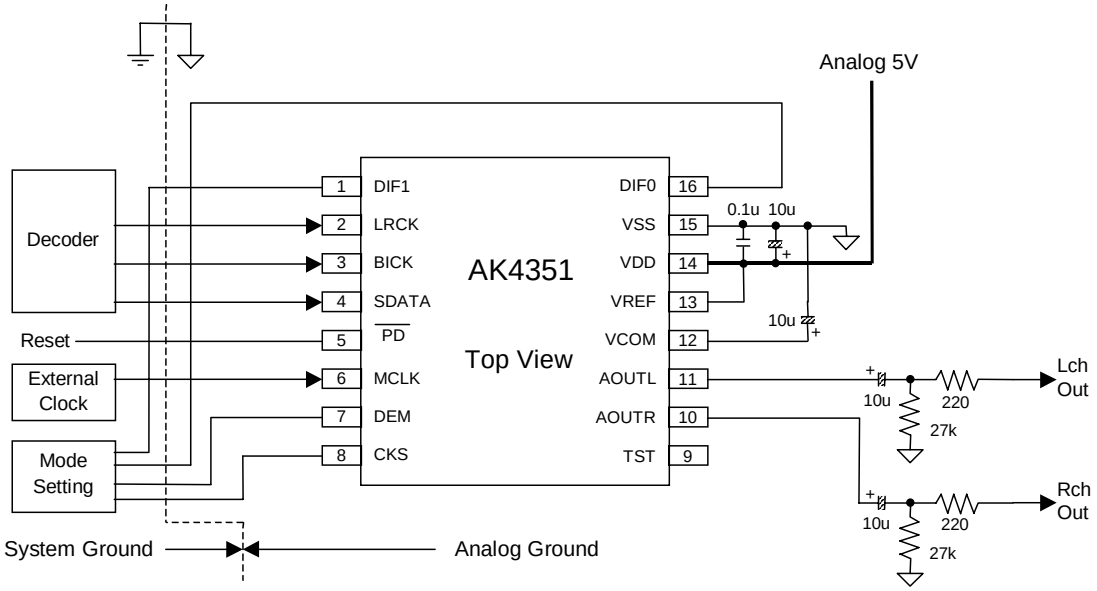


Figure 5. Typical Connection Diagram

Notes:

- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- ALL input pins except internal pull-down pins should not be left floating.
- Decoupling capacitor, especially 0.1µF ceramic capacitor for high frequency should be placed as near to VDD and VREF pins as possible.
- System ground including DSP/µP should be separated from AK4351's VSS. Both grounds should be connected by one point at power supply or regulator on system board.

1. Grounding and Power Supply Decoupling

VDD and VSS are supplied from analog supply and should be separated from system digital supply. Decoupling capacitor, especially 0.1μF ceramic capacitor for high frequency should be placed as near to VDD as possible.

2. Voltage Reference

The differential Voltage between VREF and VSS sets the analog output range. VREF pin is normally connected to VDD with a 0.1μF ceramic capacitor. VCOM is a signal ground of this chip. An electrolytic capacitor 10μF parallel with a 0.1μF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. ALL signals, especially clocks, should be kept away from the VREF and VCOM pins in order to avoid unwanted coupling into the AK4351.

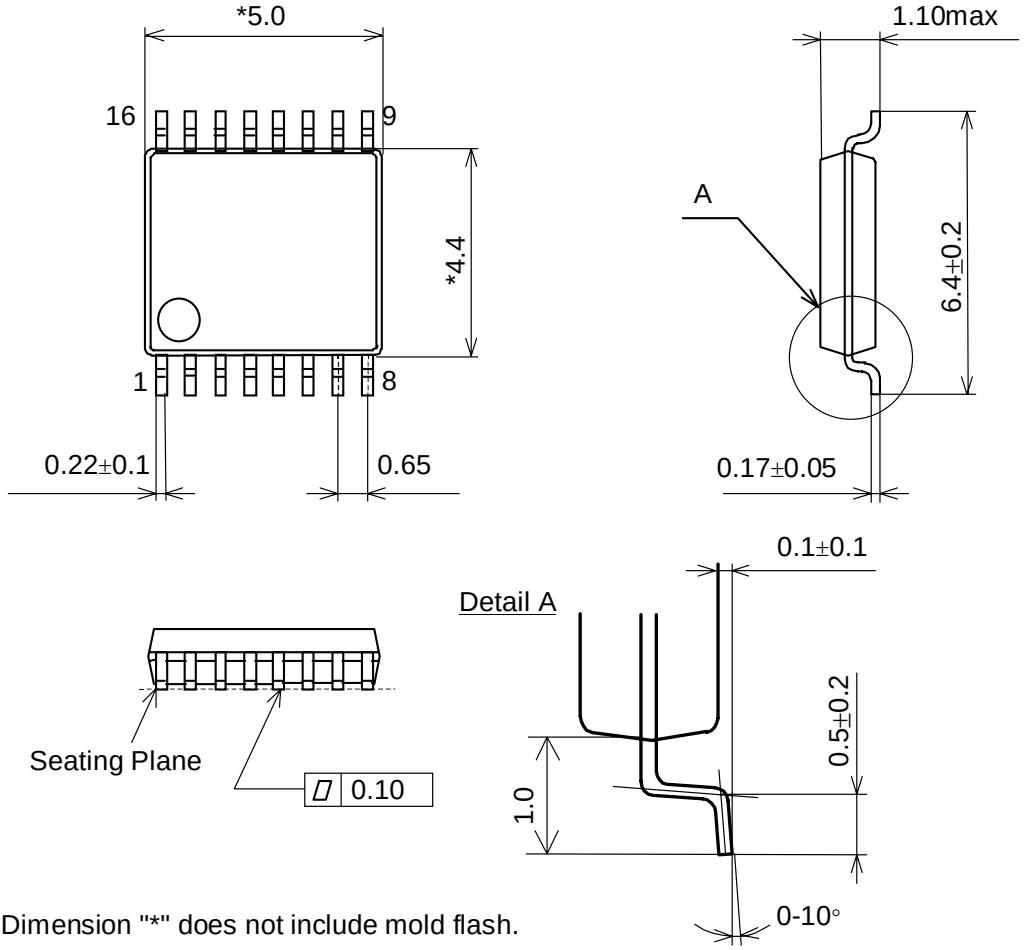
3. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The output signal range is typically 3.45Vpp. AC coupling capacitors of larger than 1μF are recommended. The internal switched-capacitor filter and continuous-time filter attenuate the noise generated by the delta-sigma modulator beyond the audio passband. Therefore, any external filters are not required for typical application. The output voltage is a positive full scale for 7FFFH(@16bit) and a negative full scale for 8000H(@16bit). The ideal output is VCOM voltage for 0000H(@16bit).

DC offsets on analog outputs are eliminated by AC coupling since analog outputs have DC offsets of VCOM + a few mV.

PACKAGE

16pin TSSOP (Unit: mm)

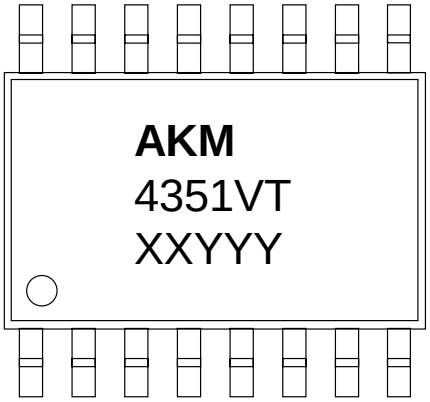


NOTE: Dimension "*" does not include mold flash.

■ **Package & Lead frame material**

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate

MARKING



Contents of XXYYY
XX: Lot#
YYY: Date Code

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