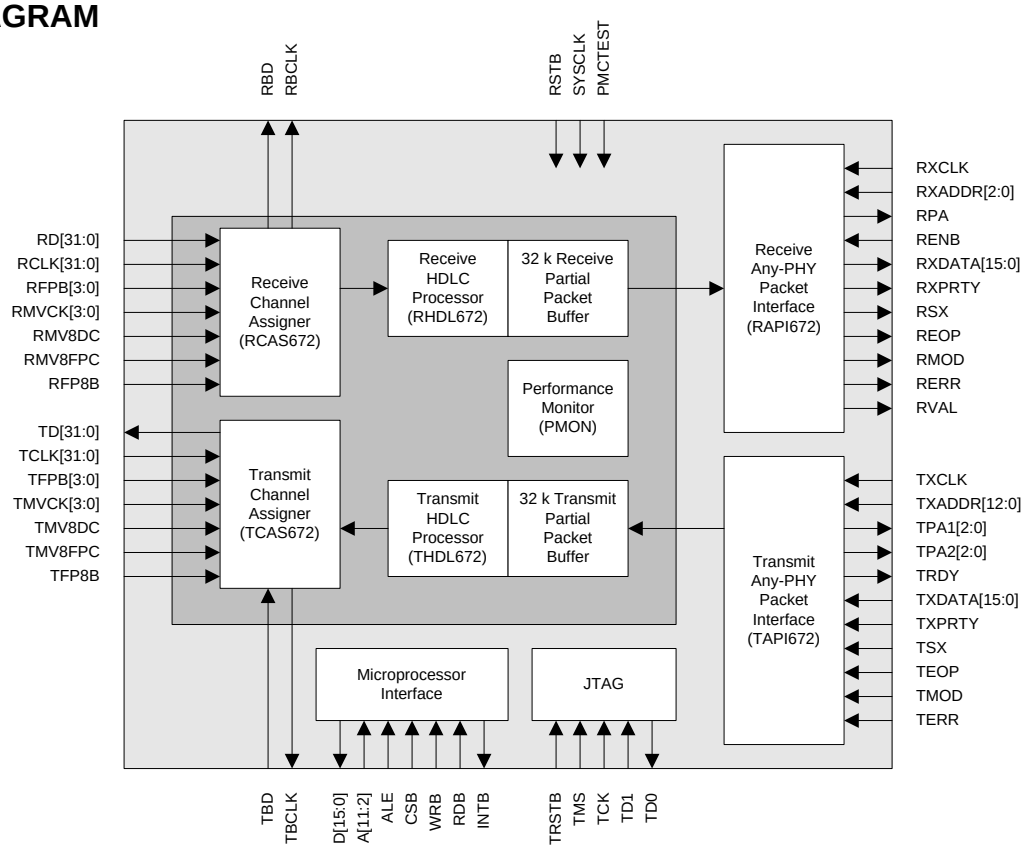
Frame Engine and Data Link Manager

FEATURES

The FREEDM-32A672 chip offers the following features:

- Single-chip multi-channel HDLC controller with a 50 MHz, 16-bit Any-PHY Packet Interface (APPI) for transfer of packet data using an external controller. Each APPI bus can support up to seven FREEDM-32A672 devices to enable high-density and low-latency applications.
- Supports up to 672 bi-directional HDLC channels assigned to a maximum of 32 MVIP digital telephony buses at 2.048 Mbit/s per link, or 8 H-MVIP buses at 8.192 Mbit/s per link.
- Supports up to 672 bi-directional HDLC channels assigned to a maximum of 32 channelized T1/J1/E1 links. You can program the number of time-slots assigned to an HDLC channel from 1 to 24 (for T1/J1) and from 1 to 31 (for E1).
- Supports up to 32 bi-directional HDLC channels, each assigned to an unchannelized arbitrary-rate link, subject to a maximum aggregate link clock-rate of 64 MHz in each direction.
- Channels assigned to links 0 to 2 support clock rates up to 52 MHz. Channels assigned to links 3 to 31 support clock rates up to 10 MHz. In the special case, where no more than 3 high-speed links are used, the maximum aggregate link clock-rate is 156 MHz.
- Links configured for channelized T1/J1/E1 or unchannelized operation support the gapped-clock method for determining time-slots, which is backwards compatible with the FREEDM-8 and FREEDM-32 devices.
- For each channel, the HDLC receiver supports programmable flag-sequence detection, bit de-stuffing and frame-check sequence validation. The receiver supports the validation of both CRC-CCITT and CRC-32 frame-check sequences.
- For each channel, the HDLC transmitter supports programmable flag-sequence generation, bit stuffing and frame-check sequence generation. The transmitter supports the generation of both CRC-CCITT and CRC-32 frame-check sequences. The

BLOCK DIAGRAM



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transmitter also aborts packets under the direction of the host or automatically when the channel underflows.

- Provides 32 kbytes of on-chip memory for partial packet buffering in both the transmit and receive directions. You can configure this memory to support a variety of different channel configurations: from a single channel with 32 kbytes of buffering to 672 channels, each with a minimum of 48 bytes of buffering.
- Provides a standard five signal P1149.1 JTAG test-port for boundary scan board-test purposes.
- Supports 5 Volt tolerant I/Os for non-APPI signals. Supports a 3.3 Volt APPI signaling environment.
- 329-pin plastic ball grid-array (PBGA) package.

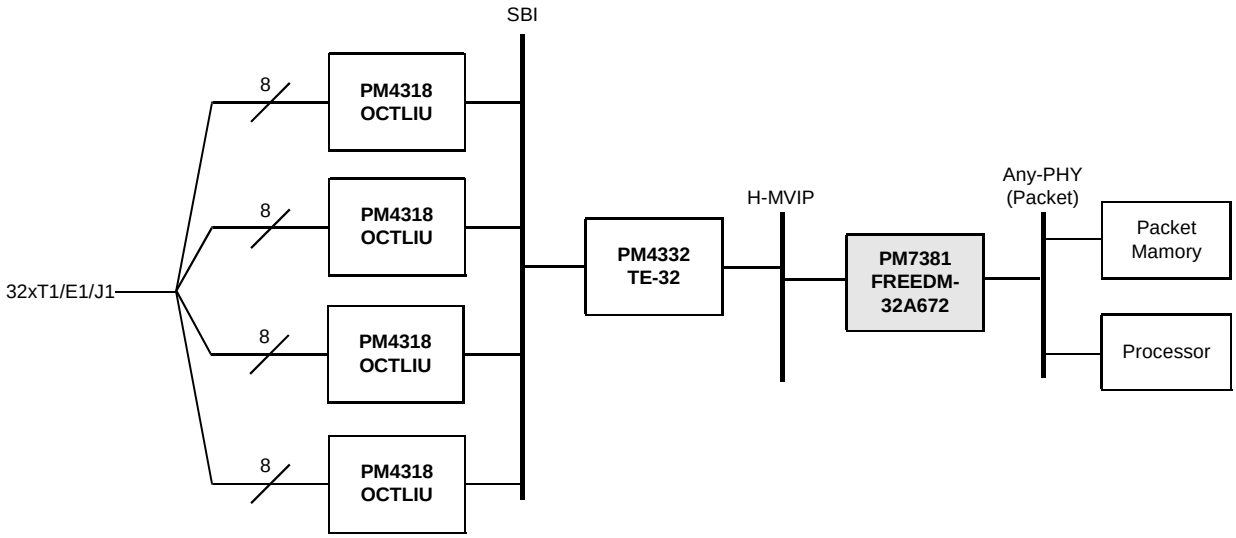
APPLICATIONS

Use the FREEDM-32A672 chip in the following applications:

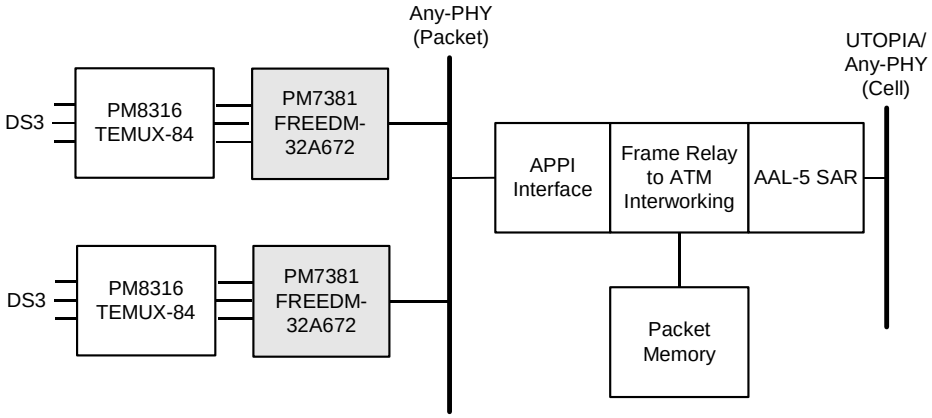
- Remote Access Concentrators.
- Frame Relay/Multiservice Switches.
- Multiservice Access Concentrators.
- Internet/Edge Routers.
- Packet Based DSLAM Equipment.

TYPICAL APPLICATIONS

EIGHT LINK T1/E1 PORT ADAPTER FOR PPP PROCESSING



N*DS3 FRAME RELAY TO ATM INTERWORKING



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