

AU9472 R2

Multimedia USB Keyboard Hub

Technical Reference Manual

Revision 2.1



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1.0 Introduction

1.1 Description

The AU9472 R2 is an integrated USB keyboard and 2 port hub controller chip. The AU9472 R2 has a built-in default keyboard matrix, so that it can be directly connected to an 18 x 8 keyboard matrix. The keyboard matrix can be customized via an optional external 1024-byte serial EEPROM. Downstream ports can be used to connect various USB peripheral devices, such as USB printers, modems, scanners, cameras, mice, and joysticks to the system without adding external glue logic. It also supports multimedia volume control, CD/DVD Play/Pause, Stop, Eject, Mute and general purpose shortcut keys such as Internet, email and help.

This single chip integration makes the AU9472 R2 the most cost effective hub/keyboard solution available in the market.

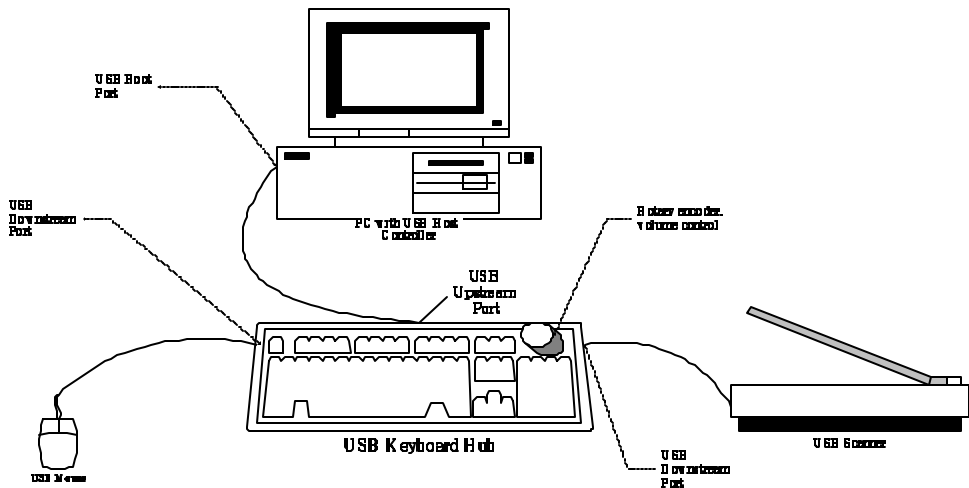
1.2 Features

- ?? Fully compliant with the Universal Serial Bus Specification, version 1.1
- ?? USB hub design is compliant with Universal Serial Bus Hub Specification, revision 1.1
- ?? USB keyboard design is compliant with USB Device Class Definition for Human Interface Devices (HID), Firmware Specification, version 1.1
- ?? Single chip integration of USB keyboard, hub, ACPI and multimedia control functions
- ?? Integrated USB hub supports two bus-powered downstream ports
- ?? Patent-pending, table-driven SCANTABLE? technology for easy customization to different keyboard matrix up to 18x8.
- ?? Support rotary encoder for multimedia volume control
- ?? Support CD/DVD Play/Pause, Fast Forward, Rewind, Stop, Eject, Mute (up to 24 keys)
- ?? Additional general purpose keys for internet, email, help...shortcuts, up to 16 keys.
- ?? Additional 2 general purpose LEDs
- ?? Support ACPI compliant suspend/shutdown key
- ?? If necessary, USB vendor ID, product ID, and keyboard scan code table can be customized via optional external EEPROM.
- ?? Built-in 3.3v voltage regulator allows single +5V operating voltage drawing directly from USB bus. This results in reduced overall system cost.
- ?? Optional gang-powered control pin for downstream port.
- ?? Runs at 12Mhz frequency
- ?? Available in 64-pin LQFP package.

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2.0 Application Block Diagram

The AU9472 R2 is a single chip which integrates USB keyboard and hub functionality. The upstream port is connected to the USB system. The downstream ports can be used for a mouse and joystick. The multimedia function keys are designed to support volume control, CD/DVD Play/Pause, Stop, Eject, Mute and general purpose shortcut keys for one key Internet, email and help.



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3.0 Pin Assignment

The AU9472 R2 is packed in a 64-pin Quad Flat Package (LQFP). The following figure shows the signal names for each of the pins on the chip of a LQFP package. The table on the following page describes each of the pin signals.

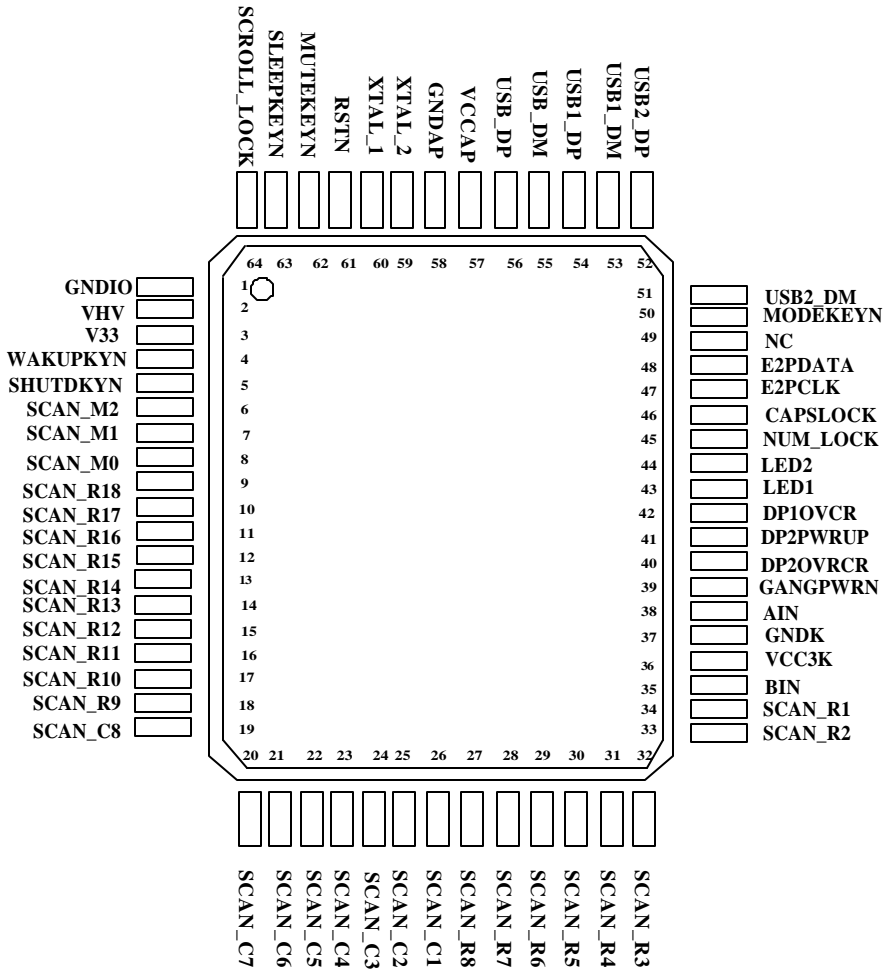


Fig 3.1 LQFP Package Diagram

Table 3-1. Pin Descriptions

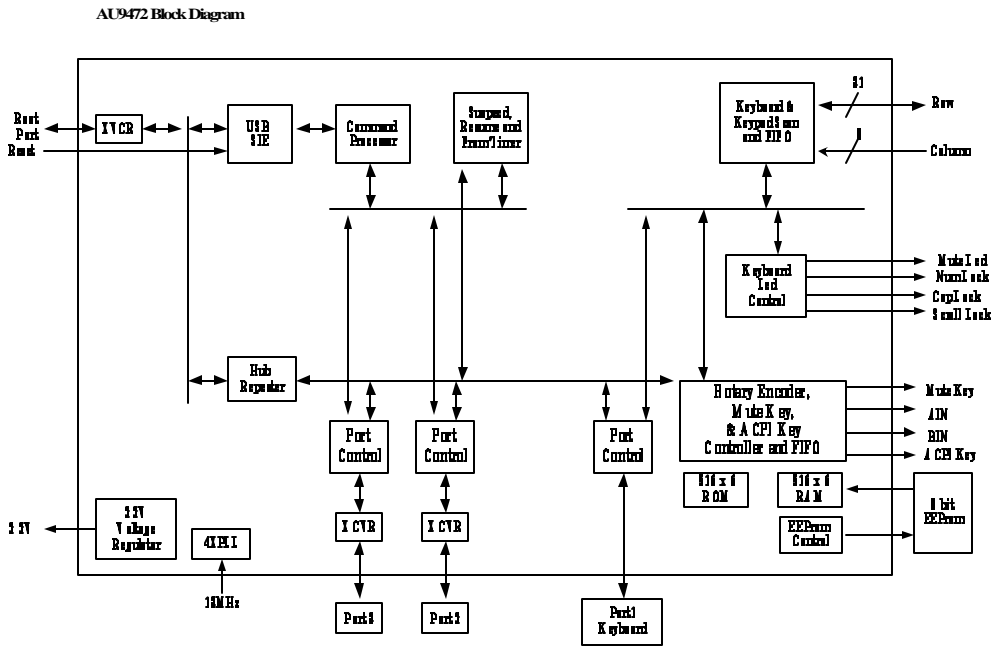
Pin #	Pin Name	IO Type	Driving Capability	Description
1	GNDIO	GND		Ground
2	VHV	5V Power Supply		5V input
3	VCC33	Regulator 3.3V Output		
4	WAKUPKYN	INPUT, PULL UP		ACPI wakeup key
5	SHUTDKYN	INPUT, PULL UP		ACPI shutdown key
6	SCAN_M2	INPUT,OUTPUT,PULL DOWN	16mA, 50KOhm	Row/Scan Line (dedicated for mm/shortcut keys)
7	SCAN_M1	INPUT/OUTPUT,PULL DOWN	16mA, 50KOhm	Row/Scan Line (dedicated for mm/shortcut keys)
8	SCAN_M0	INPUT/OUTPUT,PULL DOWN	16mA, 50KOhm	Row/Scan Line (dedicated for mm/shortcut keys)
9	SCAN_R18	INPUT/OUTPUT,PULL DOWN	16mA, 50KOhm	Row/Scan Line
10	SCAN_R17	INPUT/OUTPUT,PULL DOWN	16mA, 50KOhm	Row/Scan Line
11	SCAN_R16	INPUT/OUTPUT,PULL DOWN	16mA, 50KOhm	Row/Scan Line
12	SCAN_R15	INPUT/OUTPUT,PULL DOWN	16mA, 50KOhm	Row/Scan Line
13	SCAN_R14	INPUT/OUTPUT,PULL DOWN	16mA, 50KOhm	Row/Scan Line
14	SCAN_R13	INPUT/OUTPUT,PULL DOWN	16mA, 50KOhm	Row/Scan Line
15	SCAN_R12	INPUT/OUTPUT,PULL DOWN	16mA, 50KOhm	Row/Scan Line
16	SCAN_R11	INPUT/OUTPUT,PULL DOWN	16mA, 50KOhm	Row/Scan Line
17	SCAN_R10	INPUT,PULL UP,PULL DOWN	16mA, 50KOhm	Row/Scan Line
18	SCAN_R9	INPUT,PULL UP,PULL DOWN	16mA, 50KOhm	Row/Scan Line
19	SCAN_C8	INPUT,PULL UP	2.5K Ohm	Column line
20	SCAN_C7	INPUT,PULL UP	2.5K Ohm	Column line
21	SCAN_C6	INPUT,PULL UP	2.5K Ohm	Column line
22	SCAN_C5	INPUT,PULL UP	2.5K Ohm	Column line
23	SCAN_C4	INPUT,PULL UP	2.5K Ohm	Column line
24	SCAN_C3	INPUT,PULL UP	2.5K Ohm	Column line
25	SCAN_C2	INPUT,PULL UP	2.5K Ohm	Column line
26	SCAN_C1	INPUT,PULL UP	2.5K Ohm	Column line
27	SCAN_R8	INPUT/OUTPUT,PULL DOWN	16mA, 50KOhm	Row/Scan Line
28	SCAN_R7	INPUT/OUTPUT,PULL DOWN	16mA, 50KOhm	Row/Scan Line
29	SCAN_R6	INPUT/OUTPUT,PULL DOWN	16mA, 50KOhm	Row/Scan Line
30	SCAN_R5	INPUT/OUTPUT,PULL DOWN	16mA, 50KOhm	Row/Scan Line
31	SCAN_R4	INPUT/OUTPUT,PULL DOWN	16mA, 50KOhm	Row/Scan Line
32	SCAN_R3	INPUT/OUTPUT,PULL DOWN	16mA, 50KOhm	Row/Scan Line
33	SCAN_R2	INPUT/OUTPUT,PULL DOWN	16mA, 50KOhm	Row/Scan Line
34	SCAN_R1	INPUT/OUTPUT,PULL DOWN	16mA, 50KOhm	Row/Scan Line
35	BIN	INPUT		Rotary encoder input 'B'
36	VCC3K	Kernel 3.3V Input		+3V power supply
37	GNDK	Kernel Ground		Ground
38	AIN	INPUT		Rotary encoder input 'A'
39	GANGPWRN	OUTPUT	8mA	Port 1 power/Gang power enable (gang mode)

40	DP2OVRCUR	INPUT,PULL UP	50KOhm	Port 2 over current – low active
41	DP2PWRUP	OUTPUT	8mA	Downstream port 2 power enable – low active
42	DP1OVRCUR	INPUT,PULL UP	50KOhm	Port 1 over current – low active
43	LED1	OUTPUT	8mA	Additional LED 1 – low active – open drain
44	LED2	OUTPUT	8mA	Additional LED 2 – low active – open drain
45	NUM_LOCK	OUTPUT	16mA	Num lock LED – low active – open drain
46	CAPSLOCK	OUTPUT	16mA	Cap Lock LED – low active – open drain
47	E2PCLK	OUTPUT	4mA	EEPROM clock
48	E2PDATA	INPUT/OUTPUT,PULL UP	50KOhm	EEPROM data
49	NC			No Connection
50	MODEKEYN	INPUT		Fn Key
51	USB2_DM	INPUT/OUTPUT	16mA	USB downstream port 2 D-
52	USB2_DP	INPUT/OUTPUT	16mA	USB downstream port 2 D+
53	USB1_DM	INPUT/OUTPUT	16mA	USB downstream port 1 D-
54	USB1_DP	INPUT/OUTPUT	16mA	USB downstream port 1 D+
55	USB_DM	INPUT/OUTPUT	16mA	USB upstream D-
56	USB_DP	INPUT/OUTPUT	16mA	USB upstream D+
57	VCCAP	Analog 3.3V Input		Analog VCC
58	GNDAP	Analog Ground		Analog ground)
59	XTAL_2	OUTPUT		12MHz crystal output
60	XTAL_1	INPUT		12MHz Crystal input
61	RSTN	INPUT		Reset – low active
62	MUTEKEYN	INPUT,PULL UP	50KOhm	Mute key, low active
63	SLEEPKEYN	INPUT,PULL UP	50KOhm	ACPI (Sleep/wakeup/power down) – low active
64	SCROLL_LOCK	OUTPUT	16mA	Scroll_lock LED output – low active –open drain

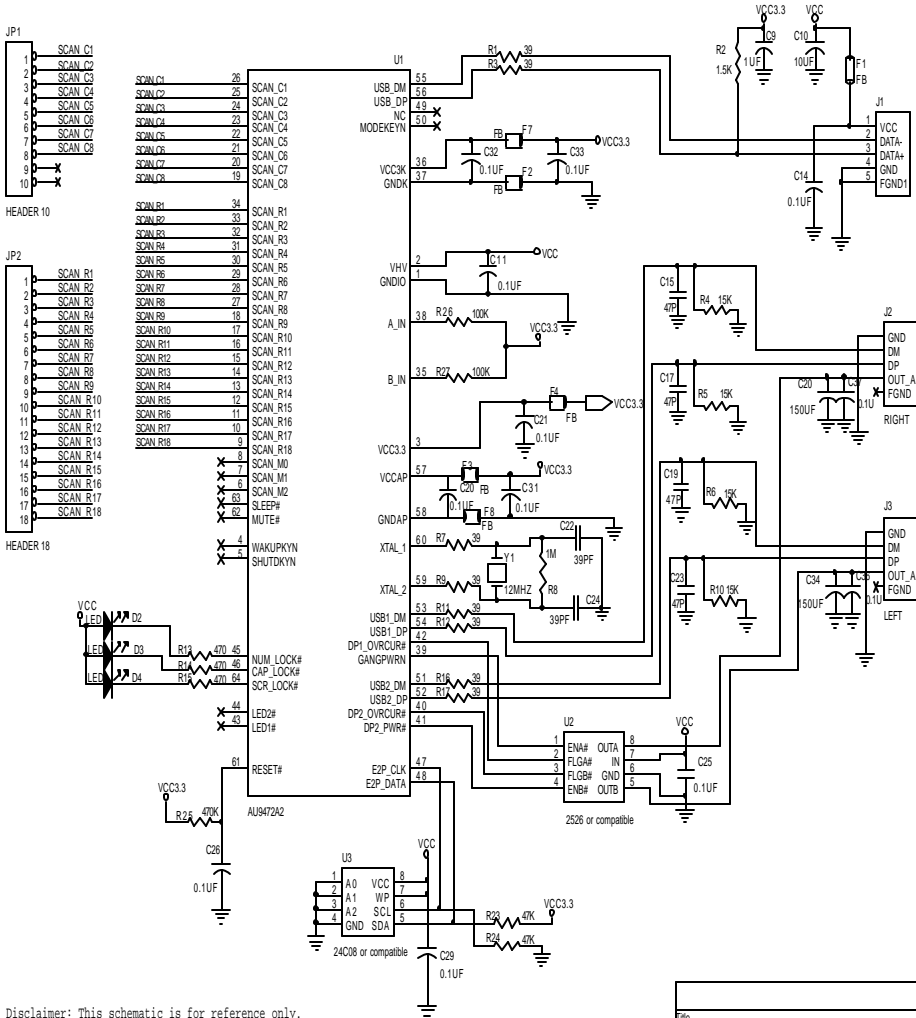
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4.0 System Architecture and Reference Design

4.1 AU9472 R2 Block Diagram



4.2 Sample Schematics



Disclaimer: This schematic is for reference only. Alcor Micro Corp. makes no warranty for the use of its products and bears no responsibility for any error that appear in this document. Specifications are subject to change without notice.

Title		
AU9472R2 USB KEYBOARD-HUB CONTROLLER		
Size	Document Number	Rev
A4	ALCOR MICRO AU9472R2	A
Date:	Friday, June 07, 2002	Sheet 1 of 1

4.3. AU9472 A2 Keyboard Hub EEPROM Sample Value

Offset	Hex value	Description
00	00,07	Configuration Byte 1 bit 0 : Individual power. Byte 1 bit 1 : Wakeup on any key. Byte 1 bit 2 : Select SelfPower change by HID feature. Byte 1 bit 3 : Enable disconnect on power change. Byte 1 bit 4 : Disable Hub(keyboard only). Byte 1 bit 5 : Enable Volume Up/Down Keys (Disable rotary encoder). Byte 1 bit 6 : Enable Split Report (16 bits-id3,8-id1) Byte 1 bit 7 : Enable Port Error
02	B1,C3	LoByte : Pointer to Hub device descriptor 000h ROM address HiByte : Xfer end address + 1
04	1C,35	LoByte : Pointer to Hub configuration descriptor 000h ROM address HiByte : Xfer end address + 1 (config+interface+endpoint)
06	C3,CC	LoByte : Pointer to HUB Class descriptor (0x29) 000h ROM address HiByte : Xfer end address + 1
08	CC,DE	LoByte : Pointer to Keyboard device descriptor 000h ROM address HiByte : Xfer end address + 1
0A	35,57	LoByte : Pointer to Keyboard configuration descriptor HiByte : Xfer end address + 1 000h ROM address (config+interface0+HID0+endpoint1+interface1+HID1+endpoint2)
0C	47,50	LoByte : Pointer to Keyboard HID descriptor (0x21) Interface 0 HiByte : Xfer end address + 1 000h ROM address
0E	70,B1	LoByte : Pointer to Keyboard Report descriptor (0x22) Interface 0 HiByte : Xfer end address + 1 000h ROM address
10	60,69	LoByte : Pointer to Keyboard HID descriptor (0x21) Interface 1 HiByte : Xfer end address + 1 000h ROM address
12	54,02	LoByte : Pointer to Keyboard Report descriptor (0x22) Interface 1 HiByte : Xfer end address + 1 start in 200h ROM address end in 300h ROM address

14	02,06	LoByte : Pointer to string descriptor (index 0) HiByte : Xfer end address + 1	300h ROM address
16	06,12	LoByte : Pointer to string descriptor (index 1) HiByte : Xfer end address + 1	300h ROM address
18	12,3A	LoByte : Pointer to string descriptor (index 2) HiByte : Xfer end address + 1	300h ROM address
1A	3A,42	LoByte : Pointer to string descriptor (index 3) HiByte : Xfer end address + 1	300h ROM address
1C	09,02,19,00,01,01,02,E0,32	Config Desc. 1 interface, self powered, remote wakeup, 100 mA Total bytes returned : 0x19	
25	09,04,00,00,01,09,00,00,02	Hub interface descriptor, interface 0. Class code 0x9, Sub Class 02	
2E	07,05,81,03,01,00,FF	Hub endpoint descriptor	
35	09,02,22,00,01,01,02,E0,32	Keybrd Config Desc. 1 interfaces, Self powered, remote wakeup, 100 mA Total bytes returned : 0x22	
3E	09,04,00,00,01,03,01,01,02	Keyboard interface descriptor, interface 0. Class code 0x3.Boot subclass	
47	09,21,10,01,00,01,22,41,00	Keyboard HID 1.1 descriptor , Country code=00	
50	07,05,81,03,08,00,0A	Keyboard endpoint descriptor	
57	09,04,01,00,01,03,00,00,02	Added Key interface descriptor, interface 1. Class code 0x3. subclass 02, (KB 1 interface, Added key Not Used)	
60	09,21,10,01,00,01,22,AE,00	Added Key HID 1.1 descriptor, Country code=00	
69	07,05,82,03,04,00,FF	Added Key endpoint descriptor	
70	05,01,09,06,A1,01,05,07, 19,E0,29,E7,15,00,25,01, 75,01,95,08,81,02,95,01, 75,08,81,01,95,05,75,01, 05,08,19,01,29,05,91,02, 95,01,75,03,91,01,95,06, 75,08,15,00,26,FF,00,05, 07,19,00,2A,FF,00,81,00, C0	Keyboard report descriptor	
B1	12,01,10,01,09,00,00,08, 8F,05,13,92,01,00,01,02, 00,01	Hub device descriptor, version 1. 1, change VID,PID Device version 1 12 Descriptor length 01 Device Descriptor 10 01 USB Version 1.1 09 Hub class 00 Sub-class 00 Device Protocol 08 Maximum packet size VV VV Vender ID – Hub Vender ID (058F) PP PP Product ID - Hub Product ID (9213) 01 00 Device release number 01 Index of Manufacturer string descriptor 02 Index of Product string descriptor 00 Index of serial number string descriptor – no serial number 01 Number of configuration	
C3	09,29,03,0C,00,16,64,02,FF	Hub class descriptor. 09 Descriptor length 29 Hub Descriptor	

4.4 Sample Key Matrix Layout Table

This table is a sample key matrix. The AU9472 R2 can also mask this matrix as default without an external EEPROM.

Table 4-1. Sample AU9472 R2 Key Matrix

	H1	H2	H3	H4	H5	H6	H7	H8
V1				⌘ Left				
V2	Alt-Left		Japan			Alt-Right	Japan	
V3		Ctrl-Left		Caps-Lock	Ctrl-Right	r	Korea-Right	
V4	Korea-Left		Shift-Right				Japan	Shift-Left
V5	Z	A	Back-Space	~	Enter	Home	⌘4	Tab
V6	X	S	+ =	1!	}]	⌘8	5	Q
V7	F3	F5	Print-Screen	Pause	F11	F9	F7	F1
V8	Esc	F4	F12	Scroll-Lock	F10	F8	F6	F2
V9	M	J	7&	6^	U	K	, <	Y
V10	N	H	8*	5%	I	L	. >	T
V11	B	G	9(4\$	O	::	?/	R
V12	V	F	0)	3#	P	”	Space-Bar	E
V13	C	D	- _	2@	[{	Pg Up 9	⌘6	W
V14	Page-Up	Page-DN	\(UK)	⌘	-	*	Pg Dn 3	Ins 0
V15	Home	End	\\	⌘	+	/	⌘2	. Del
V16	Insert	Del	⌘	⌘	⌘	Num Lock	End 1	Enter (Pad)
V17							⌘ Right	
V18	◇		Japan	Japan	Rev.Key	Brazil		

5.0 Electrical Characteristics

5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V _{CC}	Power Supply	-0.3 to 6.0	V
V _{IN}	Input Voltage	-0.3 to V _{CC} +0.3	V
V _{OUT}	Output Voltage	-0.3 to V _{CC} +0.3	V
V _{cc5}	Power Supply for Dual Oxide Cells	-0.6 to 6.0	V
V _{in5}	Power Supply for Dual Oxide Cells	-0.3 to V _{cc5} +0.3	V
V _{OUT}	Output Voltage	-0.3 to V _{cc5} +0.3	V
T _{STG}	Storage Temperature	-55 to 150	°C

5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V _{CC}	Power Supply	3.0	3.3	3.6	V
V _{IN}	Input Voltage	0	-	V _{CC}	V
V _{CC5}	Commercial Power Supply for Dual Oxide Cells	4.75	5.0	5.25	°C
	Industrial Power Supply for Dual Oxide Cells	4.5	5.0	5.5	V
V _{IN5}	Input Voltage	0	-	V _{cc5}	V
T _j	Commercial Junction Operating Temperature	0	25	115	°C
	Industrial Junction Operating Temperature	-40	25	125	°C

5.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input leakage current	no pull-up or pull-down	-1		1	?A
I_{OZ}	Tri-state leakage current		-1		1	?A
C_{IN3}	3.3V Input capacitance			2.8		?F
C_{OUT3}	3.3V Output capacitance		2.7		4.9	?F
C_{BID3}	3.3V Bi-directional buffer capacitance		2.7		4.9	?F
C_{IN5}	5V Input capacitance		2.7		5.6	?F
C_{OUT5}	5V Output capacitance					?F
C_{BID5}	5V Bi-directional buffer capacitance		2.7		5.6	?F

5.4 DC Electrical Characteristics for 5 volts operation

(Under Recommended Operating Conditions and $V_{CC}=4.5v \sim 5.25v$, $T_j=0^{\circ}C$ to $+115^{\circ}C$)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage	CMOS			$0.3 \cdot V_{CC}$	V
V_{IH}	Input High Voltage	CMOS	$0.7 \cdot V_{CC}$			V
V_{IL}	Input Low Voltage	TTL			0.8	V
V_{IH}	Input High Voltage	TTL	2.0			V
V_{t-}	Schmitt trigger negative going threshold voltage	CMOS		1.78		V
V_{t+}	Schmitt trigger positive going threshold voltage	CMOS		3.20		V
V_{t-}	Schmitt trigger negative going threshold voltage	TTL		1.10		V
V_{t+}	Schmitt trigger positive going threshold voltage	TTL		1.90		V
V_{OL}	Output low voltage	$I_{OL}=2, 4, 8, 12, 16, 24$ mA			0.4	V
V_{OH}	Output high voltage	$I_{OH}=2, 4, 8, 12, 16, 24$ mA	3.5			V
R_I	Input Pull-up/down resistance	$V_{IL}=0v$ or $V_{IH}=V_{CC}$		50		K?

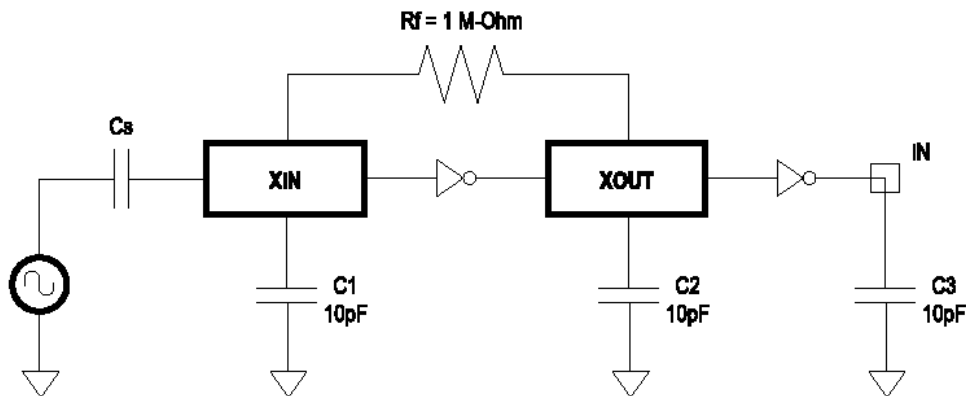
5.5 DC Electrical Characteristics for 3.3 volts operation

(Under Recommended Operating Conditions and $V_{CC}=3.0v \sim 3.6v$, $T_j = 0^{\circ}C$ to $+115^{\circ}C$)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage	CMOS			$0.3 * V_{CC}$	V
V_{IH}	Input High Voltage	CMOS	$0.7 * V_{CC}$			V
V_{t-}	Schmitt trigger negative going threshold voltage	CMOS		1.20		V
V_{t+}	Schmitt trigger positive going threshold voltage	CMOS		2.10		V
V_{OL}	Output low voltage	$I_{OH}=2, 4, 8, 12, 16, 24$ mA			0.4	V
V_{OH}	Output high voltage	$I_{OH}=2, 4, 8, 12, 16, 24$ mA	2.4			V
R_I	Input Pull-up/down resistance	$V_{IL}=0v$ or $V_{IH}=V_{CC}$		75		K?

5.6 Crystal Oscillator Circuit Setup for Characterization

The following setup was used to measure the open loop voltage gain for crystal oscillator circuits. The feedback resistor serves to bias the circuit at its quiescent operating point and the AC coupling capacitor, C_s , is much larger than $C1$ and $C2$.



5.7 USB Transceiver Characteristics

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V _{CC}	DC supply voltage		3.0	3.6	V
V _I	DC input voltage range		0	5.5	V
V _{I/O}	DC input range for I/Os		0	V _{CC}	V
V _O	DC output voltage range		0	V _{CC}	V
T _{AMB}	Operating ambient temperature range in free air	See DC and AC characteristics for individual device	0	70	°C

ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

In accordance with the Absolute Maximum Rating System, Voltages are referenced to GND (Ground=0v)

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V _{CC}	DC supply voltage		-0.5	+6.5	V
I _k	DC input diode current	V _i <0		-50	mA
V _I	DC input voltage	Note 3	-0.5	+5.5	V
V _{I/O}	DC input voltage range for I/Os		-0.5	V _{CC} +0.5	V
I _{OK}	DC output diode current	V _O > V _{CC} or V _O <0		+/-50	mA
V _O	DC output voltage	Note 3	-0.5	V _{CC} +0.5	V
I _b	DC output source sink current for VP/VM and RCV pins	V _O =0 to V _{CC}		+/-15	mA
I _b	DC output source or sink current for D+/D- pins	V _O = 0 to V _{CC}		+/-50	mA
I _{CC} , I _{GND}	DC V _{CC} or GND current			+/-100	mA
T _{STG}	Storage temperature range		-60	+150	°C
P _{TOT}	Power dissipation per package				mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The performance capability of a high performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (Ground=0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			-40 C to +85 C			
			MIN	TYP	MAX	
VHYS	Hysteresis on inputs	Vcc=3.0V to 3.6V (Note 3)	0.3	0.4	0.5	V
VIH	HIGH level input	Vcc=3.0V to 3.6V (Note 3)		1.5	2.0	V
VIL	LOW level input	Vcc=3.0V to 3.6V (Note 3)	0.8	1.1		V
RoH	Output impedance (HIGH state)	Note 2	28	34	43	ohm
RoL	Output impedance (LOW state)	Note 2	28	35	43	ohm
VOH	HIGH level output (Note 3)	Vcc=3.0V Io=6mA Vcc=3.0V Io=4mA Vcc=3.0V Io=100?A	2.2 2.4 2.8	2.7		V
VOL	LOW level output (Note 3)	Vcc=3.0V Io=6mA Vcc=3.0V Io=4mA Vcc=3.0V Io=100?A		0.3	0.7 0.4 0.2	V
IQ	Quiescent supply current	Vcc=3.6V VI=Vcc or GND Io=0		330	600	?A
Isup	Supply current in suspend	Vcc=3.6V VI=Vcc or GND Io=0			70	?A
IFS	Active supply current (Full Speed)	Vcc=3.3V		9	14	mA
ILS	Active supply current (Low Speed)	Vcc=3.3V		2		mA
ILeak	Input leakage current	Vcc=3.6V VI=5.5V or GND, not for I/O Pins		+/- 0.1	+/- 0.5	?A
IOFF	3-state output OFF-state current	Vi=Vih or Vil; Vo=Vcc or GND			+/-10	?A

NOTES:

1. All typical values are at Vcc=3.3V and Tamb=25°C.
2. This value includes an external resistor of 24 ohm +/-1%. See "Load D+ and D-" diagram for testing details.
3. All signals except D+ and D-.

AC ELECTRICAL CHARACTERISTICS

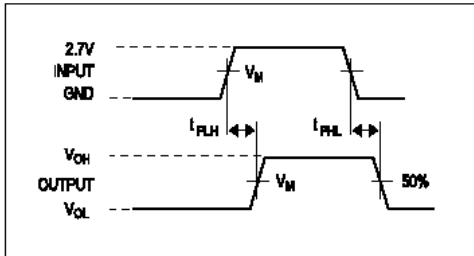
GND=0V, $t_r = t_f = 3.0$ ns; $C_L = 50$ pF, $R_L = 500$ ohms

SYMBOL	PARAMETER	WAVEFORM	LIMITS (T_{AMB})					UNIT
			0°C to +25°C			0°C to +70°C		
			MIN	TYP	MAX	MIN	MAX	
tpLH tpHL	VMO/VPO to D+/D- Full Speed	1	0 0		12 12	0 0	14 14	ns
trise tfall	Rise and Fall Times Full Speed	2	4 4	9 9	20 20	4 4	20 20	ns
tRFM	Rise and Fall Time Matching Full Speed		90		110	90	110	%
tpLH tpHL	VMO/VPO to D+/D- Low Speed	1		120 120	300 300		300 300	ns
trise tfall	Rise and Fall Times Low Speed	2	75 75		300 200	75 75	300 200	ns
tRFM	Rise and Fall Time Matching Low Speed		70		130	70	130	%
tpLH tpHL	D+/D- to RCV	3		9 9	16 16		16 16	ns
tpLH tpHL	D+/D- to VP/VM	1		4 4	8 8		8 8	ns
tpHZ tpZH tpLZ tpZL	OE# to D+/D- $R_L =$ 500ohm	4			12 12 10 10		12 12 10 10	ns
tsu	Setup for SPEED	5	0					ns
Vcr	Crossover point ¹	3	1.3		2.0	1.3	2.0	V

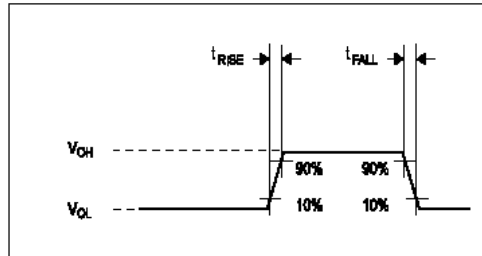
NOTE:

1. The crossover point is in the range of 1.3V to 2.5V for the low speed mode with a 5Cpf capacitance.

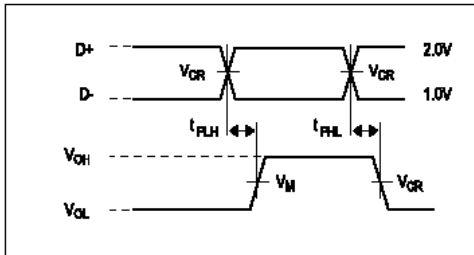
AC WAVEFORM 1.
D+/D- TO VP/VM OR VPO/VM TO D+/D-



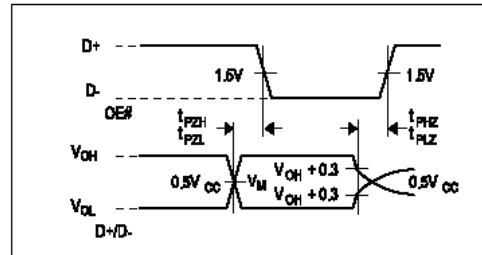
AC WAVEFORM 2.
RISE AND FALL TIMES



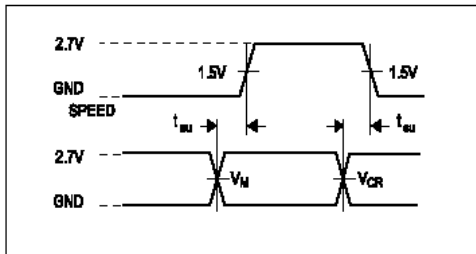
AC WAVEFORM 3.
D+/D- TO RCV



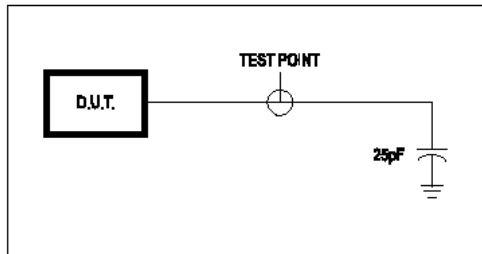
AC WAVEFORM 4.
OE# TO D+/D-



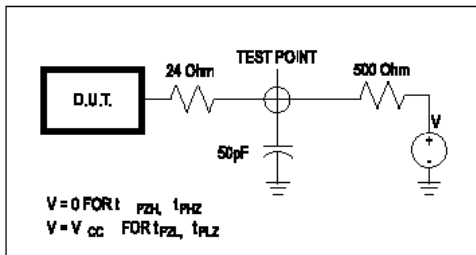
AC WAVEFORM 5.
SETUP FOR SPEED



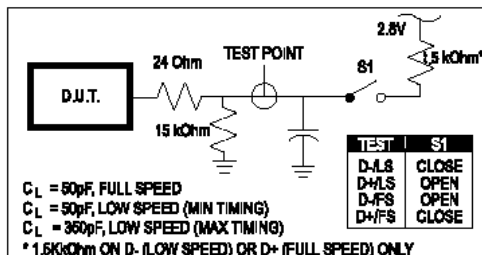
TEST CIRCUIT 1.
LOAD FOR VM/VP AND RCV



TEST CIRCUIT 2.
LOAD FOR ENABLE AND DISABLE TIMES



TEST CIRCUIT 3.
LOAD FOR D+/D-



5.8 ESD Test Results

Test Description : ESD Testing was performed on a Zapmaster system using the Human-Body –Model (HBM) and Machine-Model (MM), according to MIL_STD 883 and EIAJ IC_121 respectively.

✂✂ Human-Body-Model stress devices by sudden application of a high voltage supplied by a 100 PF capacitor through 1.5 Kohm resistance.

✂✂ Machine-Model stresses devices by sudden application of a high voltage supplied by a 200 PF capacitor through very low (0 ohm) resistance

Test circuit & condition

✂✂ Zap Interval : 1 second

✂✂ Number of Zaps : 3 positive and 3 negative at room temperature

✂✂ Criteria : I-V Curve Tracing

Model	Model	S/S	TARGET	Results
HBM	Vdd, Vss, I/C	15	6000V	Pass
MM	Vdd, Vss, I/C	15	200V	Pass

5.9 Latch-Up Test Results

Test Description: Latch-Up testing was performed at room ambient using an IMCS-4600 system which applies a stepped voltage to one pin per device with all other pins open except Vdd and Vss which were biased to 5 Volts and ground respectively.

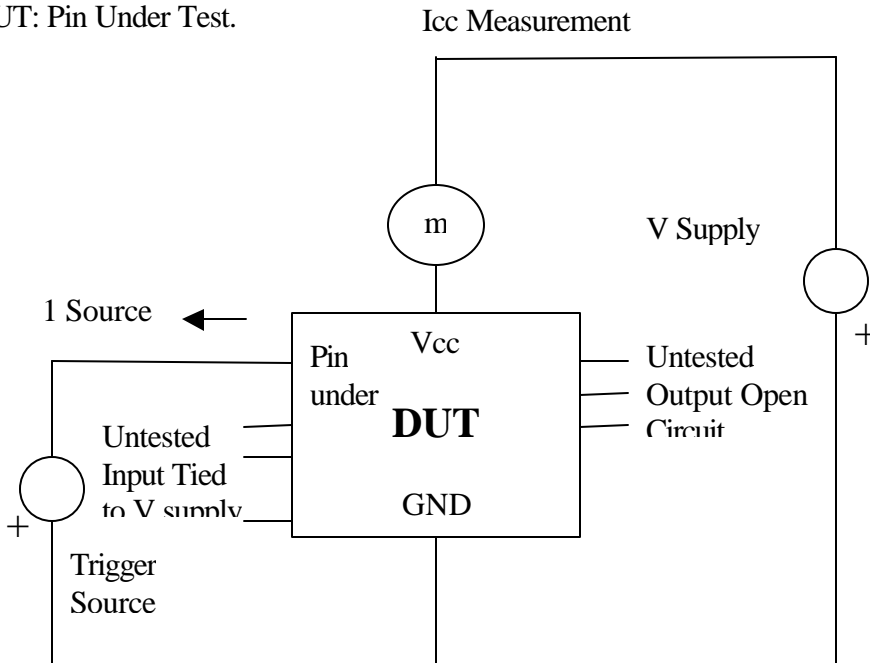
Testing was started at 5.0 V (Positive) or 0 V(Negative), and the DUT was biased for 0.5 seconds.

If neither the PUT current supply nor the device current supply reached the predefined limit (DUT=0 mA , Icc=100 mA), then the voltage was increased by 0.1 Volts and the pin was tested again.

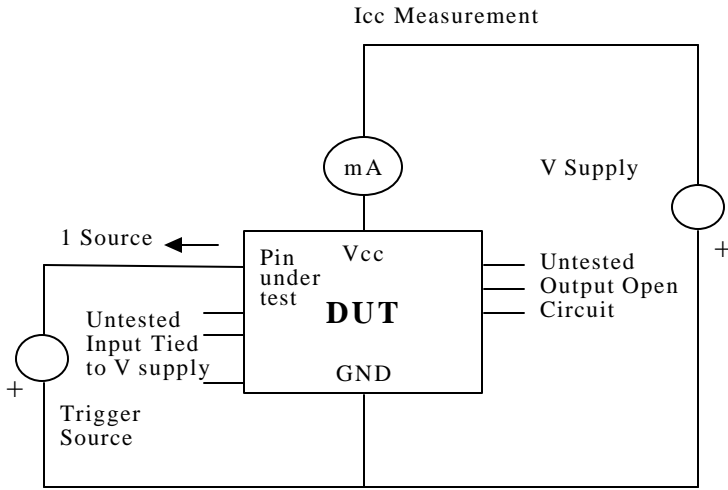
This procedure was recommended by the JEDEC JC-40.2 CMOS Logic standardization committee.

Notes:

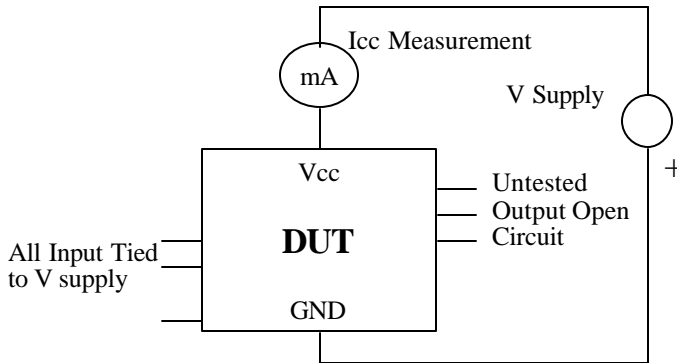
1. DUT: Device Under Test.
2. PUT: Pin Under Test.



Test Circuit : Positive Input/ output Overvoltage /Overcurrent



Test Circuit : Negative Input/ Output Overvoltage /Overcurrent



Supply Voltage test

Latch-Up Data

Model	Model	Voltage (v)/ Current	S/S	Results
Voltage	+	11.0	5	Pass
	-	11.0		
Current	+	200	5	
	-	200		
Vdd-Vxx		9.0	5	Pass

6.0 Mechanical Information

