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SIEMENS AKTIENGESELLSCHAF

T-77-07-11

Horizontal PLL for Picture-in-Picture

Preliminary Data

SDA 9086-3

MOS IC

Features

- Used in Picture-in-Picture systems (PIP)
- Field repetition frequency: 50 Hz or 100 Hz
- Clock output: 13.5 MHz or 27 MHz
- Pin compatible to SDA 9086-2
- Trigger circuit at the horizontal input

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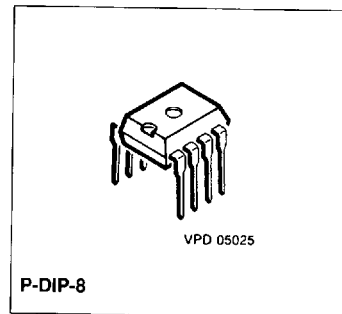
P-DIP-8

Type	Ordering Code	Package
SDA 9086-3	Q67100-H5045	P-DIP-8

The integrated circuit SDA 9086-3 generates a system clock signal from the line sync signal SC. The clock signal is fed to the output CLX as well as to the output HSP as a sync horizontal signal. Using the programming pin NC, the PLL can be adjusted from the 50 Hz- or 100 Hz-field frequency.

The input SC processes the TTL or the SSC (Super Sandcastle) input level, as selected by the programming pin VB.

The SDA 9086-3 is designed to be used in Picture-in-Picture systems (SDA 9087/88-2), however, it can be used as an individual clock generator.

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Circuit Description

The Functions of the PLL

The PLL of the SDA 9086-3 consists of a horizontal timer, a phase comparator with output current sources and a VCO. It generates a line locked system clock of 13.5 MHz or 27 MHz (depending on the field repetition rate).

In the horizontal timer the internal 13.5 MHz-clock from the VCO is divided by 864 or 432 (same factor for PAL and NTSC). The divided clock signal is fed to the HSP output as well as to the phase comparator.

The reference signal for the phase comparator is the external SC signal.

Because the PLL's phase comparator tries to match the rising edge of the two input signals, the HSP output signal is line-locked to the SC input signal. The HSP signal is available to the output pin with minimal time delay. The digital phase comparator is frequency- and phase-sensitive. The output signals are current pulses used as an "up/down" information. The external loop filter connected to the RC pin is used in order to integrate and filter these current pulses. The resulting analog signal is used as a control voltage for the VCO.

The input signal SC is fed to a timing controlled horizontal trigger circuit. This circuit prevents the repeated triggering of the phase comparator, if the signal edges are smooth and noisy.

Description of the Programming Inputs

Using the static programming pins VB and NC it is possible to select different operating modes of the SDA 9086-3 .

NC	VB	Output Frequency at CLX	Input Freq. at SC, Outp. Freq. at HSP	Input Level at SC
Ground or open	Ground or open	13.5 MHz	15.625 kHz	SSC
Ground or open	V_{DD}	13.5 MHz	15.625 kHz	TTL
V_{DD}	Ground or open	27 MHz	31.25 kHz	SSC
V_{DD}	V_{DD}	27 MHz	31.25 kHz	TTL

Pin Configuration
(top view)

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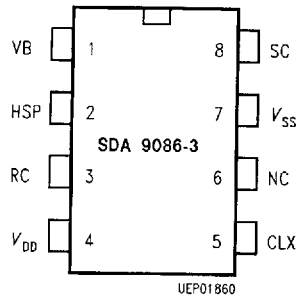
Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
1	VB	I	Programming input for the selection of the input signal at the SC pin. (TTL or SSC signal level)
2	HSP	O	Output for the horizontal sync pulse. The frequency is the same as for the SC input signal if the selection of the programming pin NC is correct.
3	RC	I/O	Selection RC loop filter pin for integration and filtering of the Up/Down current pulses of the PLL.
4	V_{DD}		Positive supply voltage
5	CLX	O	System clock output (13.5 MHz or 27 MHz)
6	NC	I	Programming input for setting the device to the used line frequency (15.625 kHz bzw. 31.25 kHz)
7	V_{SS}		Ground
8	SC	I	Horizontal sync frequency input (15.625 kHz or 31.25 kHz) TTL level are allowed.

Block Diagram

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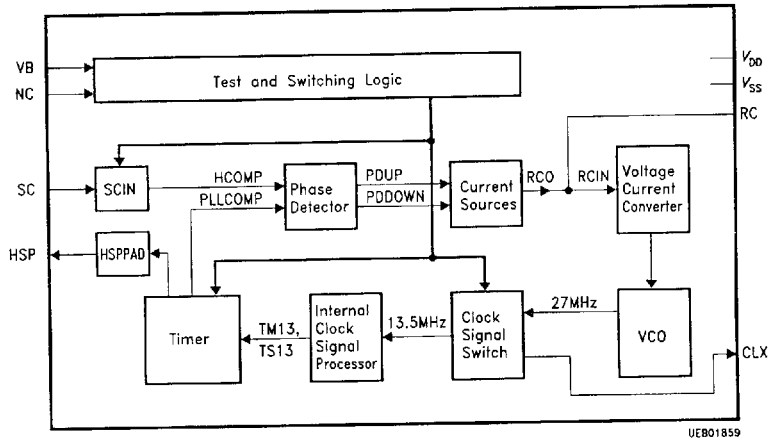
Absolute Maximum Ratings

$T_A = 0$ to $70\ ^\circ C$

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply voltage	V_{DD}	-0.3		6	V
Input voltage	V_I	-0.3		6	V
Ambient temperature	T_A	0		70	$^\circ C$
Storage temperature	T_{stg}	-55		125	$^\circ C$
Thermal resistance	R_{thSA}			105	K/W
Max. power dissipation	P_{tot}			0.2	W

Operating Range

Supply voltage	V_{DD}	4.5	5	5.5	V
Supply current	I_{DD}		20	40	mA
Ambient temperature	T_A	0		70	$^\circ C$

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Characteristics

$T_A = 25\ °C$ (all voltages relative to V_{SS})

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

Input SC, if VB = "Ground" or "Open" (Sandcastle pulse as input signal)

Low level	V_{IL}	0		$0.5\ V_{DD}$		
High level	V_{IH}	$0.65\ V_{DD}$		V_{DD}		
Switching threshold for detection of burst key			$0.6\ V_{DD}$			
Pulse width	T_{SCS}	0.1			μs	
Pulse ratio	T_{SCS}/T			0.5		

Input SC, if VB = V_{DD} (TTL level operation mode)

Low level	V_{IL}	0		0.8	V	
High level	V_{IH}	2.0		V_{DD}	V	
L-input current	I_{IL}	−50	−170	−300	μA	if $V_{IL} = 0V$
H-input current	I_{IH}	−50	−140	−300	μA	if $V_{IH} = 2V$
Pulse width	T_{SCT}	0.1			μs	
Pulse ratio	T_{SCT}/T			0.5		

Input VB, NC (Programming inputs)

Low level	V_{IL}	0		1	V	
High level	V_{IH}	3.5		V_{DD}	V	
Input current	I_{IL}	0	20	50	μA	V_{IL}
Input current	I_{IH}	10	30	100	μA	V_{IH}

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Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

Output CLX, if NC = V_{DD}

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
Period	T_{CL27}	35		40	ns	
Rise time	t_{TLH}			5	ns	TTL level
Fall time	t_{THL}			5	ns	TTL level
Low time	t_{WL}	12			ns	$V_{QL} = 0.4$ V
High time	t_{WH}	12			ns	$V_{QH} = 2.4$ V
Load capacity	C_L			20	pF	
H-output level	V_{QH}	2.4	3	V_{DD}	V	$I_{QH} = -8$ mA
L-output level	V_{QL}	0	0.15	0.4	V	$I_{QL} = 8$ mA

Output CLX, if NC = "Ground" or "open"

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
Period	$T_{CL13.5}$	70		80	ns	
Low time	t_{WL}	27			ns	$V_{QL} = 0.4$ V
High time	t_{WH}	27			ns	$V_{QH} = 2.4$ V

Output HSP

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
H-output level	V_{QH}	2.4	3	V_{DD}	V	$I_{QH} = -5$ mA
L-output level	V_{QL}	0	0.15	0.4	V	$I_{QL} = 5$ mA
Output hold time	t_{QH}	3			ns	
Output delay time	t_{QD}			20	ns	
Load capacity	C_L			20	pF	
Analog delay time referring to SC	t_{AD}		20		ns	

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Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

PLL

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
Down pulse current	I_{QD}	100	150	200	μA	$V_{RC} = 2V$
Up pulse current	I_{QU}	−100	−150	− 200	μA	$V_{RC} = 2V$
VCO frequency	f_{VCO}	151 >25		50	MHz MHz	$V_{RC} = 1V$ $V_{DD} = 4.5$ V $T_A = 3.5$ V
				> 30	MHz	$V_{RC} = 3.5V$ $V_{DD} = 5.5$ V $T_A = 70$ °C

Filter Element

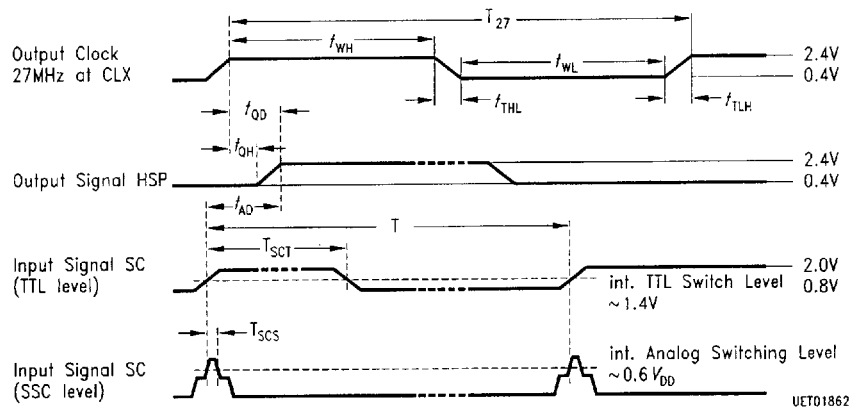| Application	C_1/pF	C_2/nF	C_3/pF	C_4/nF	$R/k\Omega$
I	180	180	–	–	25
II	80	80	100	100	30
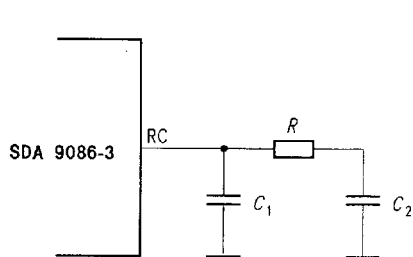
I: Standard application
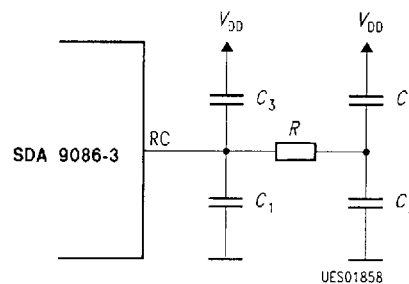
II: Recommended application
if the interferences occur on V_{DD}

Timing Diagram 1

Timing of SDA 9086-3

Output Clock 27MHz at CLX

Output Signal HSP

Input Signal SC (TTL level)

Input Signal SC (SSC level)

T_{27}

t_{WH}

t_{WL}

t_{THL}

t_{TLH}

t_{QD}

t_{QH}

t_{AD}

T_{SCT}

T

T_{SCS}

2.4V
0.4V

2.4V
0.4V

int. TTL Switch Level ~1.4V   2.0V 0.8V

int. Analog Switching Level ~0.6 V_{DD}

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Timing Diagram 2

HSP Pulse Width

Output Clock 27 MHz at CLX

Output Signal HSP

$20 \times T_{27}$

Output Clock 13.5 MHz at CLX

Output Signal HSP

$10 \times T_{13.5}$

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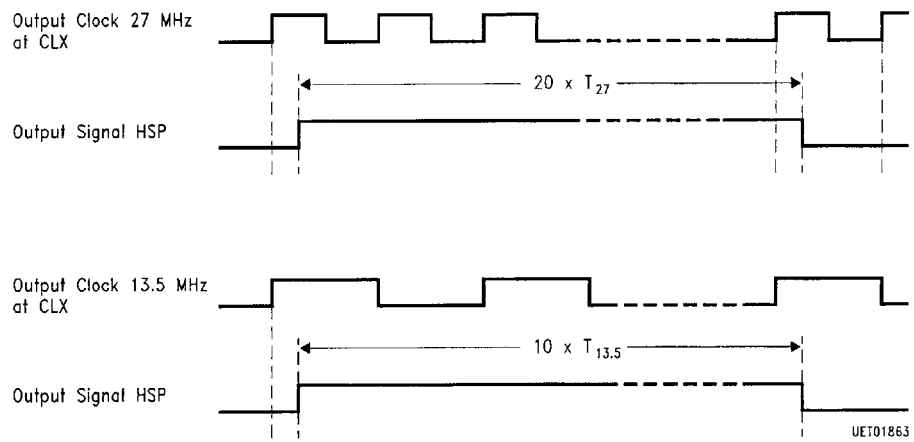
Application Circuit

Siemens Picture-in-Picture System