

TOPAZ

SEMICONDUCTOR

T-43-25
SD5200

N-CANNEL ENHANCEMENT-MODE QUAD D-MOS FET DRIVER ARRAY

ORDERING INFORMATION

Sorted Chips in Waffle Pack	SD5200CHP
16-Pin Plastic Dual In-Line Package	SD5200N
Description	30V, 80 ohm

FEATURES

- Normally OFF configuration
- Low Interelectrode capacitance
- High-speed switching

APPLICATIONS

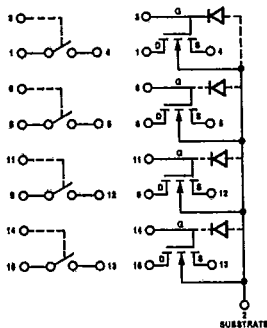
- +30V Analog Switch Drivers
- Wide-Band Dual Differential Amplifiers

ABSOLUTE MAXIMUM RATINGS (per channel, T_A = +25°C unless otherwise noted)

V _{DS} Drain-Source Voltage	+30Vdc
V _{SD} Source-Drain Voltage	+0.5Vdc
V _{DB} Drain-Body Voltage	+30Vdc
V _{SB} Source-Body Voltage	+15Vdc
V _{GS} Gate-Source Voltage	+25Vdc
V _{GB} Gate-Body Voltage	+25Vdc
Gate-Body Voltage	-0.3Vdc
V _{GD} Gate-Drain Voltage	+25Vdc
I _D Continuous Drain Current	50mA

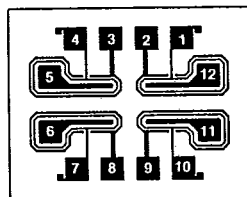
P _D Total Package Power Dissipation (at or below T _A = +25°C)	640mW
Linear Derating Factor	10.7mW/°C
P _D Single Device Power Dissipation (at or below T _A = +25°C)	300mW
Linear Derating Factor	5.0mW/°C
T _J Operating Junction Temperature Range	-55 to +85°C
T _S Storage Temperature Range	-55 to +150°C

SCHEMATIC DIAGRAM



Note: Pin numbers correspond to Package Pin-out

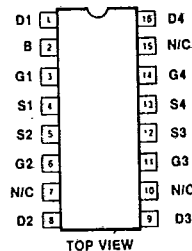
CHIP CONFIGURATION



PAD NO.	PAD FUNCTION	PAD NO.	PAD FUNCTION
1	Gate No. 1	7	Gate No. 3
2	Source No. 1	8	Source No. 3
3	Source No. 2	9	Source No. 4
4	Gate No. 2	10	Gate No. 4
5	Drain No. 2	11	Drain No. 4
6	Drain No. 3	12	Drain No. 1

Dimensions: .041 x .033 x .013 inches

PIN CONFIGURATION



DIMENSIONS
16-Pin Plastic DIP
See Package 10

TOPAZ
 SEMICONDUCTOR

 T-43-25-
SD5200
ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

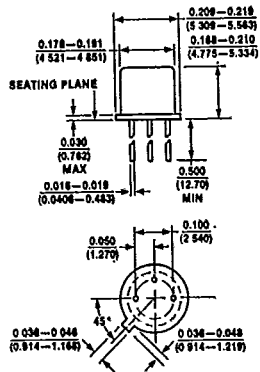
#	CHARACTERISTIC	SD5200			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
1	BV_{DS} Drain-Source Breakdown Voltage	30	35		V	$I_D = 10\mu\text{A}, V_{GS} = V_{BS} = 0$
2	BV_{SB} Source-Substrate Breakdown Voltage	15			V	$I_S = 10\mu\text{A}, V_{GB} = 0$ Drain Open
3	I_{GBS} Gate-Body Leakage Current			1.0	μA	$V_{GB} = 25\text{V}, V_{DB} = V_{SB} = 0$
4	$V_{GS(th)}$ Gate-Source Threshold Voltage	0.5	1.0	2.0	V	$V_{DS} = V_{GS}, I_D = 1.0\mu\text{A}$ $V_{SB} = 0$
5	$r_{DS(on)}$ Drain-Source ON Resistance		50	80	ohms	$V_{GS} = 5\text{V}$
6			30		ohms	$V_{GS} = 10\text{V}$
7			23		ohms	$V_{GS} = 15\text{V}$
8			19		ohms	$V_{GS} = 20\text{V}$
						$I_D = 1\text{mA}$ $V_{SB} = 0$
9	g_{fs} Common-Source Forward Transconductance	10	12		mmhos	$V_{DS} = 10\text{V}, I_D = 20\text{mA}$ $f = 1\text{KHz}, V_{SB} = 0$
10	$C_{(gs + gd + gb)}$ Gate Node Capacitance		2.4	3.5	pF	$f = 1\text{MHz}$ $V_{DS} = 10\text{V}$ $V_{GS} = V_{BS} = -15\text{V}$
11	$C_{(gd + db)}$ Drain Node Capacitance		1.3	1.5	pF	
12	$C_{(gs + sb)}$ Source Node Capacitance		3.5	4.0	pF	
13	$C_{(dg)}$ Reverse Transfer Capacitance		0.3	0.5	pF	
14	C_T Cross Talk		-107		dB	

TOPAZ SEMICONDUCTOR

PACKAGE DATA

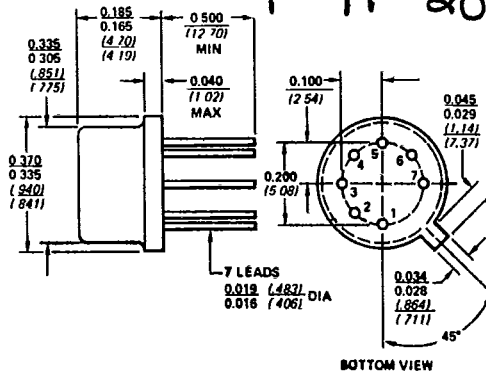
T-90-20 -
T-91-20

Package 1 (TO-18) TO-206AA



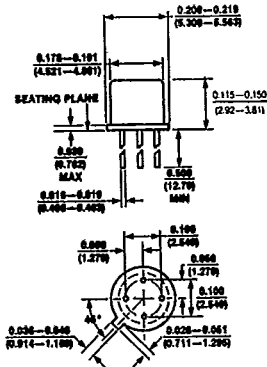
All Dimensions in Inches and (millimeters)

Package 4 (TO-78)



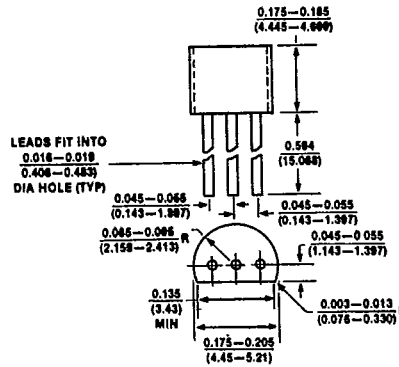
All Dimensions in Inches and (millimeters)

Package 2 (TO-52) 4-Lead



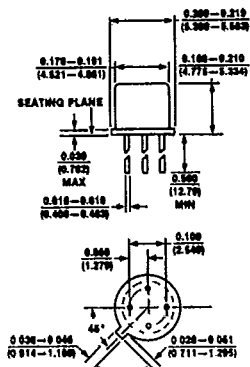
All Dimensions in Inches and (millimeters)

Package 5 (TO-92) TO-226AA



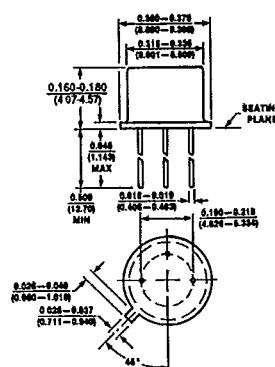
All Dimensions in Inches and (millimeters)

Package 3 (TO-72) TO-206AF



All Dimensions in Inches and (millimeters)

Package 6 (TO-39) TO-205AF

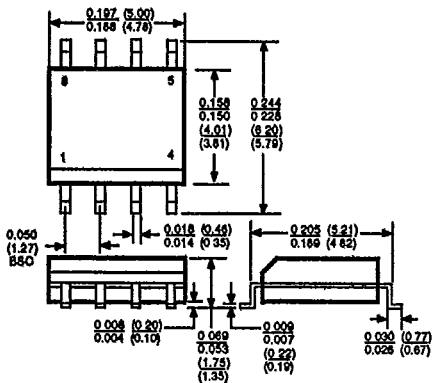


All Dimensions in Inches and (millimeters)

TOPAZ
SEMICONDUCTOR

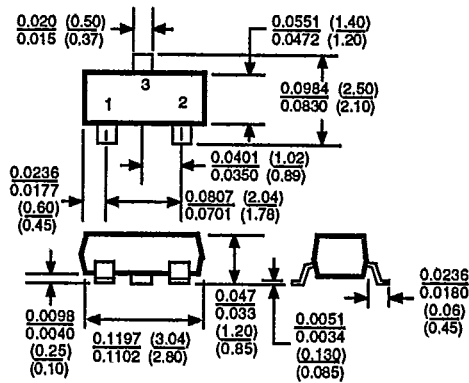
T-90-20 -
PACKAGE DATA
T-91-20 -

Package 19 (SO-8)



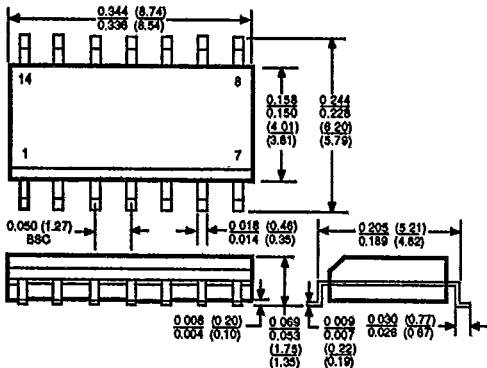
All Dimensions in Inches and (millimeters)

Package 22 (SOT-23) TO-236AA



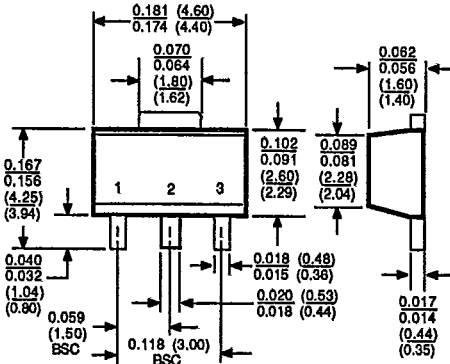
All Dimensions in Inches and (millimeters)

Package 20 (SO-14)



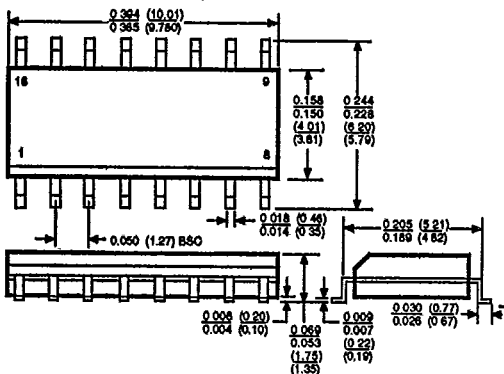
All Dimensions in Inches and (millimeters)

Package 23 (SOT-89) TO-243AA



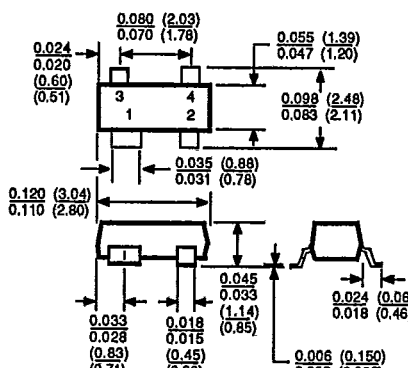
All Dimensions in Inches and (millimeters)

Package 21 (SO-16)



All Dimensions in Inches and (millimeters)

Package 24 (SOT-143)



All Dimensions in Inches and (millimeters)