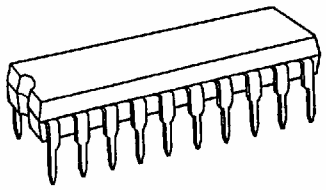
(10-Bit Serial I/O A/D Converter)

1. GENERAL DESCRIPTION

The TC35080P is a high precision, high speed monolithic CMOS 10-bit Successive Approximation A/D Converter with separate serial input and output.

This device has a clock input (IOCK) which shifts serial data in (write mode) and out (read mode), a data output enable (DOE) which controls output timing and a Successive Approximation Register Status (SARS) output. These permit easy interfacing to other devices.

The frequency of the built in A/D conversion clock is determined by the values of an external RC Network connected to the CKI and CKO terminals. For the user desires, an external clock may be connected to the CKI terminal.



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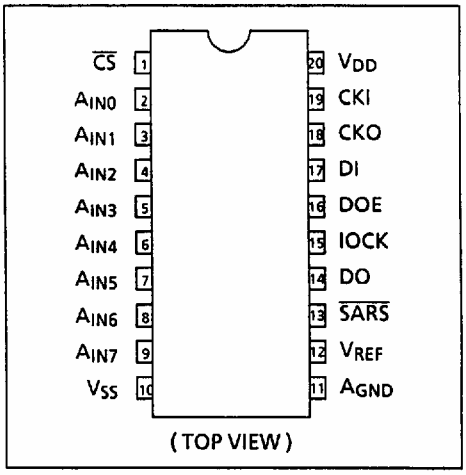


(TOP VIEW)

2. FEATURES

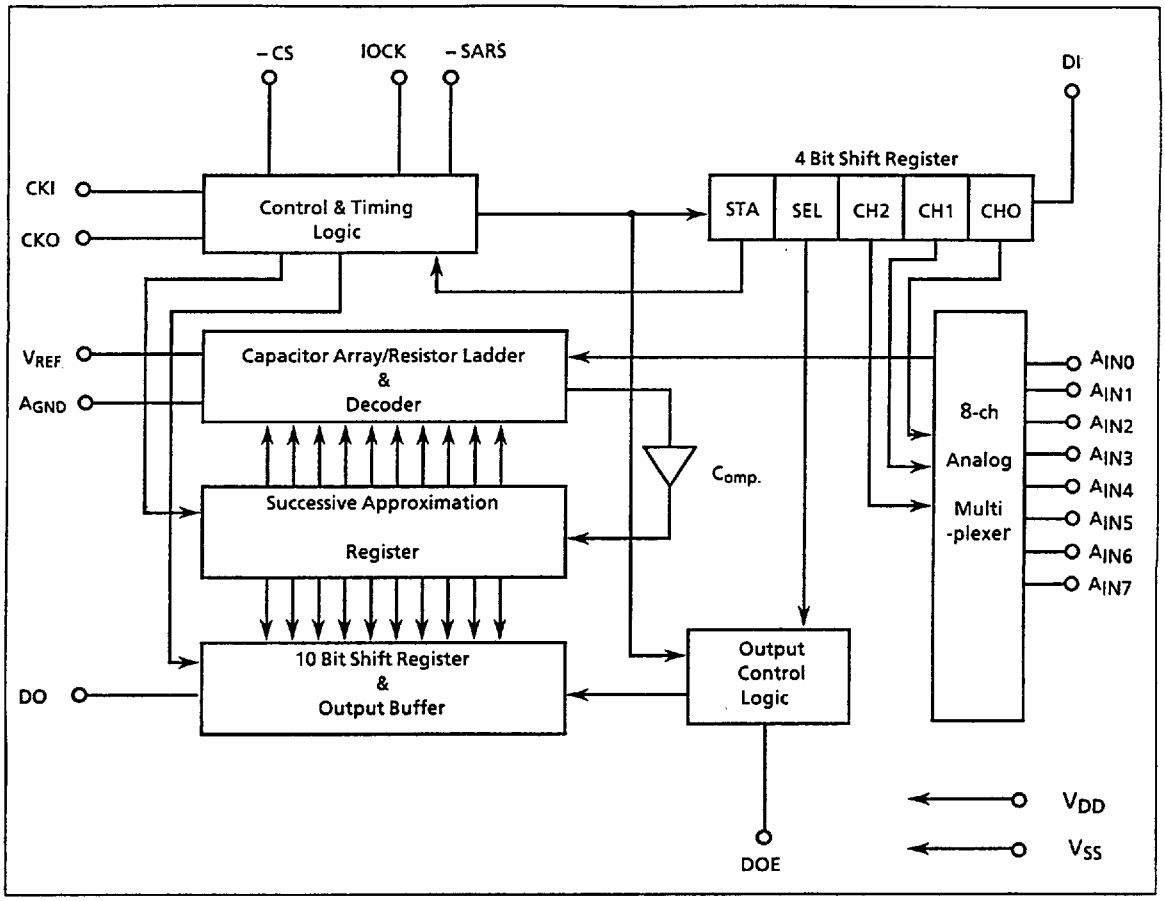
- ☐ High accuracy : 1LSB TYP.
- ☐ High speed conversion : 11μs @ fCKI = 2.0MHz
- ☐ Single power supply : 5.0V ± 10%
- ☐ Serial I/O
- ☐ Built-in 8-channel Analog multiplexer
- ☐ Latched 3-state output
- ☐ Built-in A/D Oscillator
- ☐ Zero or full scale adjustment free

APPLICATIONS

- ☐ Industrial Control Instruments
- ☐ Electrical Wiring Apparatus

* 1:Successive Approximation Register

3. SYSTEM DESCRIPTION



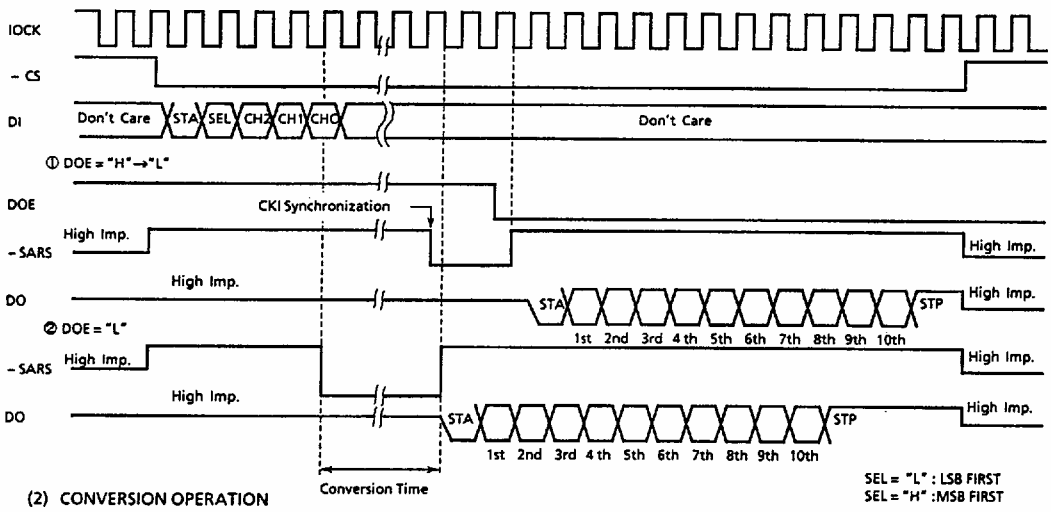
4. PIN DESCRIPTION

<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th>NAME & FUNCTION</th></tr>
<tr><td>1</td><td>– CS</td><td>[Chip Select]
At the falling edge of – CS, the device is set ready for conversion. When – CS is "H", the device is reset and all outputs go to high impedance state.</td></tr>
<tr><td>2</td><td>$A_{IN\,0}$</td><td rowspan="8">[Analog Input]
One of A_{IN0} to A_{IN7} Analog input Channels is selected according to the decoding of the Channel Select Bits (CH0, CH1, and CH2) applied to the DI input. The Full range of the input signed voltage is from A_{GND} to V_{REF}.
<table><tr><th>ON CHANNEL</th><th>CH2</th><th>CH1</th><th>CH0</th></tr><tr><td>$A_{IN\,0}$</td><td>L</td><td>L</td><td>L</td></tr><tr><td>$A_{IN\,1}$</td><td>L</td><td>L</td><td>H</td></tr><tr><td>$A_{IN\,2}$</td><td>L</td><td>H</td><td>L</td></tr><tr><td>$A_{IN\,3}$</td><td>L</td><td>H</td><td>H</td></tr><tr><td>$A_{IN\,4}$</td><td>H</td><td>L</td><td>L</td></tr><tr><td>$A_{IN\,5}$</td><td>H</td><td>L</td><td>H</td></tr><tr><td>$A_{IN\,6}$</td><td>H</td><td>H</td><td>L</td></tr><tr><td>$A_{IN\,7}$</td><td>H</td><td>H</td><td>H</td></tr></table></td></tr>
<tr><td>3</td><td>$A_{IN\,1}$</td></tr>
<tr><td>4</td><td>$A_{IN\,2}$</td></tr>
<tr><td>5</td><td>$A_{IN\,3}$</td></tr>
<tr><td>6</td><td>$A_{IN\,4}$</td></tr>
<tr><td>7</td><td>$A_{IN\,5}$</td></tr>
<tr><td>8</td><td>$A_{IN\,6}$</td></tr>
<tr><td>9</td><td>$A_{IN\,7}$</td></tr>
<tr><td>10</td><td>V_{SS}</td><td>[System Ground]
VSS = OV</td></tr>
<tr><td>11</td><td>A_{GND}</td><td>[Analog Ground]
A_{GND} defines the zero level of A_{IN}.</td></tr>
<tr><td>12</td><td>V_{REF}</td><td>[Reference Voltage]
V_{REF} defines the full scale of A_{IN}.</td></tr>
<tr><td>13</td><td>– SARS</td><td>[Successive Approximation Register Status]
– SARS is the signed output terminal which indicates the internal status of A/D converter (during conversion or after conversion that allows data to be read).</td></tr>
<tr><td>14</td><td>DO</td><td>[Data Output]
Output data is sent out in series</td></tr>
<tr><td>15</td><td>IOCK</td><td>[I/O Clock]
Clock input terminal for the input (read mode) or output (write mode) of serial data.</td></tr>
<tr><td>16</td><td>DOE</td><td>[Data Output Enable]
Timing control for conversion data output.</td></tr>
<tr><td>17</td><td>DI</td><td>[Data Input]
For starting the conversion a start bit ("L"Level) and channel select bit (from CH2 to CH0 in order) are to be applied.</td></tr>
<tr><td>18</td><td>CKO</td><td>[Clock Output]
Clock output terminal for A/D conversion.</td></tr>
<tr><td>19</td><td>CKI</td><td>[Clock Input]
Clock input terminal for A/D conversion.</td></tr>
<tr><td>20</td><td>V_{DD}</td><td>[System Power Supply]
V_{DD} = 5V ± 10%</td></tr>
</table>

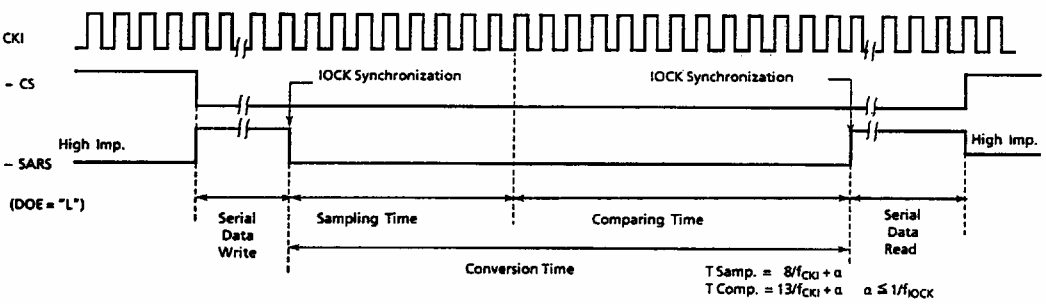
5. FUNCTIONAL DESCRIPTION

5.1 TIMING CHART

(1) WRITE / READ OPERATION OF SERIAL DATA



(2) CONVERSION OPERATION



5.2 SYSTEM INITIALIZATION

When −CS set high, all circuits except the output latch circuit are reset and all outputs are set to the high impedance state.

When the power is switched ON or a wrong operation occurs, set −CS high to initialize the internal circuits.

5.3 AD CONVERSION

When −CS goes low and after writing the serial data from DI, conversion begins. After a certain period for conversion, the conversion data is output in series from DO as determined by the output data format (SEL bit from DI) and output control enable (DOE). This completes one conversion cycle.During this period, −CS must be held low.

① Write Mode

After −CS goes low, output data format (SEL) and channel select (CH2,CH1,CH0) are written into the 4 Bit shift resister in order followed by the start bit (STA="L"). This is written on the raising edge of IOCK.

② Conversion Mode (TC = Tsamp + Tcomp)

After completing the write of serial data, the sampling cycle (Tsamp=8/fCKI+ α) status in the internal circuits, as well as sampling of the selected input voltage level. After the sampling cycle, the comparison cycle (Tcomp=13f_{CKI}+ α) stars and the analog input level is converted a ten bit digital data stream.

③ Read Mode

After the conversion cycle, the start bit (STA="L"), the 10-bit conversion data stream and the stop bit (STP="H") are output in that order synchronously with the falling edge of IOCK from DO according to output data format (SEL) and output control (DOE).

- Output Data Format

SEL= "L" :10-bit conversion data is output from LSB TO MSB.
SEL="H" :10-bit conversion data is output from MSB TO LSB.

- Output Control

DOE="L" : SAR status output (−SARS) goes low during conversion mode (Tc) and when the conversion is just completed, it goes high, then the conversion data stream output status.

DOE="H" →"L" : At the start of conversion, DOE is high, −SARS goes low at the end of the conversion, and conversion data is allowed reading. If DOE is set low, and −SARS goes high on the falling edge of IOCK ,the output of conversion data begins.

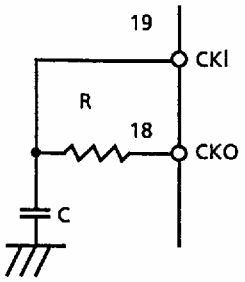
④ Serial Conversion

−CS is set high (100ns MIN) once every conversion cycle. This resets the internal circuitry for the next conversion.

5.4 CLOCK

Separate clocks are provided for A/D conversion (CKI,CKO) and serial data read / write functions (IOCK).

The clock for A/D conversion is composed of an oscillation circuit which uses an external resistor and capacitor. If desired an external clock may be used on the CKI pin.



6. ELECTRICAL CHARACTERISTICS

6.1 MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5$ to $V_{SS}+7$	V
Input Voltage	V_{IN}	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
Reference Supply Voltage	V_{REF}	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
Analog Ground Voltage	A_{GND}	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
Input Current	I_{IN}	± 10	mA
Power Dissipation	P_D	300	mW
Storage Temperature Range	T_{stg}	−65 to 150	°C

6.2 RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0.0V)

CHARACTERISTIC	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Input Voltage	V_{IN}		0.0	–	V_{DD}	V
Reference Voltage	V_{REF}	A_{GND} = 0.0V	3.0	V_{DD}	V_{DD}	V
Analog Grand Voltage	A_{GND}	V_{REF} = 5.0V	0.0	0.0	0.0	V
V_{REF} – A_{GND} Voltage		V_{DD} = 5.0V ± 10%	3.0	V_{DD}	V_{DD}	V
Clock Frequency	f_{CKI}	V_{DD} = 5.0V ± 10%	0.4	–	2.0	MHz
	f_{IOCK}	V_{DD} = 5.0V ± 10%	0.0001	–	2.0	MHz
Minimum Clock Pulse Width	$t_{w\,CKI}$	V_{DD} = 5.0V ± 10%	0.2	–	–	μs
	$t_{w\,IOCK}$	V_{DD} = 5.0V ± 10%	0.1	–	–	μs
Operation Temperature	T_{por}	V_{DD} = 5.0V ± 10%	−40	–	85	°C

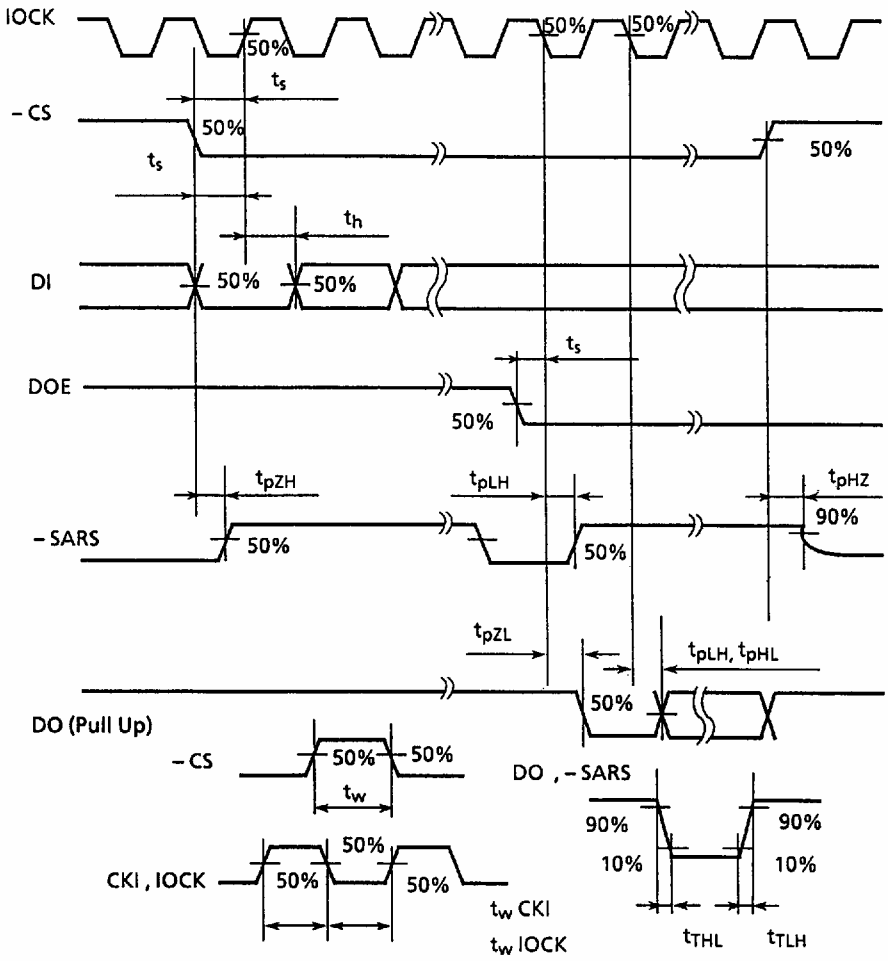
6.3 DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0V ± 10%, V_{SS} = 0.0V)

CHARACTERISTIC		SYMBOL	CONDITION	Ta = 25°C			Ta = −40 to 85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Voltage	"H" level	V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	V_{DD} − 0.05	V_{DD}	−	V_{DD} − 0.05	−	V
	"L" level	V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	−	0.0	0.05	−	0.05	
Output Current	"H" level	I_{OH}	$V_{OH} = V_{DD} - 0.4V$ $V_{IN} = V_{SS}, V_{DD}$	−0.44	−	−	−0.36	−	mA
	"L" level	I_{OL}	$V_{OL} = 0.4V$ $V_{IN} = V_{SS}, V_{DD}$	2.0	−	−	1.6	−	
Input Voltage	"H" level	V_{IH}		2.0	−	−	2.0	−	V
			CKI Terminal, V_{DD} = 5.0V	4.5	−		4.5		
	"L" level	V_{IL}		−	−	0.8	−	0.8	
			CKI Terminal, V_{DD} = 5.0V		−	0.5		0.5	
3-State Disable Current		I_{DH} I_{DL}	$V_{OH} = V_{DD}$, $V_{OL} = V_{SS}$	−	−	± 1.0	−	± 10	μA
Digital Input Current		I_{IH} I_{IL}	$V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	−	−	± 1.0	−	± 10	μA
On-Channel Input Current		I_{ON}	$V_{AIN} = V_{SS}, V_{DD}$ Sampling Cycle = 20μs	−	−	± 15	−	± 18	μA
Off-Channel Input Current		I_{OFF}	$V_{AIN} = V_{SS}, V_{DD}$	−	−	± 0.5	−	± 5	μA
Operating Consumption Current		I_{DD}	Sampling Cycle = 20μs	−	−	5.0	−	6.5	mA
Quiescent Supply Current		I_{DDS}	CKI = V_{SS}, V_{DD} IOCK = V_{SS}, V_{DD} − CS = V_{DD}	−	−	10	−	100	μA
Reference Resister		R_{Ref}		1.9	3.2	4.3	1.6	4.8	kΩ

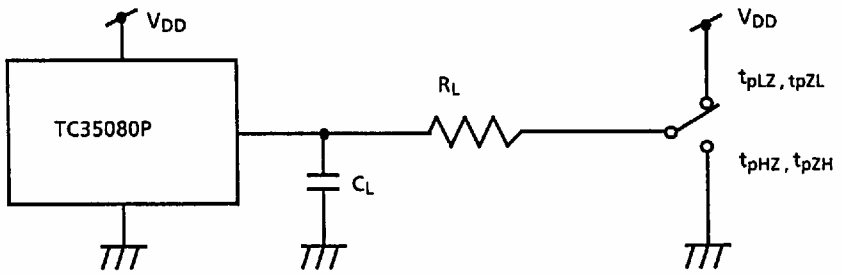
6.4 SWITCHING CHARACTERISTICS (V_{DD} = 5.0 ± 10%, V_{SS} = 0.0V, Ta = 25°C)

CHARACTERISTIC	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Rise/Fall Time DO, – SARS	t_{TLH} t_{THL}	CL = 50pF	–		100	ns
Propagation Delay Time DO, – SARS	t_{PLH} t_{PHL}	CL = 50pF	–		200	ns
3-State Output Enable Time DO, – SARS	t_{PZH} t_{PZL}	CL = 50pF RL = 1KΩ	–		200	ns
3-State Output Disable Time DO, – SARS	t_{PHZ} t_{PLZ}	CL = 50pF RL = 1KΩ	–		200	ns
Minimum Pulse Width – CS	$t_{W}(H)$		–		100	ns
Minimum Set up Time DI, DOE	t_s		–		100	ns
Minimum Holding Time DI, DOE	t_h		–		100	ns
Input Capacitance	$C_{IN}1$	Digital Input	–	5	–	pF
	$C_{IN}2$	Analog Input (OFF)	–	5	–	
	$C_{IN}3$	Analog Input (ON)	–	40	–	
Output Capacitance	C_{OUT}	3-State Output	–	10	–	pF

6.4.1 SWITCHING CHARACTERISTICS TEST WAVE FORMS



6.4.2 3-STATE OUTPUT TEST CIRCUIT



6.5 SYSTEM CHARACTERISTICS (Ta = −40 to 85°C)

CHARACTERISTIC	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT.
Zero Point Error	E_{ZR}	V_{DD} = 5.0V V_{REF} = 5.000V f_{CKI} = 2.0MHz	–	± 1/4	± 1	LSB
Full Scale Error	E_{FS}		–	± 1/4	± 1	LSB
Nonlinearity	E_{LI}		–	± 1/2	–	LSB
Total Error	E_T		–	± 3/4	± 1.5	LSB
Conversion Time	T_C	f_{CKI} = 2.0MHz	–	11	–	μs