SUMMIT
MICROELECTRONICS, Inc.

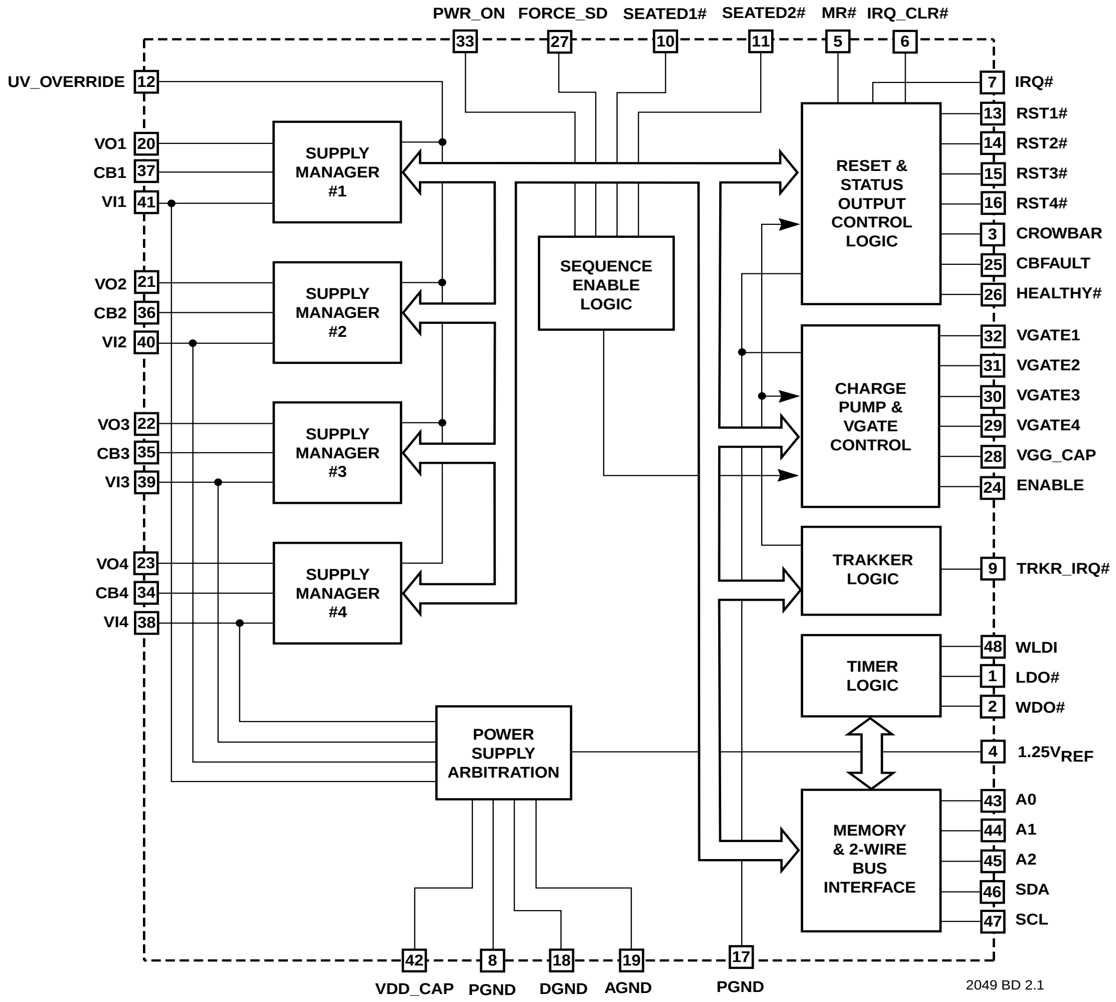
SMT4004

Distributed Power Hot-Swap Controller

FEATURES

- Programmable Voltage and Current Monitoring
  - Monitors 4 independent supplies
  - Programmable Host-side Under- and Over-Voltage Thresholds
  - Programmable Card-side Under-Voltage Monitors
  - Programmable Card-side Circuit Breaker Delay and QuickTrip™ Threshold Levels
- Programmable Card-side Trakker Function
  - Programmable Slew Rate Control
  - Guarantees and Enforces Supply Differential Tracking
- Programmable Watchdog and Longdog Timers (0 to 6.4 seconds)
- Operates From Any One of Four Supply Voltages
- Nonvolatile Fault Register
  - Records Source of Any Interrupt
  - Readable in “Dead Board” Environment
- All Communications to Configuration Registers and Memory Array are via 2-wire Serial Interface

FUNCTIONAL BLOCK DIAGRAM



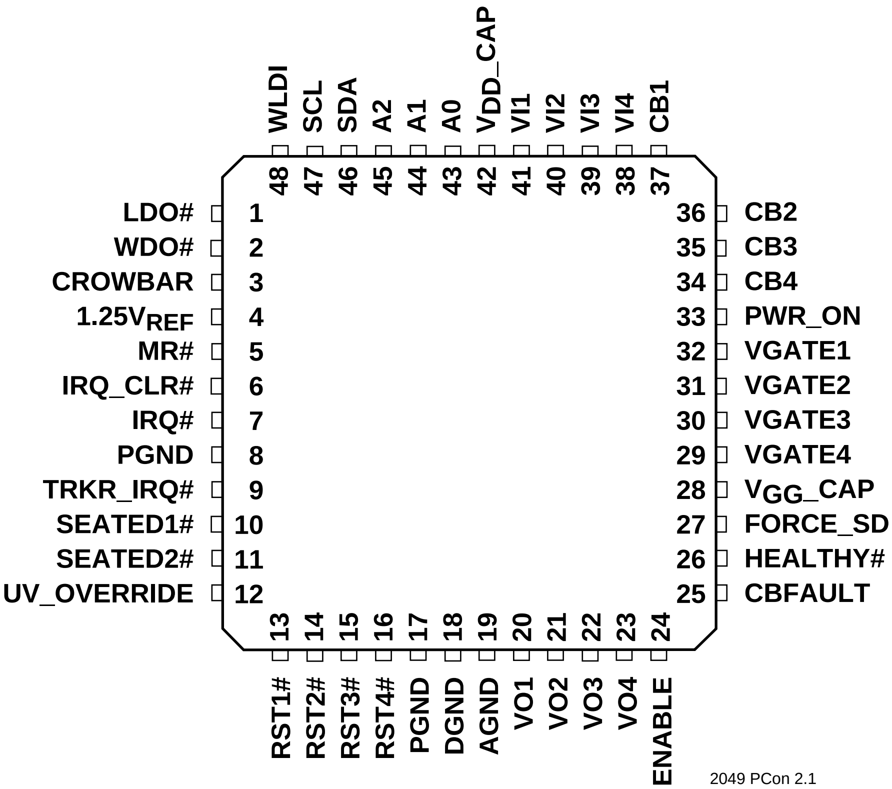
DESCRIPTION

The SMT4004 is a fully integrated programmable voltage manager IC, providing supervisory functions and tracking control for up to four independent power supplies. The four internal managers perform the following functions: Monitor source (bus-side) voltages for under- and over-voltage conditions, monitor each supply for over-current conditions, monitor back end (card-side) voltages for two staged levels of under-voltage conditions, insure power to the card-side logic tracks within the specified parametric limits, and provide supply status information to a host processor.

The SMT4004 incorporates nonvolatile programmable circuits for setting all of the monitored thresholds for each manager. Individual functions are also programmable allowing interrupts or reset conditions to be generated by any combination of events. Because of a proprietary EEPROM technology that it employs it is also able to store fault conditions as they occur. In the case of a catastrophic failure the fault is recorded in the registers and then can be read for analysis.

PIN CONFIGURATION

48-Pin TQFP



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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-55°C to 125°C
Storage Temperature	-65°C to 150°C
Lead Solder Temperature (10 secs)	300 °C
Terminal Voltage with Respect to GND:	
V_0, V_1, V_2, and V_3	-0.3V to 6.0V
All Others	-0.3V to 6.0V

*COMMENT

Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

DC OPERATING CHARACTERISTICS

(**Over Recommended Operating Conditions; Voltages are relative to GND**)

Symbol	Parameter	Notes			Min.	Typ.	Max.	Units
VI	Supply voltages VI1 through VI4	Highest VI (≥2.7V) powers the SMT4004			2.7		5.5	V
I_{DD} On	Power supply current	PWR_ON and ENABLE active				1	3	mA
I_{DD} Off		ENABLE inactive					0.1	mA
P_{VIT}	Programmable VI input threshold range	8-bit resolution, 20mV/bit			0.9		6.0	V
VI_{HYS}	OV/UV trip hysteresis					10		mV
V_{CB}	Circuit breaker trip voltage				20	25	30	mV
CB_{DELAY}	Over-current filter	Programmable. Set by Register R1B, data bits D1 & D0, respectively	0	0		25		µs
			0	1		50		µs
			1	0		100		µs
			1	1		200		µs
V_{QCB}	Quick-trip voltage	Programmable. Set by Register R1A, data bits D7 & D6 (*e.g.*), respectively	0	0		Off		
			0	1		75		mV
			1	0		100		mV
			1	1		150		mV
V_{REF}	1.25V_{REF} output voltage	R_{LOAD} = 2kΩ			1.23	1.25	1.27	V
V_{VG} On	VGATE drive output voltage	MOSFET switches On			14		16	V
V_{VG} Off		VG_{SINK} = 1mA			0		0.4	V
I_{VG}	VGATE drive output current	MOSFET switches On					80	µA
SR_{VG}	VGATE output voltage slew rate	Programmable. Set by Register R10, data bits D3 & D2 or D1 & D0, respectively	0	0		100		V/s
			0	1		250		V/s
			1	0		500		V/s
			1	1		1000		V/s
SR_{DELTA}	TRAKKER slew differential	VO pins, delta differential allowed				100		mV
P_{OVT}	Programmable card-side voltage threshold range	8-bit resolution, 20mV/bit			0.9		6.0	V
OV_{HYS}	OV input hysteresis					10		mV
V_{IH}	Input high voltage	VI = 2.7V			0.9 × VI		VI	V
		VI = 5V			0.7 × VI		VI	V
V_{IL}	Input low voltage	VI = 2.7V			–0.1		0.1 × VI	V
		VI = 5V			–0.1		0.3 × VI	V
V_{OL}	Open drain outputs	I_{SINK} = 2mA			0		0.4	V
t_{CROW}	Crowbar output pulse width	2.5V min. into 1kΩ			4	5	7	µs

2049 Elect Table 1.0

PIN DESCRIPTIONS AND DEVICE OPERATION

THE *TRAKKER* SUPPLY VOLTAGES

The **VI** inputs of all four supply managers are diode ORed and tied to the device's internal V_{DD} node. The ***TRAKKER*** will use the highest VI input for its supply voltage. At least one VI input must be at or above 2.7V for proper device operation.

V_{DD}_CAP — Charge storage connection for the chip's internal power suply. For most applications a 10µF capacitor should be connected to his pin.

V_{GG}_CAP — This pin should be tied to a capacitor to be charged by the charge pump. The capacitor should be of sufficient size so as to provide current to the VGATE outputs under varying load conditions.

PGND — Power ground

DGND — Digital Ground

AGND — Analog Ground

TIMERS

LDO# — The longdog timer output is an active-low open-drain output that can be wire-ORed with other open-drain signals. The longdog timer is generally programmed to generate an output at a time interval longer than the watchdog timer. The time interval is programmed in Register ***R1C***.

WDO# — The watchdog timer output is an active-low open-drain output that can be wire-ORed with other open-drain signals. The watchdog timer is generally programmed to generate an output at a time interval shorter than the longdog timer. The time interval is programmed in Register ***R1C***.

WLDI — Watchdog and longdog timer reset input. A low-to-high transition on this pin will reset both the watchdog timer and the longdog timer.

The watchdog and longdog work in tandem: resetting one resets the other. Generally, the longdog will be programmed to time out sometime after the watchdog. As an example, the WDO# output could be used to generate a warning interrupt and the LDO# output could be tied to a system reset line.

Both timers can be turned off, facilitating system debug and also allowing operating systems to 'boot up' and configure themselves without interrupts or resets.

SUPPLY MANAGERS

The electrical placement of the SMT4004 on a printed circuit card is such that it separates the host power supply and any on-board DC-to-DC converters (or LDOs) from the backend circuitry such as multiple DSPs, microprocessors and associated glue logic. The host supplies, and any other regulated voltages that will be "switched" by the device, are referred to as bus-side voltages. The voltages that are on the backend circuitry side of the switches are referred to as card-side voltages.

The four supply manager blocks are identical. Each contains three primary functional blocks: the first monitors the bus-side voltages, the second monitors the card-side voltages, and the third monitors over-current conditions for that particular supply.

BUS-SIDE MANAGEMENT

Figure 1 illustrates the functional blocks of the four supply managers. Each manager block can be independently enabled or electrically removed from the device.

The VI input monitors the bus-side voltage for both under-voltage and over-voltage conditions. The thresholds for the under-voltage detection for VI inputs are programmed in Registers ***R00*** through ***R03***. The VI input is effectively the V_{REF} of a nonvolatile DAC. The DAC has been designed so that the threshold can be determined by multiplying the binary value of the Register times 20mV and adding that to 0.9V in the formula $P_{VIT} = 0.9V + (0.2mV \times n)$, where n is the register value (0 - 255 decimal). This allows very precise monitoring of voltages in the range of 0.9V to 6V without the use of external resistor divider networks.

The over-voltage section works in a similar manner, with the formula being $Offset = (P_{VIT} \times 1.2) + [(0.04 \times P_{VIT}) \times n]$, where n is the register value in ***R04*** through ***R07***. All enabled manager blocks must ensure their respective VI inputs are within the programmed limits before the VGATE outputs can be turned on and the ***TRAKKER*** logic enabled. The VI comparator outputs can also be used to generate a general interrupt.

It should be noted that either one or both of the bus-side monitors could be disabled via Registers ***R04*** through ***R07***.

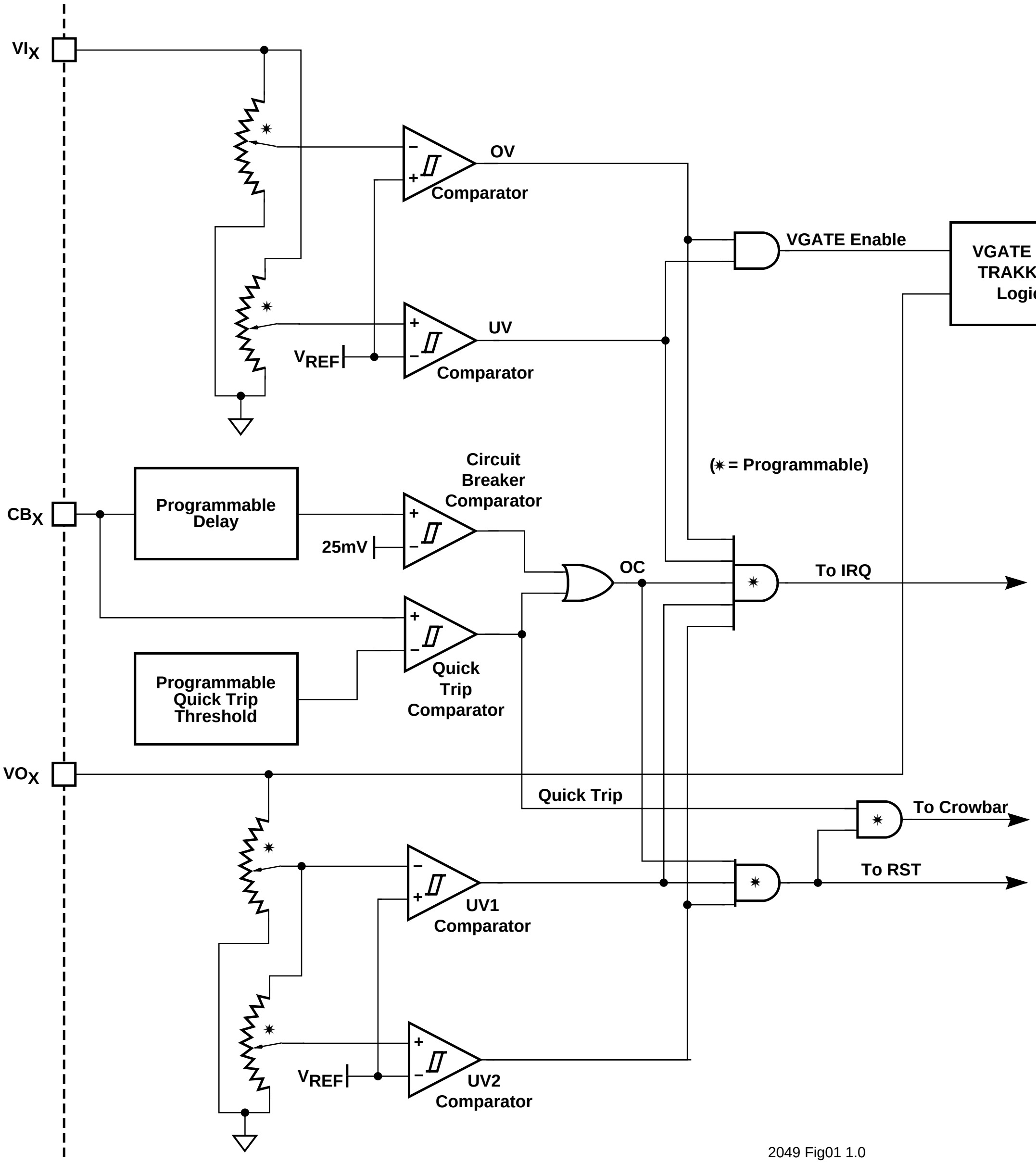


Figure 1. Supply Manager Circuit

CARD-SIDE MANAGEMENT

On the card-side the ***TRAKKER*** monitors two programmable under-voltage thresholds on the VO inputs: UV1 and UV2. UV1 can be used to generate a warning interrupt that the supply is decaying, and UV2 can be used to generate a reset condition or a crowbar output. The card-side under-voltage (UV1) threshold value is programmed in Registers **R08** through **R0B**. Like the bus-side thresholds the levels can be programmed in 20mV increments (on top of 0.9V). The second level (UV2) is determined by the formula $UV2 = UV1 - [(UV1 \times 0.01) \times n]$, where n is the value in Registers **R0C** through **R0F**.

It should be noted that either one or both of the card-side monitors can be disabled via Registers ***R0C*** through ***R0F***.

OVER-CURRENT PROTECTION

The CB inputs are the circuit breaker inputs for the supply voltages. With a series resistor placed in the supply path between VI and CB the circuit breaker will trip whenever the voltage across the resistor exceeds 25mV.

The on-board electronic circuit breaker can be programmed to application specific levels. The circuit breaker delay defines the period of time the voltage drop across R_S is greater than 25mV but less than V_{QCB} before the VGATE output will be shut down. This is effectively a filter to prevent spurious shutdowns of VGATE. The delays that can be programmed are 25µs, 50µs, 100µs and 200µs. The programmable delay bits are located in Register ***R1B***.

The Quick-Trip circuit breaker threshold (V_{QCB}) can be set to 150mV, 100mV, 75mV or off (Register ***R1A***). This is the threshold voltage drop across R_S that is placed between V_{SS} and CBSense. If the voltage drop exceeds the programmed threshold, the electronic circuit breaker will immediately trigger with no delay.

The outputs of these comparators can be used to generate interrupts and reset conditions and toggle the crowbar output.

POWER-ON SEQUENCING

In order to begin sequencing of the card-side supplies (ramping the VGATE outputs) a number of conditions must be met. All enabled bus-side voltages must be above their respective under-voltage thresholds, **the card-side voltages** (*e.g.*, residual capacitor stored potentials) **must be near zero volts**, and **the following inputs must be properly set**.

ENABLE — When active the ENABLE input brings the IC out of a standby mode where the charge pump supplying the VGATE outputs is turned on (and begins charging the VGG_CAP) and the bandgap reference is turned on. The ENABLE input can be programmed to be either active low (default from the factory) or active high (Register ***R1B***).

SEATED1# and SEATED2# — the SEATED inputs are effectively two additional enable inputs that must be low to enable the sequencing of the card-side voltages. In a staggered pin environment these inputs can be tied to the "short" pins, insuring the card is fully seated before any power is applied to the card-side logic. These inputs can also be tied to card insertion switches to indicate proper seating.

PWR_ON — the PWR_ON input is the last input that will typically be driven to enable power sequencing to the card-side. The PWR_ON input can be programmed to be either active low (default from the factory) or active high (Register ***R1B***).

TRAKKING AND SOFTSTART CONTROL

VGATE — The VGATE outputs are used to control the "turning-on" of the card-side voltages. The ramp rate (for both turn-on and turn-off) of the outputs is programmable from 100V/s to 1000V/s (Register ***R10***). The four outputs ramp at the same slew-rate, so normally there will be no differential voltage between any of the supplies until each reaches its maximum level.

The ramp rates are inherently adaptive. That is, if the difference between any VO input is greater than 100mV in the linear region, the slew rate will be increased or decreased to minimize the differential. The comparisons are made between VO1 and VO2, VO2 and VO3, VO3 and VO4, and VO4 and VO1. If at any time a differential of greater than 300mV is detected a pre-programmed (Register ***R10***) action can be taken. The ***TRAKKER*** can shut down the offending supply, generate an interrupt output, or ignore the situation.

If **SoftStart** is enabled (Registers ***R0C*** through ***R0F***) the supply or supplies designated will be ramped as soon as the input conditions are met and no Trakking will be performed. Any supply not designated as a softstart supply will not be ramped until the designated supply has reached its VO threshold. This type of operation would commonly be used where a bus voltage (*e.g.*, 5V) is first switched to a DC-to-DC converter or group of LDOs; and then their outputs would be switched in a Trakking mode to the card-side logic.

Supply managers designated for Trakking will not begin start-up until the soft start channels are fully turned on. The delay is approximated by the formula $t_D = 16{,}000 \div SR$, where t_D is the time delay in milliseconds between the PWR_ON signal going high and the start of the tracking ramp-up, and SR is the programmed start-up slew rate in V/s. For example, the time delay for a programmed slew rate of 500V/s is: $t_D = 16{,}000 \div 500 = 32$ms.

POWER MANAGEMENT STATUS OUTPUTS

The ***TRAKKER*** has two types of status outputs that it provides to the host system or host processor resident on its board. One type of output is "hardwired" internally and the other is programmable.

HEALTHY# — The HEALTHY output is an active-low open-drain output that can be wire-ORed with other open-drain signals. It is driven low when all of the enabled managers' card-side voltages are valid and there are no over-current conditions. The signal is used to indicate the power supplies are within their programmed operating limits.

CBFAULT — CBFAULT is driven active whenever an over-current condition is detected. It is a programmable output that can be either an active high or active low (factory default) output.

RESETS

RST1# to RST4# — Associated with each manager is a reset output. They are active-low open-drain outputs that can be wire-ORed with other open-drain signals. The user can select UV1, UV2 and/or an over-current condition as the trigger for the reset pulse by programming Registers ***R11*** and ***R12*** (the default condition from the factory is all conditions generate a reset). The reset pulse width is adjustable by writing to Register ***R1C*** (default condition from the factory is pulse of 200ms).

MR# — When driven low the manual reset input will automatically drive all four reset outputs low.

INTERRUPTS

IRQ# — the IRQ output is an active low open-drain output that is driven low whenever one or more of its programmed triggers is active. There are twenty programmable sources for generating the interrupt: bus-side over- and under-voltage, card-side under-voltage 1 and 2, and an over-current condition. Each source is individually enabled by writing to Registers ***R13, R14*** and ***R15***. The default from the factory is to enable all sources. The IRQ# output can only be cleared by bringing **IRQ_CLR#** low, or after a power-down/power-up sequence.

TRKR_IRQ# — the ***TRAKKER*** interrupt indicates there was a skew of greater than 300mV during the power on cycle. The source of the TRKR_IRQ# is programmable and can be initiated by any one of the managers. The configuration Registers ***R11*** and ***R12*** select the source of interrupt. Configuration Register ***R10*** enables the TRKR_IRQ# output (or one of three other options). The default from the factory is to enable all sources. The *TRKR_IRQ#* output can only be cleared by bringing IRQ_CLR high or after a power-down/power-up sequence.

In order to avoid false interrupts during a power-on sequence there is a programmable "power-on interrupt hold-off" register. The delay can be programmed from 200ms to 1600ms. The interrupt hold-off is in Register ***R15*** and its default value from the factory will be 1600ms.

FAULT REGISTER

Whenever an interrupt is generated the cause of the fault will be recorded in the nonvolatile status Register. In order to avoid false recordings during power-down situations, no faults will be recorded if the PWR_ON input has been deactivated. The fault Registers are located at ***R1D*** through ***R1F***. The fault source is indicated by a "1" in the assigned bit location. Overwriting the fault Register with "0's" is the only way to clear a recorded fault condition.

CROWBAR — The CROWBAR output is another form of status output. The conditions to generate a crowbar output are programmable in Register ***R19***. Whenever one of the conditions occurs the CROWBAR output will strobe. Rapid shutdown of the card-side supplies may be required to prevent damage to the DSP's or microprocessors. SCRs with a fast turn-on time make excellent crowbar devices and only need a pulse of gate current to 'trigger.'

MEMORY AND REGISTER ACCESS

A0, A1 & A2 — The address pins are biased either to the highest VI pin or GND, and provide a mechanism for assigning a unique address to the SMH4004.

SDA — SDA is a bidirectional serial data pin. It is configured as an open drain output and will require a pull-up to the highest VI pin.

SCL — SCL is the serial clock input.

MISCELLANEOUS MANAGER SIGNALS

1.25V$_{REF}$ — This pin is a 1.25V Reference output that can be used in conjunction with external circuitry.

UV_OVERRIDE — The Under-Voltage Override input will disable the under-voltage comparators. This can be used for board test and also during system margining.

FORCE_SD — When asserted the Force Shut Down input will immediately clamp the VGATE outputs to ground. This can be used in conjunction with the **CROWBAR**. The active level for **FORCE_SD** is programmable and accessible in Register ***R1B***.

REGISTER FORMATS AND FUNCTIONS

There are four basic register types. The first are those that set a monitoring threshold where the binary value written to the register is multiplied times the base incremental voltage. The second type enables or disables a specific function: unless otherwise indicated a “1” will always enable the function and a “0” will disable or deselect that function. **Note**: only the enabled condition will be depicted in the following tables. The third Register type allows selection of various timer values. These are not incremental, like the thresholds, but specific bit patterns select specific timer values. The fourth register type is the nonvolatile fault register that records fault conditions. A “0” in any bit location indicates its corresponding monitor function was within specified limits when the fault occurred. A “1” in any bit location indicates its corresponding monitor function was outside its specified limits when the fault occurred.

Bus-side Under-voltage Threshold

Registers **00**, **01**, **02** and **03** are identical. Their contents select the under-voltage threshold for the VI1, VI2, VI3 and VI4 inputs, respectively.

Register R00, R01, R02, R03								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	1	1	1	1	1	1	1	Highest threshold adjustment = 6.0V
0	0	0	0	0	0	0	0	Lowest threshold adjustment = 0.9V
0	0	0	0	0	0	1	0	Threshold = 0.9V + (2 × .02V) = 0.94V, *e.g.*

2049 Table01 1.0

Bus-side Under-voltage Threshold Enable and Over-voltage Offset

Registers **04**, **05**, **06** and **07** are identical. Their contents determine whetheror not the under- or over-voltage capabilities are enabled, and establish the over-voltage offset value for the VI1, VI2, VI3 and VI4 inputs, respectively.

Register R04, R05, R06, R07								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
x	**1**	x	x	x	x	x	x	Enables under voltage detection
x	x	**1**	x	x	x	x	x	Enables over voltage detection
x	x	x	**0**	**0**	**0**	**1**	**0**	Threshold = ($VI_{THRESHOLD}$ + 20%) + ($\boldsymbol{n} \times .04VI_{THRESHOLD}$) where ***n*** = register binary value

2049 Table02 1.0

Card-side Under-voltage Threshold

Registers **08**, **09**, **0A** and **0B** are identical. Their contents select the under-voltage threshold for the VO1, VO2, VO3 and VO4 inputs, respectively.

Register R08, R09, R0A, R0B								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	1	1	1	1	1	1	1	Highest threshold adjustment = 6.0V
0	0	0	0	0	0	0	0	Lowest threshold adjustment = 0.9V
0	0	0	0	0	0	1	0	Threshold = 0.9V + (2 × .02V) = 0.94V, *e.g.*

2049 Table03 1.0

Card- side Under-voltage Threshold Enable and Over-voltage Offset

Registers **0C**, **0D**, **0E** and **0F** are identical These registers will either enable or disable their associated power management functions and soft start capability. Their contents also determine whether the under- or over-voltage capabilities are enabled and the contents establish the over-voltage offset value for the VO1, VO2, VO3 and VO4 inputs, respectively.

Register R0C, R0D, R0E, R0F								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	x	x	x	x	x	x	x	Power management channel enabled
x	**1**	x	x	x	x	x	x	1 = Enable soft start; 0 = Enable Trakking
x	x	**1**	x	x	x	x	x	Enables under voltage 2
x	x	x	**0**	**0**	**0**	**1**	**0**	Threshold = $(UV1) - (n \times UV1 \times 0.01)$ where n = register binary value

2049 Table04 1.0

Addressing and Slew Rate Control

Configuration Register **10** is used to configure the addressing protocol for the **TRAKKER**. Bit 7 determines whether the device will respond with an acknowledge to any bus request addressing its device type identifier, or whether it will be selective and only respond if the A2, A1 and A0 bits match the biasing of the external pins. Bit 6 selects the device type identifier to be used for the memory array.

<table>
<tr><th colspan="9">Register R10</th></tr>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Action</th></tr>
<tr><td>0</td><td>x</td><td colspan="6" rowspan="4">x</td><td>Responds only to Pin biased bus addresses</td></tr>
<tr><td>1</td><td>x</td><td>Responds to all bus addresses</td></tr>
<tr><td>x</td><td>0</td><td>Memory device-type identifier 1010</td></tr>
<tr><td>x</td><td>1</td><td>Memory device-type identifier 1011</td></tr>
<tr><td colspan="9">TRAKKER over/under 300mV differential action</td></tr>
<tr><td colspan="2" rowspan="4">x</td><td>0</td><td>0</td><td colspan="4" rowspan="4">x</td><td>Ignore</td></tr>
<tr><td>0</td><td>1</td><td>Shut down the faulty supply and TRKR_IRQ#</td></tr>
<tr><td>1</td><td>0</td><td>Shut down all supplies and TRKR_IRQ#</td></tr>
<tr><td>1</td><td>1</td><td>Generate TRKR_IRQ#</td></tr>
<tr><td colspan="9">TRAKKER slew rate low to high (off to on)</td></tr>
<tr><td colspan="4" rowspan="4">x</td><td>0</td><td>0</td><td colspan="2" rowspan="4">x</td><td>100V/s</td></tr>
<tr><td>0</td><td>1</td><td>250V/s</td></tr>
<tr><td>1</td><td>0</td><td>500V/s</td></tr>
<tr><td>1</td><td>1</td><td>1000V/s</td></tr>
<tr><td colspan="9">TRAKKER slew rate high to low (on to off)</td></tr>
<tr><td colspan="6" rowspan="4">x</td><td>0</td><td>0</td><td>100V/s</td></tr>
<tr><td>0</td><td>1</td><td>250V/s</td></tr>
<tr><td>1</td><td>0</td><td>500V/s</td></tr>
<tr><td>1</td><td>1</td><td>1000V/s</td></tr>
</table>

2049 Table05 1.0

Reset Source Select and *TRAKKER* IRQ Select (for Supply Managers 1 and 2)

Register R11								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
VO1-1	**VO1-2**	**VI1O**	**TRKR1**	**VO2-1**	**VO2-2**	**VI2O**	**TRKR2**	
1	x	x	x	x	x	x	x	Selects card-side1 UV1 as RST#1 trigger
x	**1**	x	x	x	x	x	x	Selects card-side1 UV2 as RST#1 trigger
x	x	**1**	x	x	x	x	x	Selects CBI1 as RST#1 trigger
x	x	x	**1**	x	x	x	x	Selects TRK1 error as an interrupt source
x	x	x	x	**1**	x	x	x	Selects card-side2 UV1 as RST#2 trigger
x	x	x	x	x	**1**	x	x	Selects card-side2 UV2 as RST#2 trigger
x	x	x	x	x	x	**1**	x	Selects CBI2 as RST#2 trigger
x	x	x	x	x	x	x	**1**	Selects TRK2 error as an interrupt source

2049 Table06 1.0

Reset Source Select and *TRAKKER* IRQ Select (for Supply Managers 3 and 4)

Register R12								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
VO3-1	**VO3-2**	**VI3O**	**TRKR3**	**VO4-1**	**VO4-2**	**VI4O**	**TRKR4**	
1	x	x	x	x	x	x	x	Selects card-side3 UV1 as RST#3 trigger
x	**1**	x	x	x	x	x	x	Selects card-side3 UV2 as RST#3 trigger
x	x	**1**	x	x	x	x	x	Selects CBI3 as RST#3 trigger
x	x	x	**1**	x	x	x	x	Selects TRK3 error as an interrupt source
x	x	x	x	**1**	x	x	x	Selects card-side4 UV1 as RST#4 trigger
x	x	x	x	x	**1**	x	x	Selects card-side4 UV2 as RST#4 trigger
x	x	x	x	x	x	**1**	x	Selects CBI4 as RST#4 trigger
x	x	x	x	x	x	x	**1**	Selects TRK4 error as an interrupt source

2049 Table07 1.0

IRQ Source Select (for Supply Managers 1 and 2)

Register R13								
D7	D6	D5	D4	D3	D2	D1	D0	Action
VI1-OV	VI1-UV	VO1-1	VO1-2	VI2-OV	VI2-UV	VO2-1	VO2-2	
1	x	x	x	x	x	x	x	Selects bus-side1 OV as an IRQ# trigger
x	**1**	x	x	x	x	x	x	Selects bus-side1 UV as an IRQ# trigger
x	x	**1**	x	x	x	x	x	Selects card-side1 UV1 as an IRQ# trigger
x	x	x	**1**	x	x	x	x	Selects card-side1 UV2 as an IRQ# trigger
x	x	x	x	**1**	x	x	x	Selects bus-side2 OV as an IRQ# trigger
x	x	x	x	x	**1**	x	x	Selects bus-side2 UV as an IRQ# trigger
x	x	x	x	x	x	**1**	x	Selects card-side2 UV1 as an IRQ# trigger
x	x	x	x	x	x	x	**1**	Selects card-side2 UV2 as an IRQ# trigger

2049 Table08 1.0

IRQ Source Select (for Supply Managers 3 and 4)

Register R14								
D7	D6	D5	D4	D3	D2	D1	D0	Action
VI3-OV	VI3-UV	VO3-1	VO3-2	VI4-OV	VI4-UV	VO4-1	VO4-2	
1	x	x	x	x	x	x	x	Selects bus-side3 OV as an IRQ# trigger
x	**1**	x	x	x	x	x	x	Selects bus-side3 UV as an IRQ# trigger
x	x	**1**	x	x	x	x	x	Selects card-side3 UV1 as an IRQ# trigger
x	x	x	**1**	x	x	x	x	Selects card-side3 UV2 as an IRQ# trigger
x	x	x	x	**1**	x	x	x	Selects bus-side4 OV as an IRQ# trigger
x	x	x	x	x	**1**	x	x	Selects bus-side4 UV as an IRQ# trigger
x	x	x	x	x	x	**1**	x	Selects card-side4 UV1 as an IRQ# trigger
x	x	x	x	x	x	x	**1**	Selects card-side4 UV2 as an IRQ# trigger

2049 Table09 1.0

IRQ Power-on Delay and Source Select (for All Supply Managers)

Register R15								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
x	**0**	**0**	**0**	x	x	x	x	IRQ# power on delay off (0ms)
x	**1**	**0**	**0**	x	x	x	x	IRQ# power on delay 200ms
x	**1**	**0**	**1**	x	x	x	x	IRQ# power on delay 400ms
x	**1**	**1**	**0**	x	x	x	x	IRQ# power on delay 800ms
x	**1**	**1**	**1**	x	x	x	x	IRQ# power on delay 1600ms
x	x	x	x	**1**	x	x	x	Supply 1 over-current triggers IRQ#
x	x	x	x	x	**1**	x	x	Supply 2 over-current triggers IRQ#
x	x	x	x	x	x	**1**	x	Supply 3 over-current triggers IRQ#
x	x	x	x	x	x	x	**1**	Supply 4 over-current triggers IRQ#

2049 Table10 1.0

CROWBAR Source Enables

Register R19								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
FORCE _SD	**IRQ#**	**TRK_ IRQ#**	**RST1**	**RST1**	**RST1**	**RST1**	**QUICK TRIP**	
1	x	x	x	x	x	x	x	Enable FORCE_SD
x	**1**	x	x	x	x	x	x	General interrupt
x	x	**1**	x	x	x	x	x	TRAKKER interrupt
x	x	x	**1**	x	x	x	x	Supply 1 reset
x	x	x	x	**1**	x	x	x	Supply 2 reset
x	x	x	x	x	**1**	x	x	Supply 3 reset
x	x	x	x	x	x	**1**	x	Supply 4 reset
x	x	x	x	x	x	x	**1**	Quick Trip condition

2049 Table11 1.0

Quick-trip Voltage Thresholds

Register R1A								
D7	D6	D5	D4	D3	D2	D1	D0	Action
MANAGER 1		MANAGER 2		MANAGER 3		MANAGER 4		
0	0	x						Off
0	1							75mV
1	0							100mV
1	1							150mV
x		0	0	x				Off
		0	1					75mV
		1	0					100mV
		1	1					150mV
x				0	0	x		Off
				0	1			75mV
				1	0			100mV
				1	1			150mV
x						0	0	Off
						0	1	75mV
						1	0	100mV
						1	1	150mV

2049 Table12 1.0

Over-current Delay and Active Pin Level Select

Register R1B								
D7	D6	D5	D4	D3	D2	D1	D0	Action
na	na	CB	EN	PO	F-SD	OC - DLY		
x	x	1	x	x	x	x	x	CBFAULT output (1 = active high)
		x	1	x	x	x	x	ENABLE input (1 = active high)
		x	x	1	x	x	x	PWR_ON input (1 = active high)
		x	x	x	1	x	x	FORCE_SD input (1 = active high)
Over-current delay								
x	x	x	x	x	x	0	0	25µs
		x	x	x	x	0	1	50µs
		x	x	x	x	1	0	100µs
		x	x	x	x	1	1	200µs

2049 Table13 1.0

Timer Configuration Register

Register R1C								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
RESET PERIOD		**LONGDOGTIMER**			**WATCHDOG TIMER**			
0	**0**	x			x			25ms
0	**1**							50ms
1	**0**							100ms
1	**1**							200ms
x		**0**	**x**	**x**	x			Off
		1	**0**	**0**				800ms
		1	**0**	**1**				1600ms
		1	**1**	**0**				3200ms
		1	**1**	**1**				6400ms
x		x			**0**	**x**	**x**	Off
					1	**0**	**0**	400ms
					1	**0**	**1**	800ms
					1	**1**	**0**	1600ms
					1	**1**	**1**	3200ms

2049 Table14 1.0

Status Registers

SR1D								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
VI1-UV	**VI2-UV**	**VI3-UV**	**VI4-UV**	**VI1-OV**	**VI2-OV**	**VI3-OV**	**VI4-OV**	
1	x	x	x	x	x	x	x	Bus-side1 UV
x	**1**	x	x	x	x	x	x	Bus-side2 UV
x	x	**1**	x	x	x	x	x	Bus-side3 UV
x	x	x	**1**	x	x	x	x	Bus-side4 UV
x	x	x	x	**1**	x	x	x	Bus-side1 OV
x	x	x	x	x	**1**	x	x	Bus-side2 OV
x	x	x	x	x	x	**1**	x	Bus-side3 OV
x	x	x	x	x	x	x	**1**	Bus-side4 OV

2049 Table15 1.0

SR1E								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
VO1-UV1	**VO2-UV1**	**VO3-UV1**	**VO4-UV1**	**VO1-UV2**	**VO2-UV2**	**VO3-UV2**	**VO4-UV2**	
1	x	x	x	x	x	x	x	Card-side1 UV1
x	**1**	x	x	x	x	x	x	Card-side2 UV1
x	x	**1**	x	x	x	x	x	Card-side3 UV1
x	x	x	**1**	x	x	x	x	Card-side4 UV1
x	x	x	x	**1**	x	x	x	Card-side1 UV2
x	x	x	x	x	**1**	x	x	Card-side2 UV2
x	x	x	x	x	x	**1**	x	Card-side3 UV2
x	x	x	x	x	x	x	**1**	Card-side4 UV2

2049 Table16 1.0

SR1F								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
TRK1	**TRK2**	**TRK3**	**TRK4**	**OC1**	**OC2**	**OC3**	**OC4**	
1	x	x	x	x	x	x	x	TRAKKER error supply 1
x	**1**	x	x	x	x	x	x	TRAKKER error supply 2
x	x	**1**	x	x	x	x	x	TRAKKER error supply 3
x	x	x	**1**	x	x	x	x	TRAKKER error supply 4
x	x	x	x	**1**	x	x	x	Over-current supply 1
x	x	x	x	x	**1**	x	x	Over-current supply 2
x	x	x	x	x	x	**1**	x	Over-current supply 3
x	x	x	x	x	x	x	**1**	Over-current supply 4

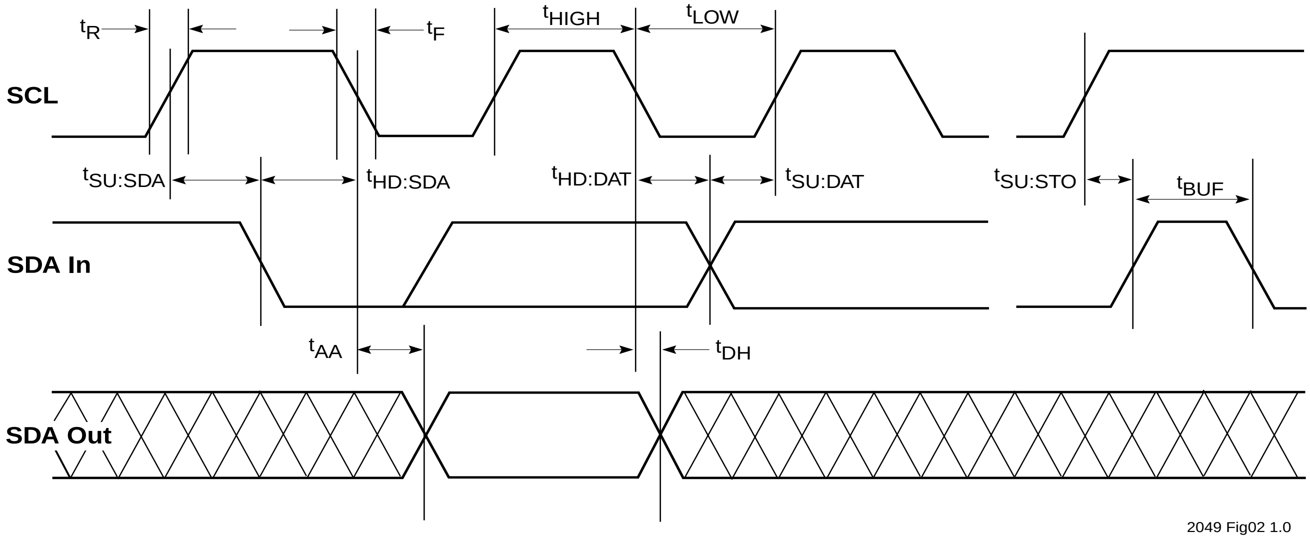
2049 Table17 1.0

AC OPERATING CHARACTERISTICS

Over recommended operating conditions

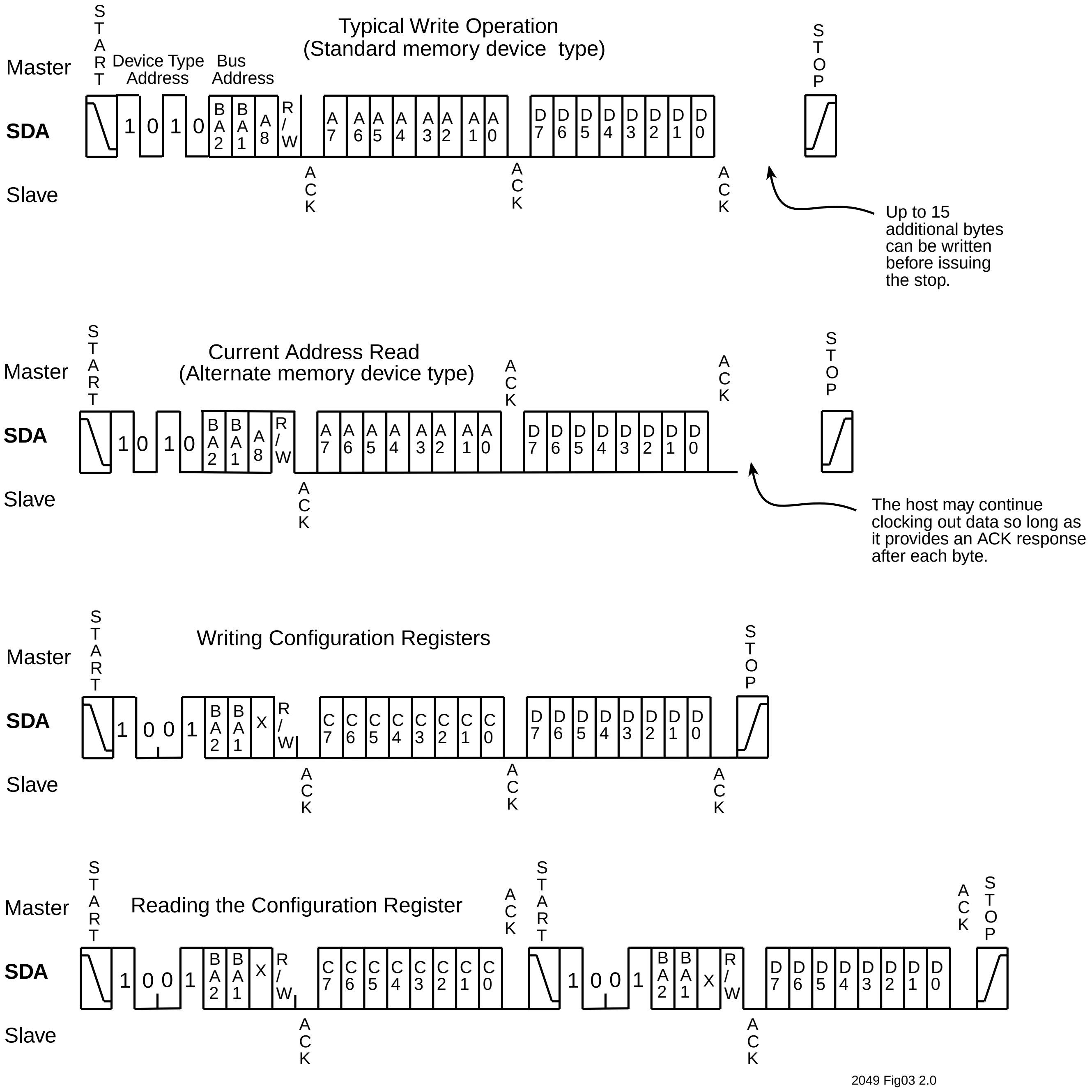
Symbol	Parameter	Conditions	Min.	Max.	Units
f_{SCL}	SCL clock frequency		0	100	kHz
t_{LOW}	Clock low period		4.7		µs
t_{HIGH}	Clock high period		4.0		µs
t_{BUF}	Bus free time	Before new transmission	4.7		µs
$t_{SU:STA}$	Start condition setup time		4.7		µs
$t_{HD:STA}$	Start condition hold time		4.0		µs
$t_{SU:STO}$	Stop condition setup time		4.7		µs
t_{AA}	Clock edge to valid output	SCL low to valid SDA (cycle n)	0.3	3.5	µs
t_{DH}	Data Out hold time	SCL low (cycle n+1) to SDA change	0.3		µs
t_R	SCL and SDA rise time			1000	ns
t_F	SCL and SDA fall time			300	ns
$t_{SU:DAT}$	Data In setup time		250		ns
$t_{HD:DAT}$	Data In hold time		0		ns
TI	Noise filter SCL and SDA	Noise suppression		100	ns
t_{WR}	Write cycle time			5	ms

2049 Table18 2.0



2049 Fig02 1.0

Figure 2. Memory Operating Characteristics



Typical Write Operation
(Standard memory device type)

Up to 15 additional bytes can be written before issuing the stop.

Current Address Read
(Alternate memory device type)

The host may continue clocking out data so long as it provides an ACK response after each byte.

Writing Configuration Registers

Reading the Configuration Register

Figure 3. Read and Write Operations

MEMORY AND REGISTER OPERATION

The ***TRAKKER*** has a nonvolatile memory that is configured as a 256 x 8 array. Configuration Registers reside in another ‘device type’ address space.

All read and write operations to both ‘device type’ spaces are handled via an industry standard two-wire interface. The bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus

Data Protocol

The protocol defines any device that sends data onto the bus as a “transmitter” and any device that receives data as a “receiver.” The device controlling data transmission is called the “master” and the controlled device is called the “slave.” The ***TRAKKER*** will always be a “slave” device since it never initiates a data transfer.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock high time, because changes on the data line while SCL is high will be interpreted as start or stop condition.

START and STOP Conditions

When both the data and clock lines are high, the bus is said to be not busy. A high-to-low transition on the data line, while the clock is high, is defined as the “START” condition. A low-to- high transition on the data line while the clock is high is defined as the “STOP” condition.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line low to ACKnowledge that it received the eight bits of data.

The ***TRAKKER*** will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected the ***TRAKKER*** will respond with an ACKnowledge after the receipt of each subsequent 8-bit word. In the READ mode the ***TRAKKER*** transmits eight bits of data, releases the SDA line, and then monitors the line for an ACKnowledge signal. If an ACKnowledge is detected, and no STOP condition is generated by the master, the ***TRAKKER*** will continue to transmit data. If an ACKnowledge is not detected the ***TRAKKER*** will terminate further data transmissions and await a STOP condition before returning to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see the following Table). The next three bits are the physical device address.

Read/Write Bit

The last bit of the data stream defines the operation to be performed. When set to “1,” a read operation is selected; when set to “0,” a write operation.

MEMORY WRITE OPERATIONS

The ***TRAKKER*** allows two types of write operations: byte-write and page write. A byte-write operation writes a single byte during the nonvolatile write period (tWR). The page write operation allows up to 16 bytes in the same page to be written during t_{WR}.

Byte Write

After the slave address is sent (to identify both the slave device and a read or write operation), a second byte is transmitted which contains the 8-bit address of any one of the 256 words in the array. Upon receipt of the word address the ***TRAKKER*** responds with an ACKnowledge. After receiving the next byte of data it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the ***TRAKKER*** begins the internal write cycle. While the internal write cycle is in progress the ***TRAKKER*** inputs are disabled, and the device will not respond to any requests from the master.

Device Type				Bus Address			R / W	Action
D7	D6	D5	D4	D3	D2	D1	D0	
1	0	1	0	A2	A1	A0	1 / 0	Memory device-type address
1	0	1	1					Alternate memory device-type address
1	0	0	1					Configuration registers device-type address

2049 Table19 1.0

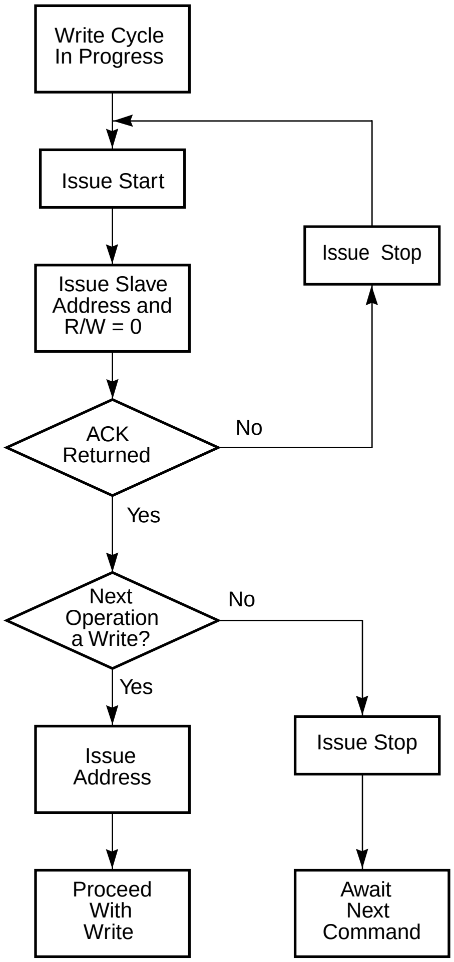
Page Write

The ***TRAKKER*** is capable of a 16-byte page-write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word the master can transmit up to 15 more bytes of data. After the receipt of each byte the ***TRAKKER*** will respond with an ACKnowledge.

The ***TRAKKER*** automatically increments the address for subsequent data words. After the receipt of each word, the low order address bits are internally incremented by one. The high order bits of the address byte remain constant. Should the master transmit more than 16 bytes, prior to generating the STOP condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 3 for the address, ACKnowledge and data transfer sequence.

Acknowledge Polling

When the ***TRAKKER*** is performing an internal WRITE operation it will ignore any new START conditions. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete. See the flow diagram for the proper sequence of operations for polling.



2049 Flow01 1.0

Flow Chart

READ OPERATIONS

Read operations are initiated with the R/W bit of the identification field set to "1." There are two different read options:

1. Current Address Byte Read
2. Random Address Byte Read

Current Address Read

The ***TRAKKER*** contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address location n, the next read operation would access data from address location n+1 and increment the current address pointer. When the ***TRAKKER*** receives the slave address field with the R/W bit set to "1" it issues an acknowledge and transmits the 8-bit word stored at address location n+1. The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point the ***TRAKKER*** discontinues data transmission.

Random Address Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE), followed by the address of the word it is to read. This procedure sets the internal address counter of the ***TRAKKER*** to the desired address. After the word address acknowledge is received by the it the master immediately reissues a start condition followed by another slave address field with the R/W bit set to READ. The ***TRAKKER*** will respond with an acknowledge and then transmit the 8 data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The ***TRAKKER*** discontinues data transmission and reverts to its standby power mode.

Sequential READ

Sequential reads can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ). However, the master now responds with an ACKnowledge, indicating that it requires additional data from the ***TRAKKER***. The ***TRAKKER*** continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP condition. During a sequential read operation the internal address counter is automatically incremented with each ACKnowledge signal. For read operations all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address the address counter will 'roll-over' and the memory will continue to output data.

APPLICATION CIRCUIT

See Figure 4. A typical circuit soft starting the 5V supply and TRAKKING the 3.3V, 2.5V and 1.8V supplies

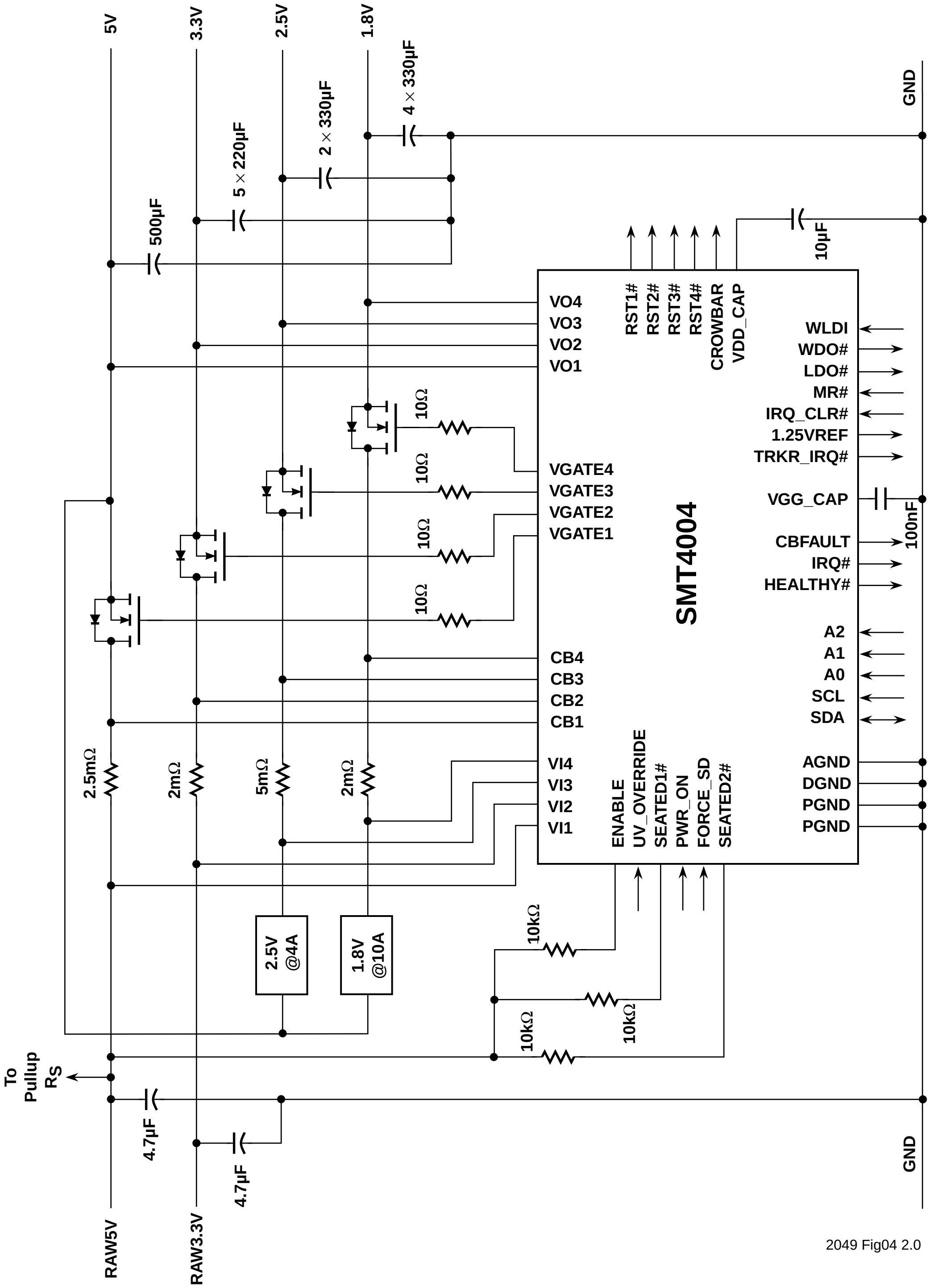


Figure 4. Application Circuit

ORDERING INFORMATION

SMT4004 F

Base Part Number

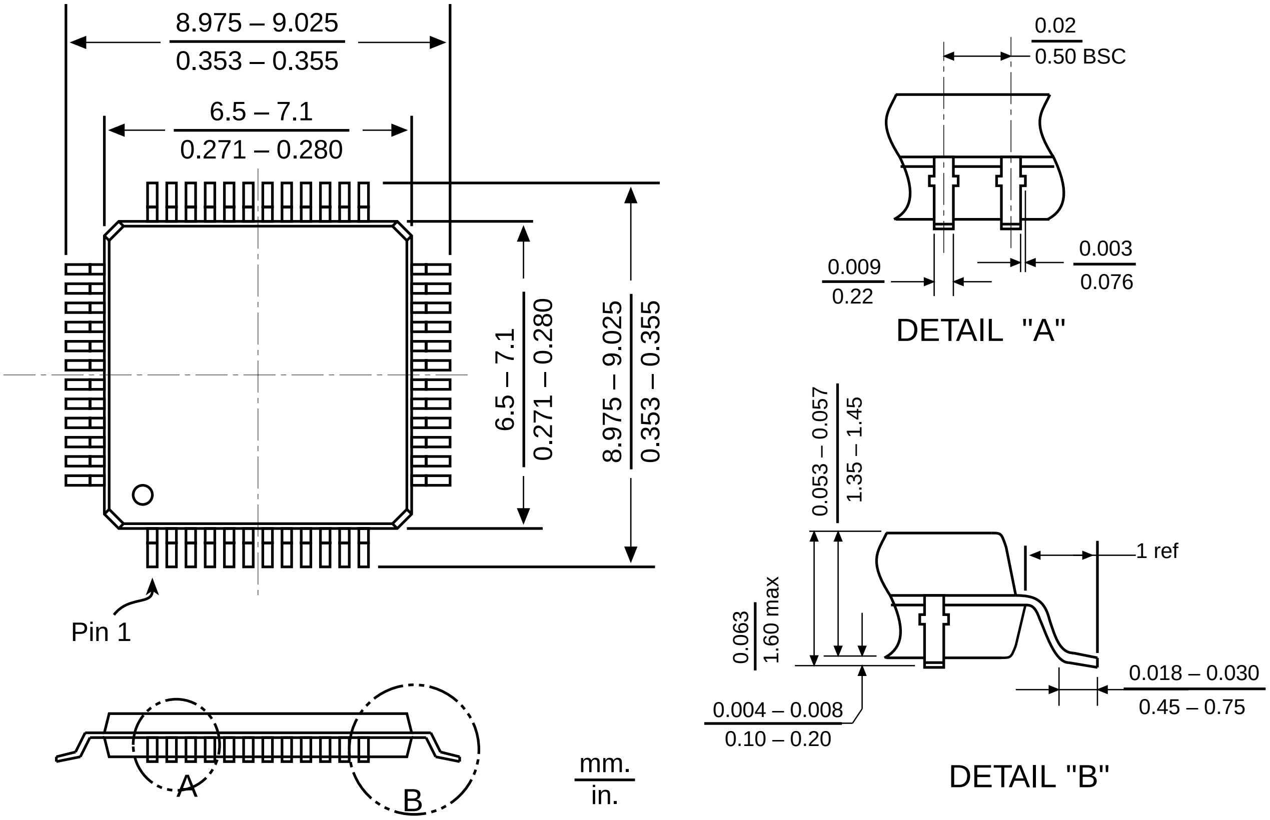
Package
F = 48 Pin TQFP

Register	Hex Contents	Configured as:
R0	B4	VO Threshold of 4.5V
R1	69	V1 Threshold of 3.OV
R2	41	V2 threshold of 2.2V
R3	28	V3 Threshold of 1.7V
R4	60	V0 UV and OV enabled OV set to 5.5V
R5	60	V1 UV and OV enabled OV set at 3.6V
R6	62	V2 UV and OV enabled OV set at 2.8V
R7	67	V3 UV and OV enabled OV set at 2.5V
R8	B9	Card Side VO Threshold of 4.6V
R9	6E	Card Side V 1 Threshold of 3.1 V
RA	46	Card Side V2 threshold of 2.3V
RB	2D	Card Side V3 Threshold of 1.8V
RC	A2	Card Side VO Threshold 2 of 4.5V
RD	A3	Card Side V 1 Threshold 2 of 3.OV
RE	A4	Card Side V2 threshold 2 of 2.2V
RF	A6	Card Side V3 Threshold 2 of 1.7V
R10	05	Responds to pin biased addresses, 1010$_{BIN}$, 250V/s slew rate on and off
R11	FF	Enable all RESET sources
R12	FF	Enable all RESET and IRQ sources
R13	FF	Enable all IRQ sources
R14	FF	Enable all IRQ sources
R15	EF	800 ms POR to IRQ delay, enable all sources
R19	81	Enable Crowbar on manual input and Quicktrip only
R1A	AA	Enable 100mV Quicktrip all manager circuits
RIB	02	All outputs active low, over current delay 100µs
RIC	F6	Reset 200ms, Longdog 3200ms, Watchdog 1600ms

2049 Reg Table 1.0

PACKAGE

48 PIN TQFP PACKAGE



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