OKI Semiconductor

MSM51C256A

262,144-Word × 1-Bit DYNAMIC RAM

DESCRIPTION

The MSM51C256A is a new generation dynamic RAM organized as 262,144-word × 1-bit. The technology used to fabricate the MSM51C256A is OKI's COMS silicon gate process technology. The device operates at a single 5V power supply. Its I/O pins are TTL compatible.

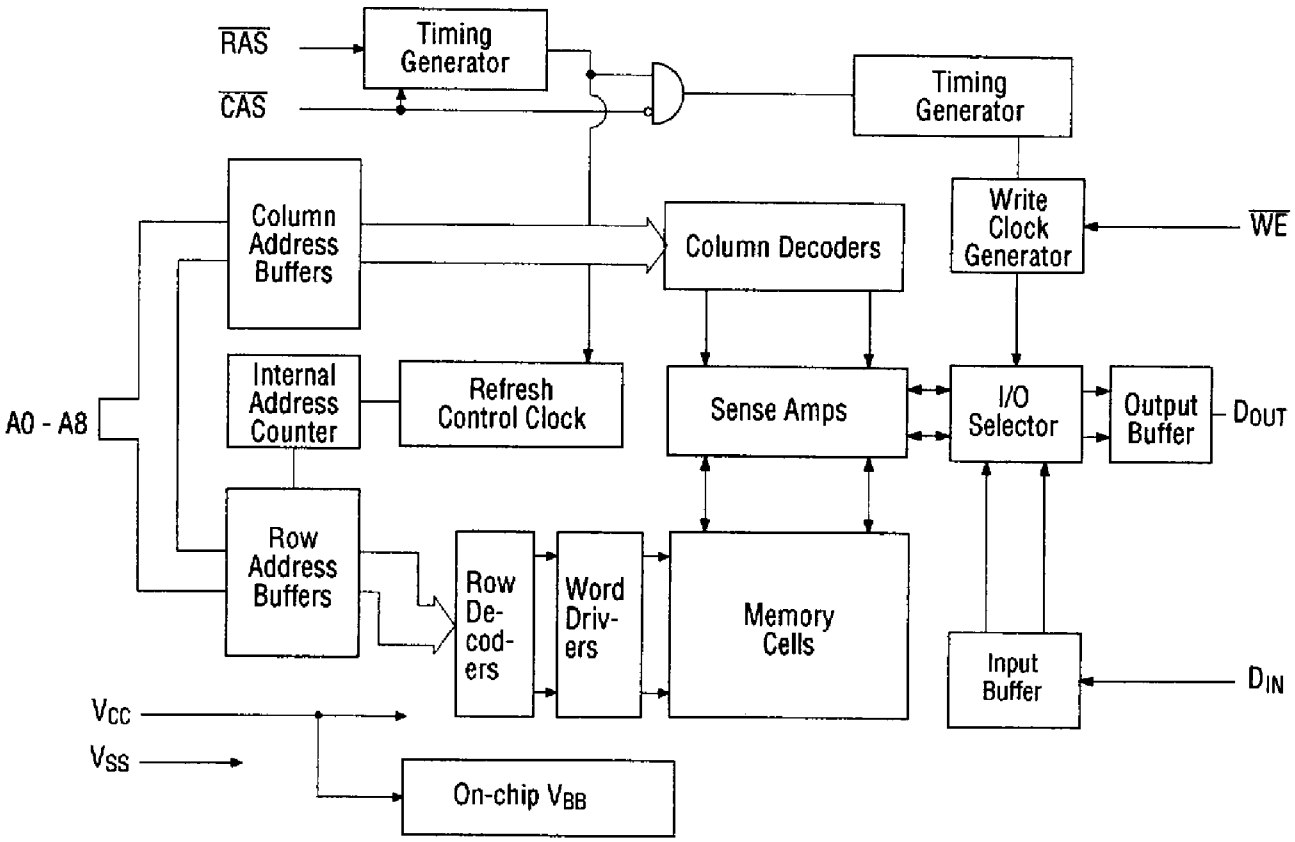
FEATURES

- Silicon gate, triple polysilicon CMOS, 1-transistor memory cell
- 262,144-word × 1-bit organization
- Single 5V power supply ±10% tolerance
- Input: TTL compatible
- Output: TTL compatible, tristate
- Refresh: 256 cycles/4ms
- Common I/O capability using Early Write operation
- Fast page mode, read modify write capability
- $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh, $\overline{RAS}$-only refresh capability
- Package:
  16-Pin 300mil Plastic DIP (DIP16-P-300)
  18-Pin 290mil Plastic QFJ (QFJ18-P-R290 JEDEC AB Type)

PRODUCT FAMILY

Family	Access Time (Max.)			Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}		Operating (Max.)	Standby (Max.)
MSM51C256A-70	70ns	35ns	20ns	140ns	357.5mW	11mW
MSM51C256A-80	80ns	40ns	20ns	160ns	302.5mW	
MSM51C256A-10	100ns	50ns	25ns	190ns	247.5mW	

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D*	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	−55 to 150	°C

*: Ta = 25°C

Recommended Operating Conditions

(Ta = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

Capacitance

(V_{CC} = 5V ±10%, Ta = 25°C, f = 1MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A8, D_{IN})	C_{IN1}	—	4	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	—	5	pF
Output Capacitance (D_{OUT})	C_{OUT}	—	6	pF

DC Characteristics

(V_{CC} = 5V ± 10%, Ta = 0 to 70°C)

Parameter	Symbol	Condition	MSM 51C256A-70		MSM 51C256A-80		MSM 51C256A-10		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH} = –5.0mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 4.2mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	0V ≤ V_I ≤ 6.5V; All other pins not under test = 0V	–10	10	–10	10	–10	10	µA	
Output Leakage Current	I_{LO}	D_{OUT} disable 0V ≤ V_O ≤ 5.5V	–10	10	–10	10	–10	10	µA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = Min.	—	65	—	55	—	45	mA	1
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	—	3	—	3	—	3	mA	1
		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} –0.2V	—	2	—	2	—	2	mA	1
Average Power Supply Current ($\overline{RAS}$-only Refresh)	I_{CC3}	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH} t_{RC} = Min.	—	65	—	55	—	45	mA	1, 2
Average Power Supply Current ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$ refresh	—	65	—	55	—	45	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$ = V_{IL} $\overline{CAS}$ cycling, t_{PC} = Min.	—	60	—	50	—	40	mA	1, 3

Notes: 1. Specified values are obtained with the output open.
2. Address can be changed less than one time while $\overline{RAS}$ = V_{IL}.
3. Address can be changed less than one time while $\overline{CAS}$ = V_{IH}.

AC Characteristics (1/2)

(V_{CC} = 5V ± 10%, Ta = 0 to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM 51C256A-70		MSM 51C256A-80		MSM 51C256A-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	
Random Read or Write Cycle Time	t_{RC}	140	—	160	—	190	—	ns	
Read Modify Write Cycle Time	t_{RMW}	165	—	185	—	220	—	ns	
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t_{PRMW}	70	—	75	—	85	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	4, 5, 6
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	4, 5
Access Time from Column Address	t_{AA}	—	35	—	40	—	50	ns	4, 6
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	40	—	45	—	50	ns	4
Output Low Impedance from $\overline{CAS}$	t_{CLZ}	0	—	0	—	0	—	ns	
Output Buffer Turn-off Delay	t_{OFF}	0	20	0	20	0	20	ns	7
Transition Time	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	—	70	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode Cycle Only)	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{CAS}$ Pulse Width (Fast Page Mode Cycle Only)	t_{CP}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	22	60	25	75	ns	5
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	35	17	40	20	50	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	12	—	15	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	ns	
Column Address Hold Time from $\overline{RAS}$	t_{AR}	55	—	60	—	75	—	ns	
Column Address to RAS Lead Time	t_{RAL}	35	—	40	—	50	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	8
Write Command Hold Time from $\overline{RAS}$	t_{WCR}	55	—	60	—	75	—	ns	
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	9
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	20	—	ns	
Write Command to RAS Lead Time	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to CAS Lead Time	t_{CWL}	20	—	20	—	25	—	ns	

AC Characteristics (2/2)

(V_{CC} = 5V ± 10%, Ta = 0 to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM 51C256A-70		MSM 51C256A-80		MSM 51C256A-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	ns	10
Data-in Hold Time from $\overline{RAS}$	t_{DHR}	55	—	60	—	75	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	20	—	20	—	25	—	ns	9
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	35	—	80	—	100	—	ns	9
Column address to $\overline{WE}$ Delay Time	t_{AWD}	10	—	40	—	50	—	ns	9
Read Command Hold Time Reference to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	8
$\overline{RAS}$ to $\overline{CAS}$ Set-up Time ($\overline{CAS}$ Before $\overline{RAS}$)	t_{CSR}	30	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$)	t_{CHR}	10	—	30	—	30	—	ns	
$\overline{CAS}$ Active Delay from $\overline{RAS}$ Precharge	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time (Refresh Counter Test)	t_{CPT}	40	—	40	—	50	—	ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	10	—	10	—	15	—	ns	

Notes:

1. An initial pause of 100μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$-only refresh) before proper device operation is achieved.

2. The AC characteristics assume t_T = 5ns.

3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels of input signals for timing measurement. Ttransition times (t_T) are measured between V_{IH} and V_{IL}.

4. Measured with a load circuit equivalent to 2TTL loads and 100pF.

5. Operating within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.

6. Operating within the t_{RAD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then access time is controlled exclusively by t_{AA}.

7. t_{OFF} (Max.) defines the time at which the output achives the open circuit condition and is not referenced to output voltage levels.

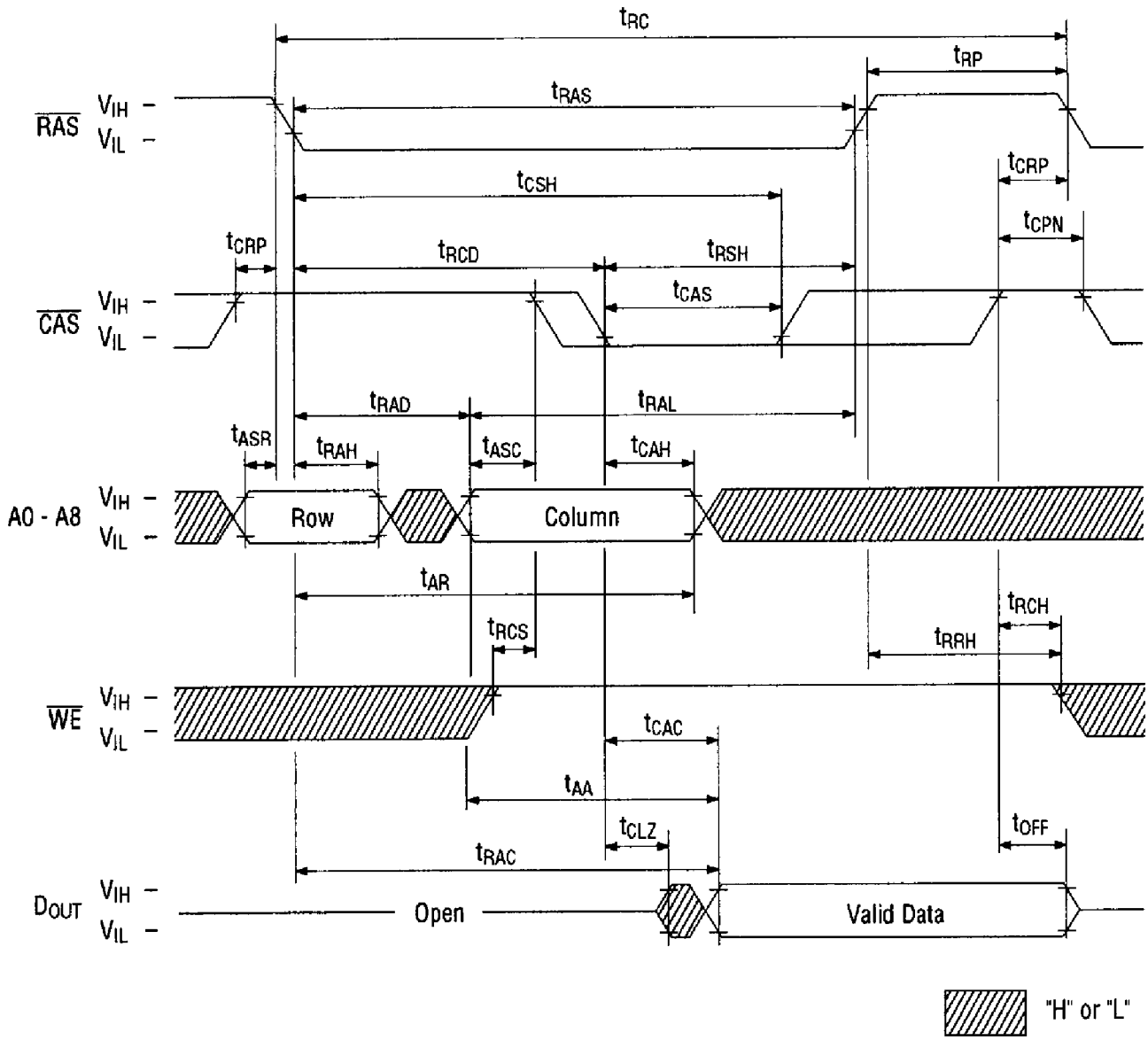
8. Either t_{RRH} and t_{RCH} must be satisfied for a read cycle.

9. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (Min.) the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$ (Min.) and $t_{AWD} \geq t_{AWD}$ (Min.), the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

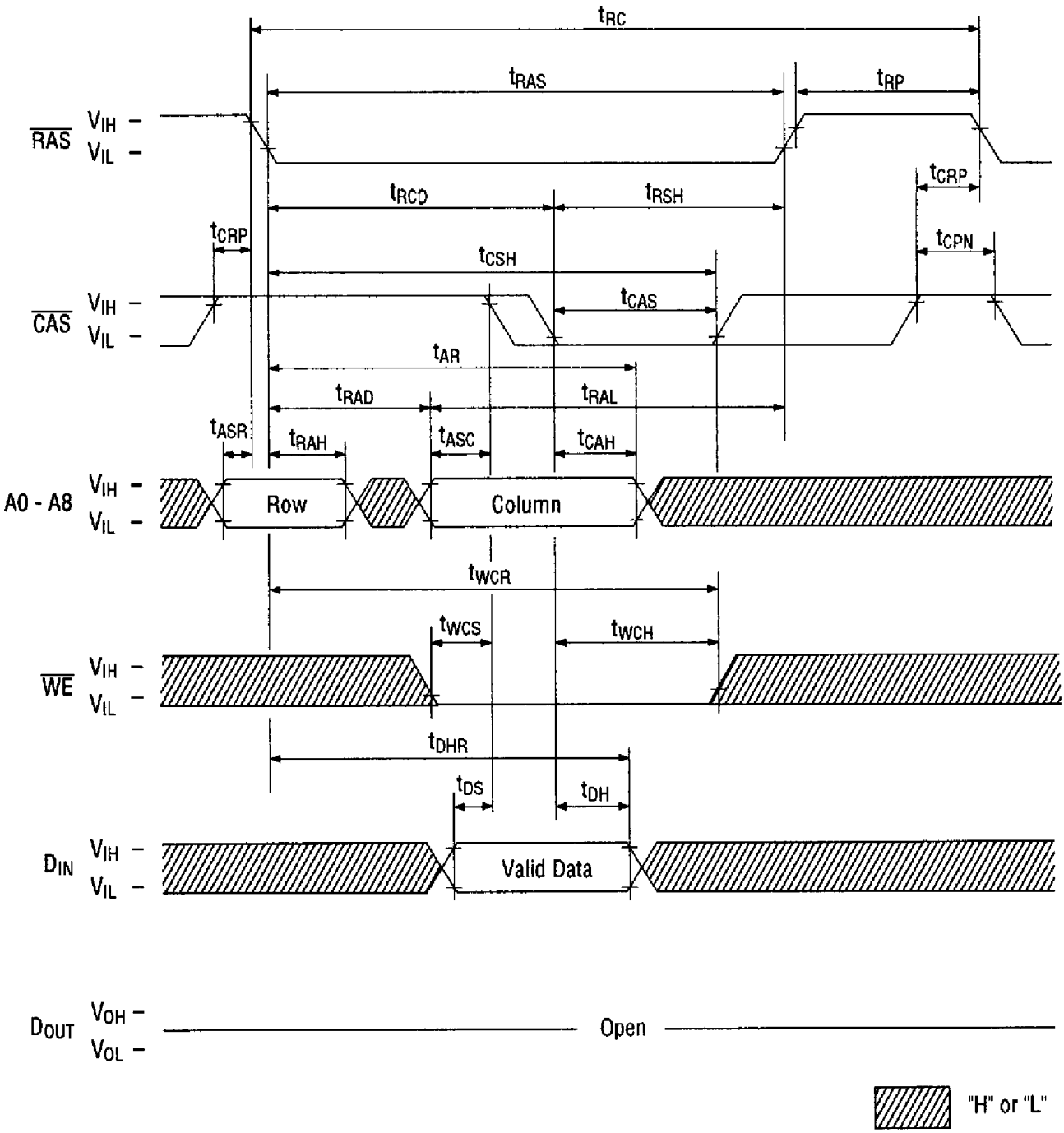
10. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.

TIMING WAVEFORM

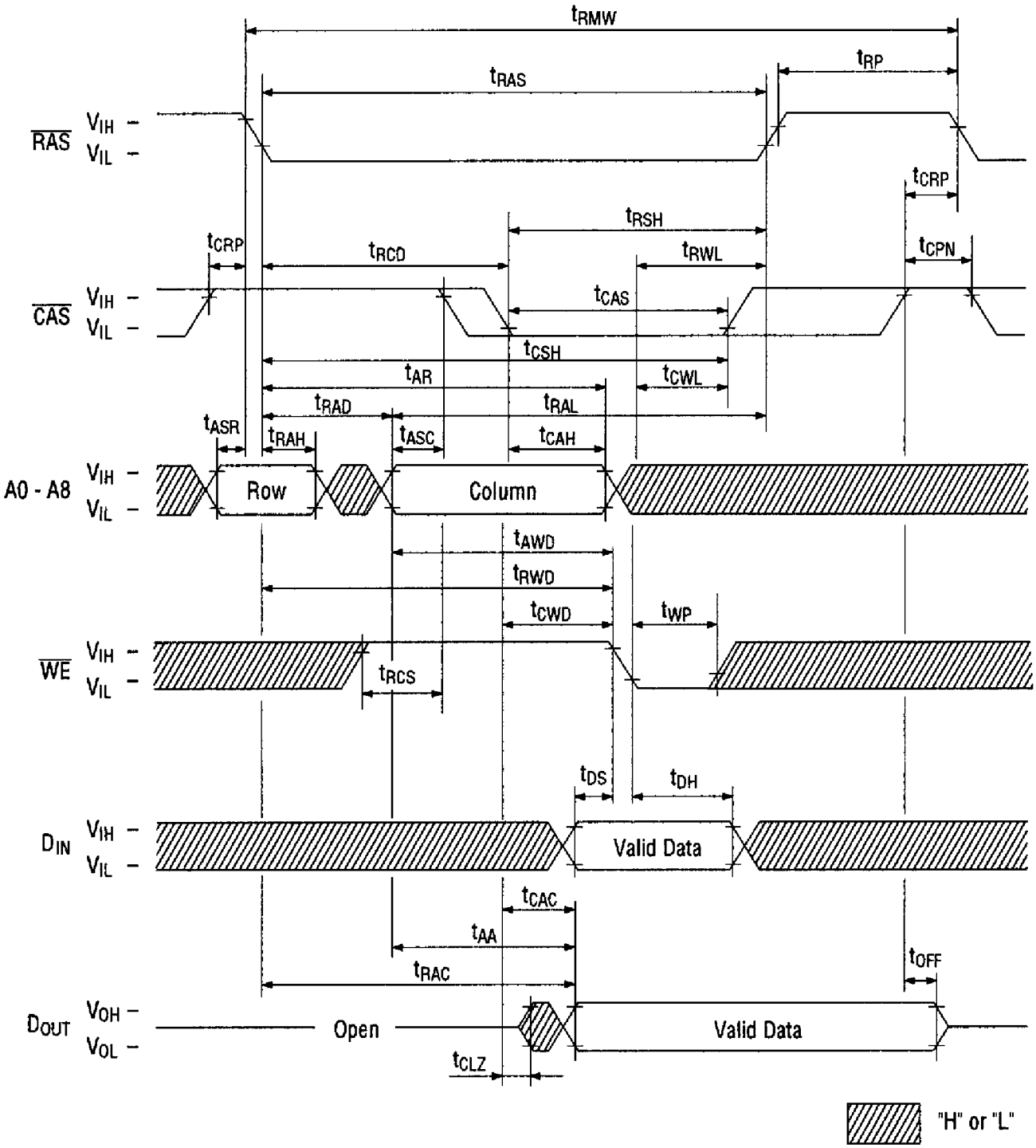
Read Cycle



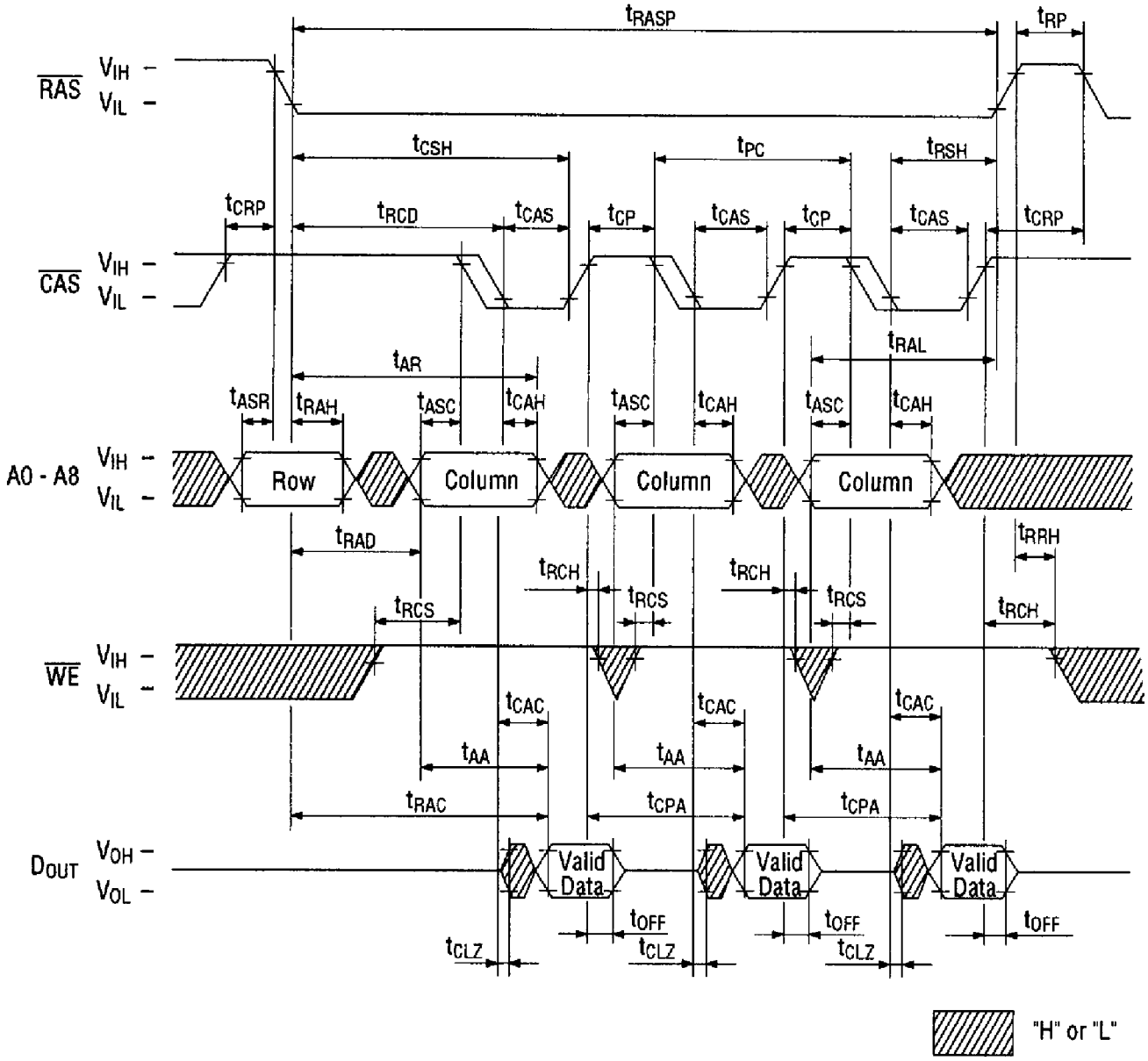
Write Cycle (Early Write)



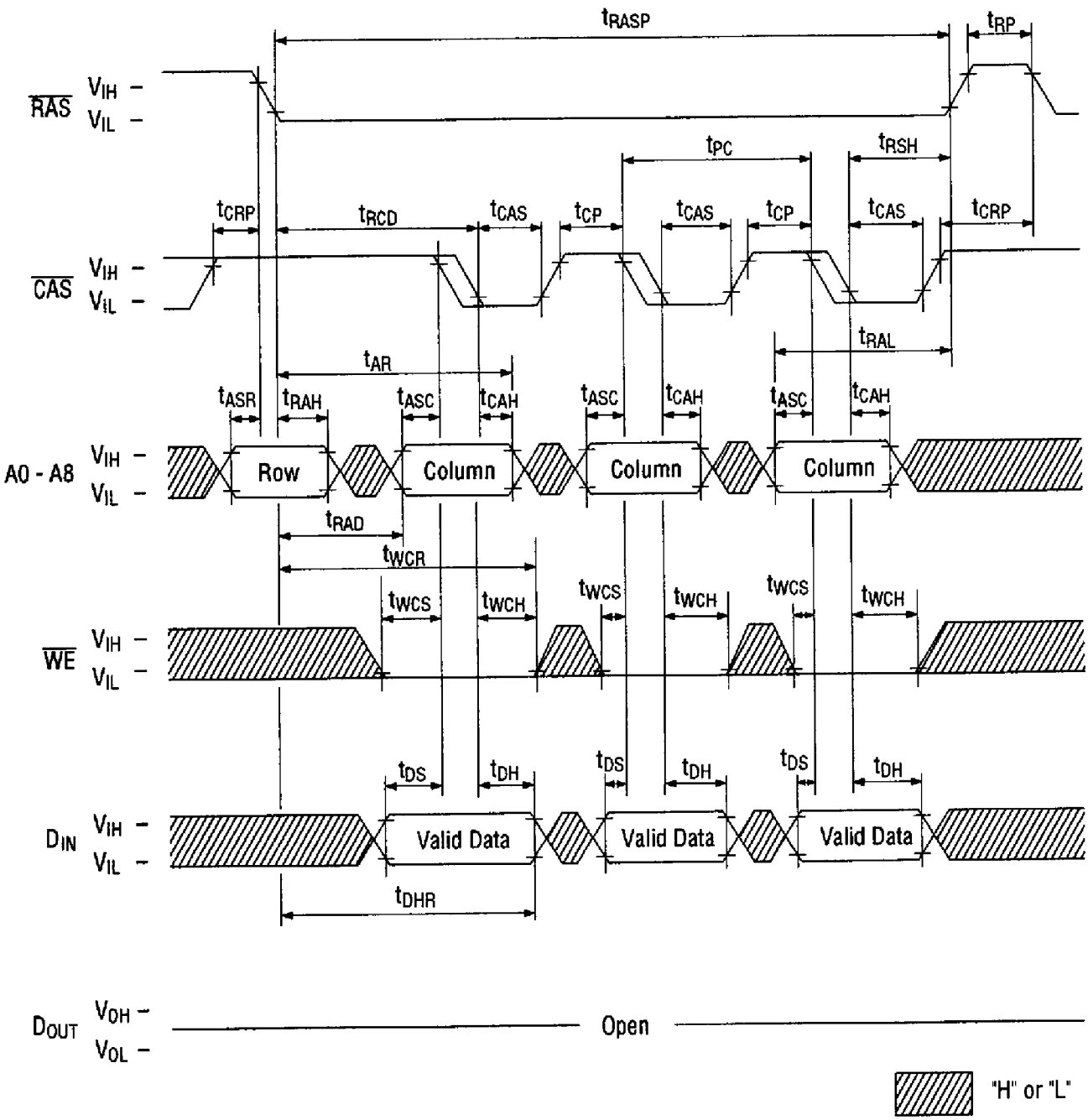
Read Modify Write Cycle



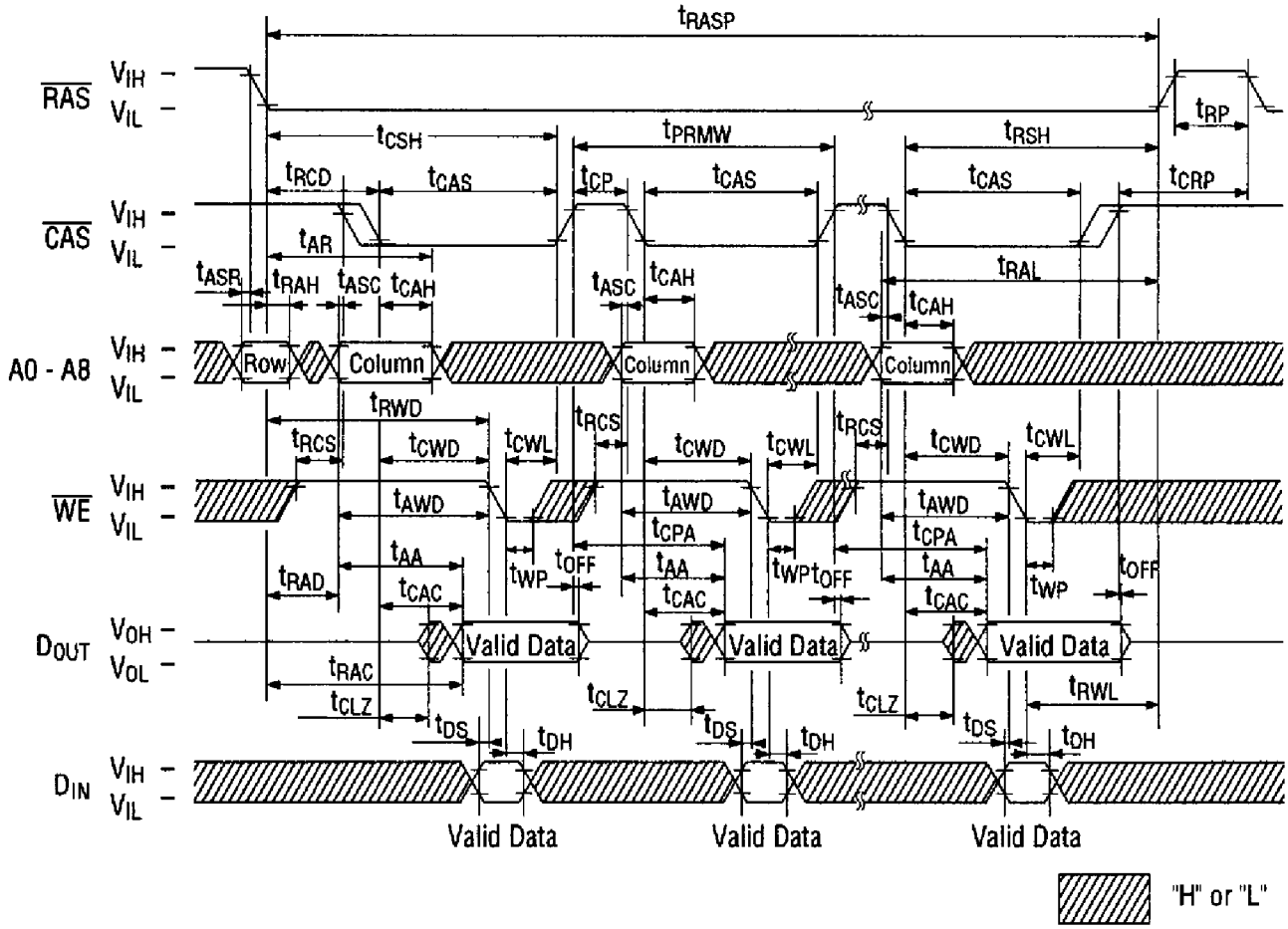
Fast Page Mode Read Cycle



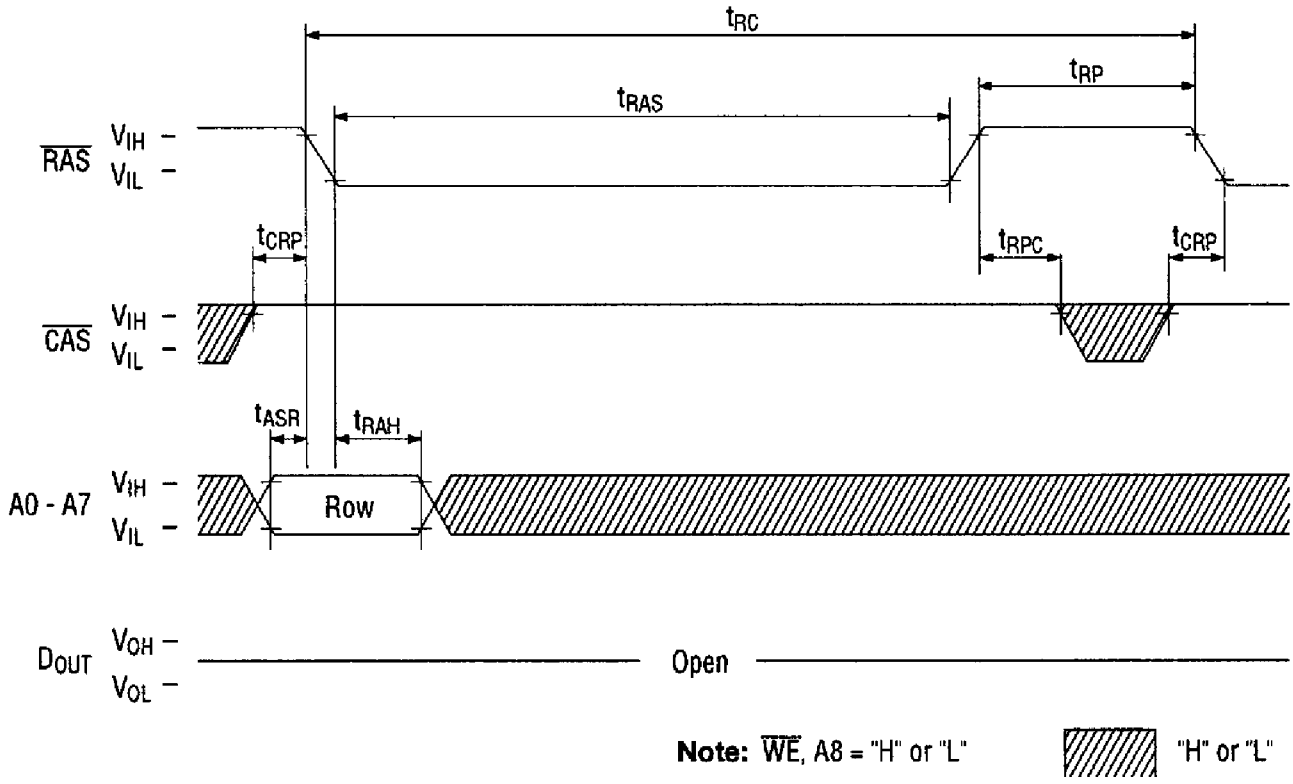
Fast Page Mode Write Cycle (Early Write)



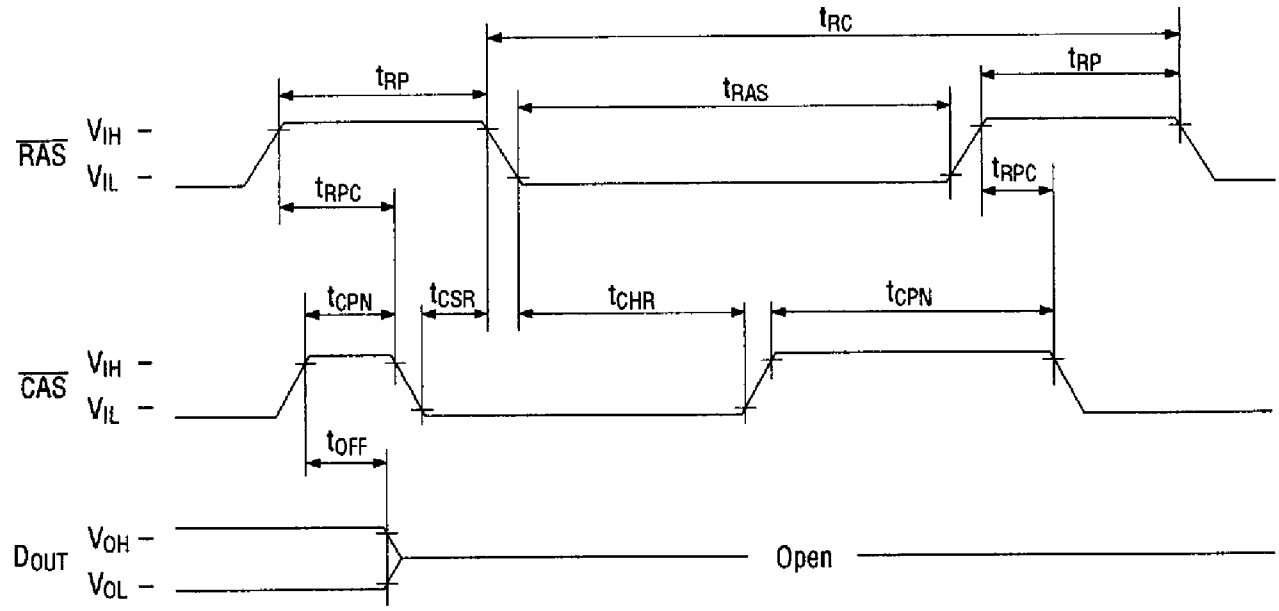
Fast Page Mode Read Modify Write Cycle



RAS-only Refresh Cycle

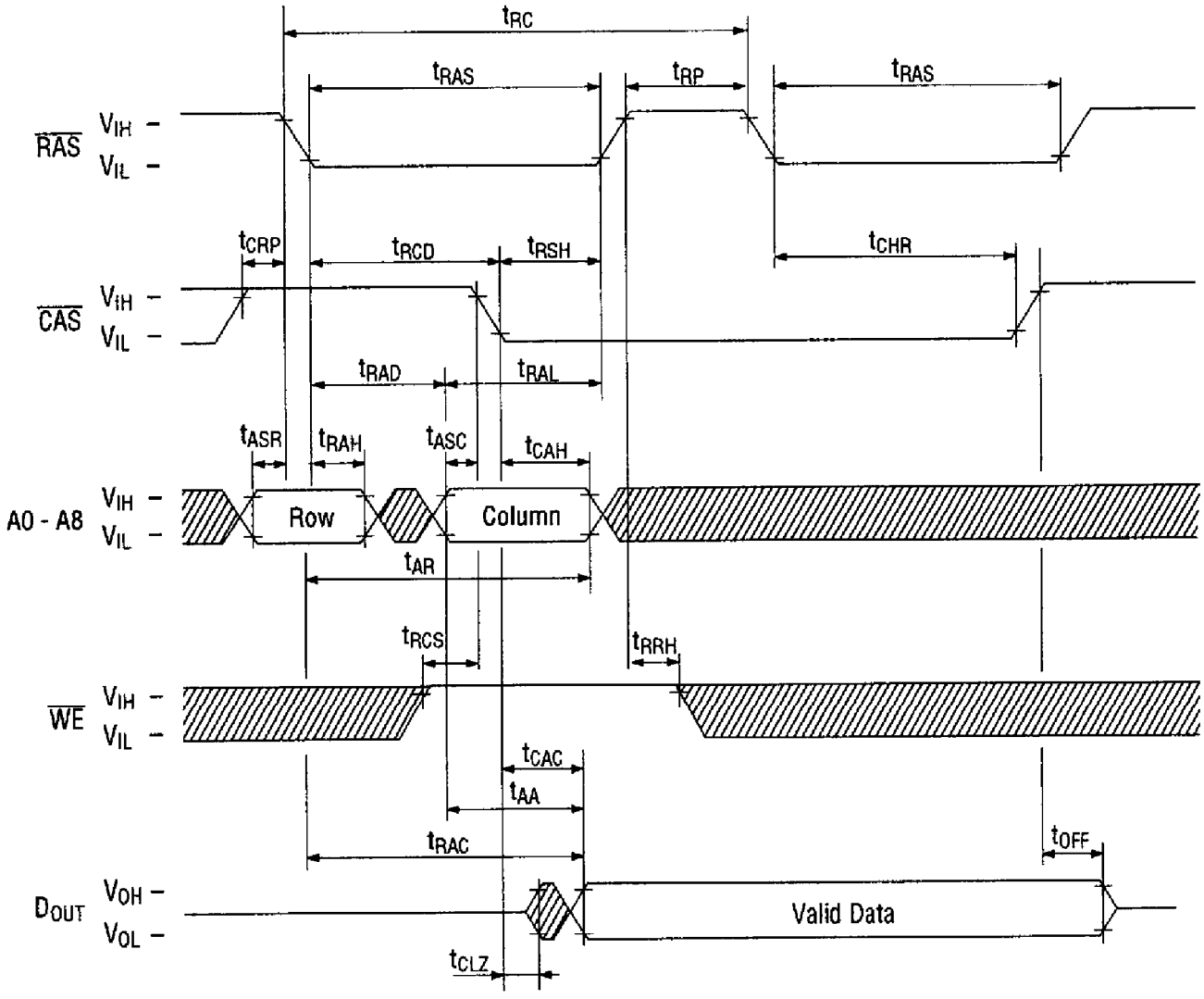


$\overline{CAS}$ Before $\overline{RAS}$ Auto-refresh Cycle



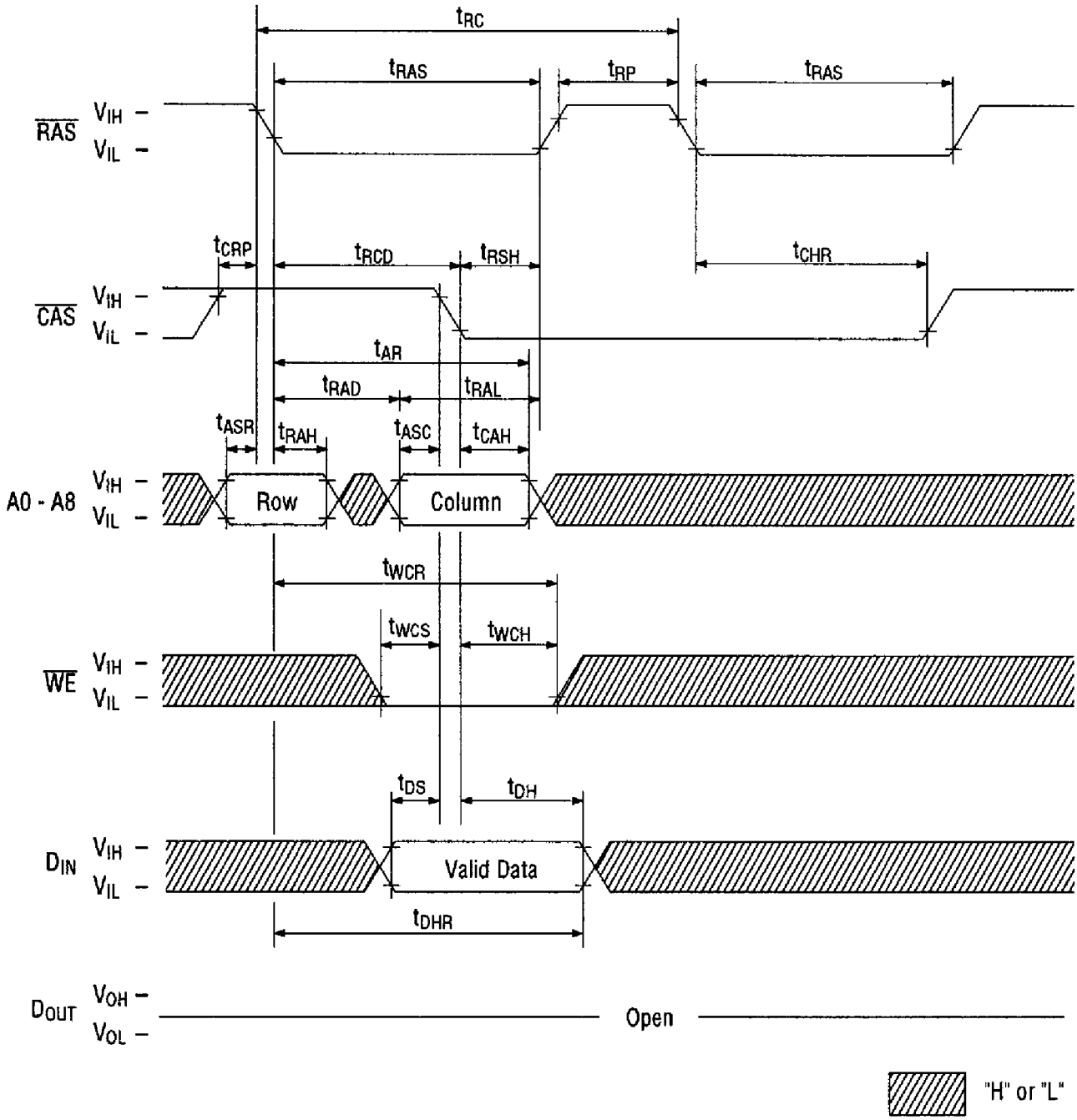
Note: $\overline{WE}$, A0 - A8 = "H" or "L" "H" or "L"

Hidden Refresh Read Cycle



"H" or "L"

Hidden Refresh Write Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle