M56768SP/FP

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VCR

DESCRIPTION

The M56768SP/FP is a semiconductor integrated circuit, an oxide-film separated ECL/I²L PLL frequency synthesizer. The prescaler and PLL, with a maximum operating frequency of 1.0 GHz, are housed on a single chip.

FEATURES

- Built-in prescaler with input amplifier (fmax=1.0GHz)
- Low power dissipation (Icc=30mA at Vcc=5V)
- Fine tuning capability (62.50kHz/step)
- PLL lock/unlock status display output
- Serial data input (2 or 3 data transfer lines)

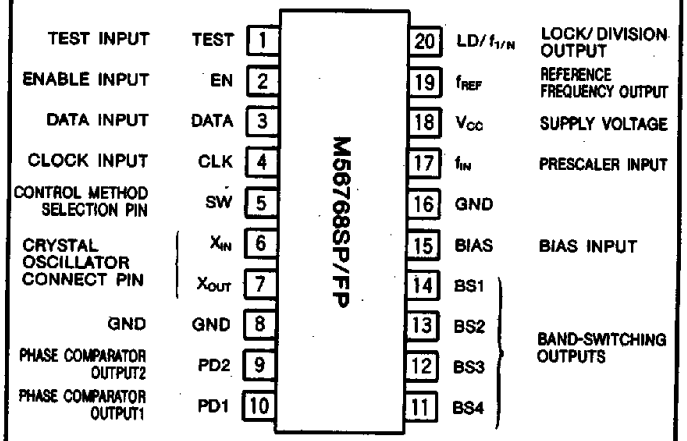
APPLICATION

TV and VCR tuners

RECOMMENDED OPERATING CONDITION

Supply voltage range.....4.5~5.5V
Operating frequency(1).....4MHz(Typ)
(Crystal oscillator circuit)
Operating frequency(2).....80~100MHz(f_{IN} input)
Output low-level current.....2mA(Max)(Pin ⑲.⑳)
Band output low-level current.....1mA(Max)(Pin ⑪.⑫.⑬.⑭)

PIN CONFIGURATION (TOP VIEW)

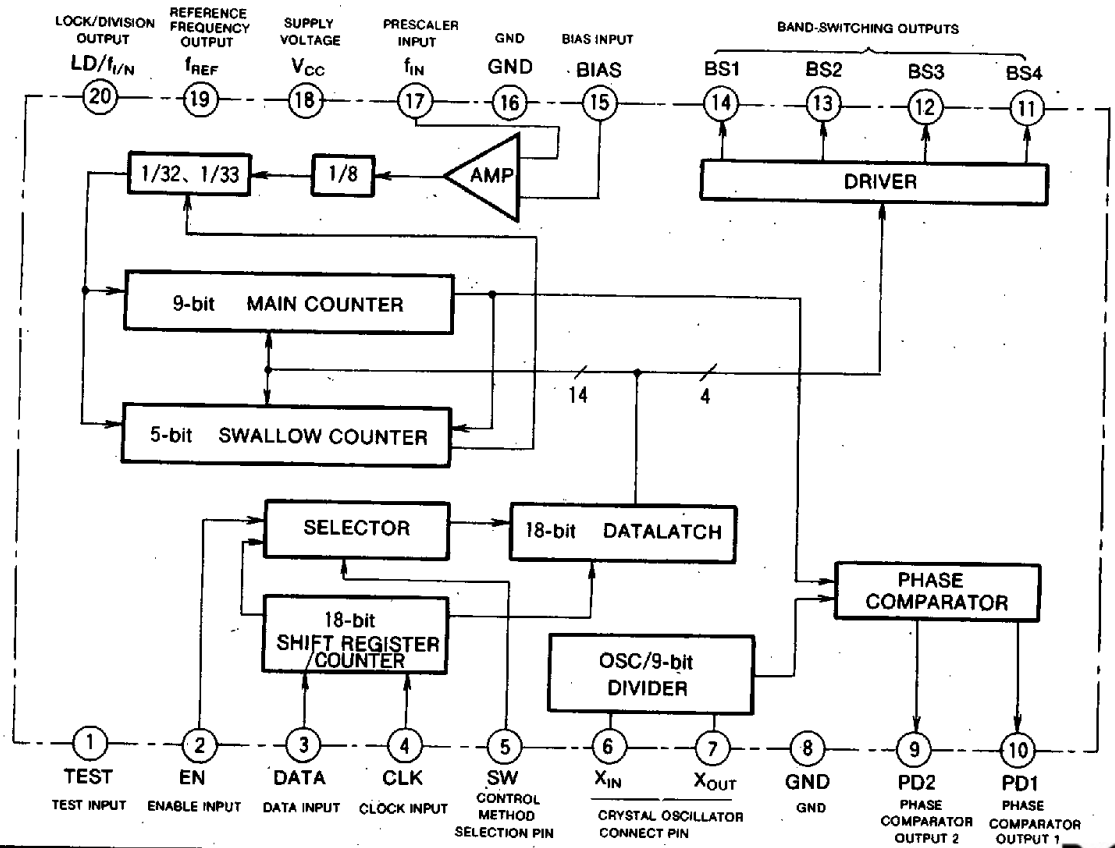


Outline 20P4B(SP)
20P2N-A(FP)

FUNCTION

The M56768SP/FP is a PLL frequency synthesizer IC for TVS and VCRS. The prescaler is realized in emitter-coupled logic, and the PLL in integrated injection logic. The maximum operating frequency of the prescaler is 1.0 GHz.The first stage is a fixed 1/8 prescaler, and the second stage is a 1/32 1/33 dual-modulus prescaler. The PLL consists of a 4MHz crystal oscillator, a 9-bit reference frequency divider, a programmable divider(a 9-bit M counter and a 5-bit S counter), a phase comparator, and a lock detector. Four band-switching circuits are also provided.

BLOCK DIAGRAM



SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VCR

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings		Unit
		Min.	Max.	
V_{CC}	supply voltage	−0.5	6.5	V
V_I	Input voltage	−0.5	6.5	V
V_{O1}	Output voltage (1) PD output	−0.5	5.5	V
V_{O2}	Output voltage (2) Other than above	−0.5	6.5	V
V_{BD}	Output withstanding voltage		13	V
Pd	Power dissipation		550	mW
Topr	Operating temperature	−20	75	℃
Tstg	Storage temperature	−40	125	℃

ELECTRICAL CHARACTERISTICS (Ta=25℃, V_{CC}=5.0V, unless otherwise noted)

Symbol	Parameter		Test pin	Test conditions	Limits			Unit
					Min.	Typ.	Max.	
V_{IH}	High-level input voltage		1, 2, 3, 4, 5		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		1, 2, 3, 4, 5				0.7	V
$I_{IH}1$	High-level input current 1		1, 3, 4, 5, 2	V_{CC}=5.5V, V_I=2.7V			50	μA
$I_{IL}1$	Low-level input current 1		1, 3, 4, 5, 2	V_{CC}=5.5V, V_I=0.4V		−100	−200	μA
V_{IC}	Input clamp voltage		1, 2, 3, 4,	V_{CC}=4.5V, I_{IC}=−1.0mA		−1.3	−1.8	V
V_{OL}	Low-level output voltage		19, 20	V_{CC}=4.5V, I_{OL}=2mA		0.3	0.5	V
$I_{OLK}1$	Output leak current	PD output	10	V_{CC}=5.5V, V_O=0.5~4.8V	−1.0		1.0	μA
$I_{OLK}2$		BS output	11~14	V_{CC}=4.5V, V_O=12V			10	μA
$I_{OLK}3$		Other than above	19, 20	V_{CC}=5.5V, V_O=5.5V			10	μA
I_{CC}	Supply current		18	V_{CC}=5.5V		30	55	mA

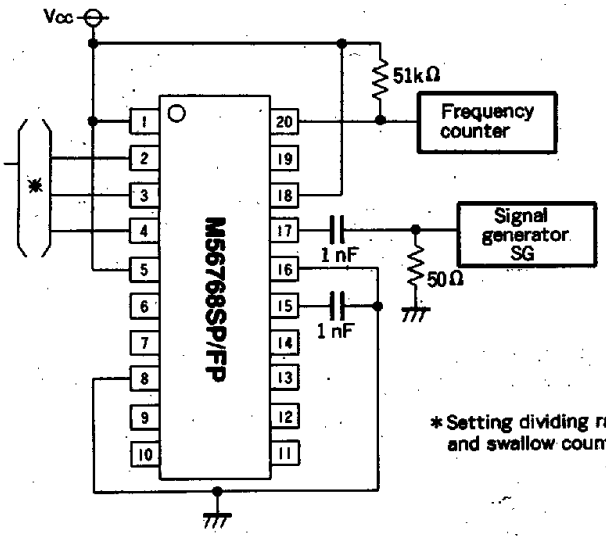
Typical values are at V_{CC}=5.0V, Ta=25℃.

SWITCHING CHARACTERISTICS

Symbol	Parameter	Test pin	Test conditions		Limits			Unit
					Min.	Typ.	Max.	
fopr	Prescaler Operating frequency	17	V_{CC}=4.5~5.5V V_{IN}=V_{IN}min~V_{IN}max		80		1000	MHz
V_{IN}	Operating input voltage	17	V_{CC}=4.5~5.5V	80~100MHz 100~1000MHz	−24 −27		4 4	dBm
t_{PWC}	Clock pulse width	4	V_{CC}=4.5~5.5V		1			μs
$t_{SU(D)}$	Data setup time	3			2			μs
$t_{H(D)}$	Data hold time	3			1			μs
$t_{SU(E)}$	Enable setup time	2			3			μs
$t_{H(E)}$	Enable hold time	2			3			μs
t_{INT}	Enable data internal time	2, 3			1			μs
tr	Rising time	2, 3, 4					1	μs
tf	Falling time	2, 3, 4					1	μs

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VCR

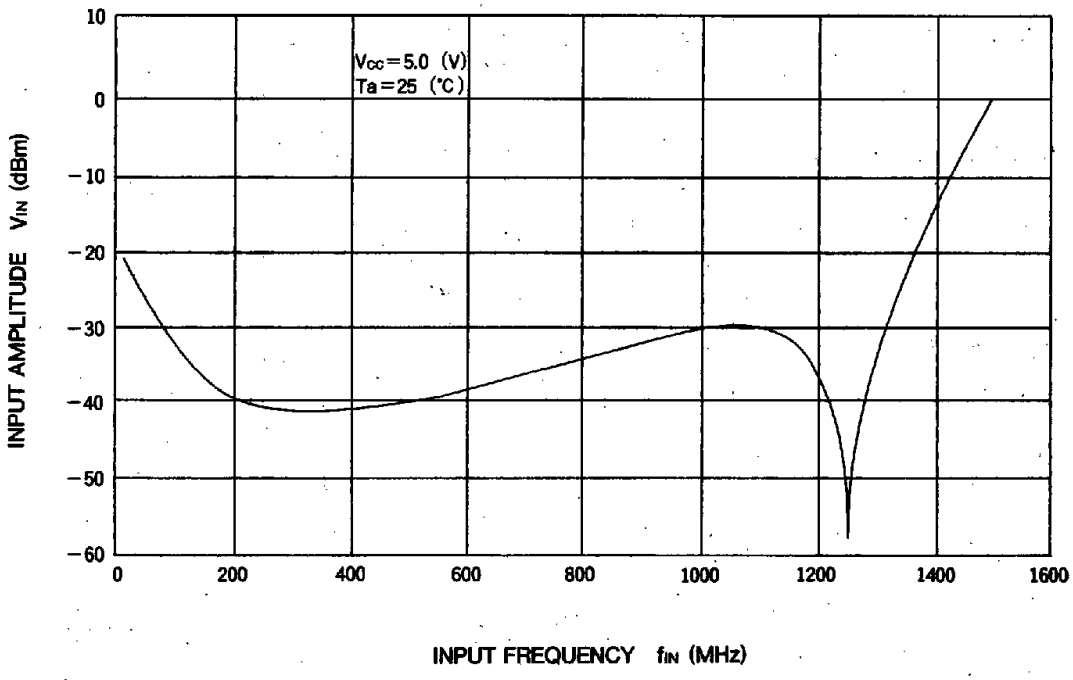
TEST CIRCUIT



Unit Resistance : Ω
Capacitance : F

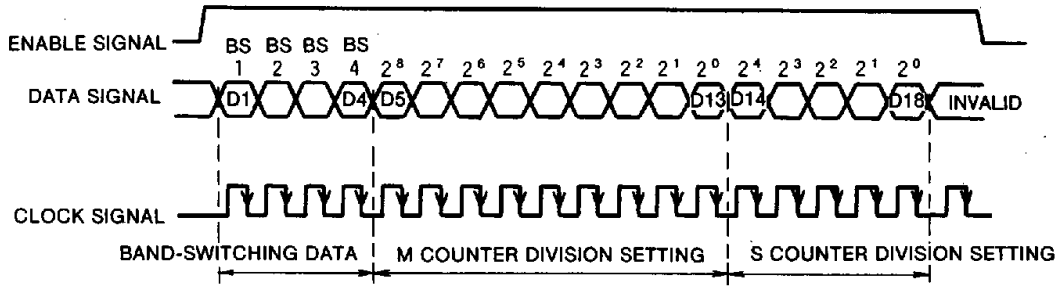
TYPICAL CHARACTERISTICS

INPUT AMPLITUDE VS INPUT FREQUENCY



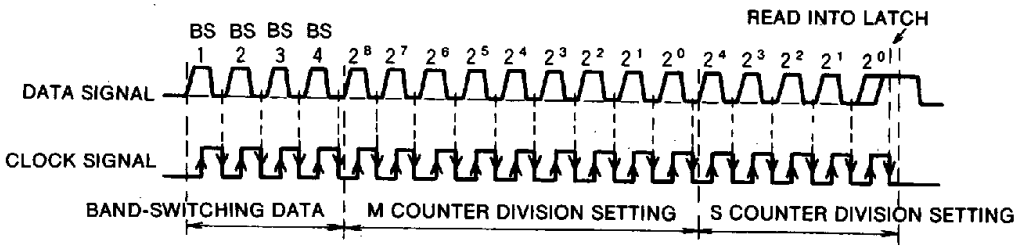
HOW TO SET THE DIVIDING RATIO OF THE PROGRAMMABLE DIVIDER AND BAND-SWITCHING OUTPUT

(1) When the control method selection pin SW is set to Vcc or OPEN, the division ratio of the programmable divider and band-switching output is set as shown below.
When set high, the data and clock signals are read, and the data is read into the latch at the falling edge of the 18th clock signal pulse. The clock signal then becomes invalid.



*Data is read when CLK drops from high to low.

(2) When the control methed selection pin SW is set to GND, the division ratio of the programmable divider and band-switching output is as shown below.



*Data is read when CLK rises from low to high. If data is high when CLK drops from high to low, content is transferred to latch circuit.

Total division N is given by the following formulas, in addition to the prescaler used in the previous stage.

$N=8(32M+S)$ M : 9-bit Main Counter Division
S : 5-bit Swallow Counter Division

The M and S counters are binary and the possible division ranges are as follows

$32 \leqq M \leqq 511$
$0 \leqq S \leqq 31$

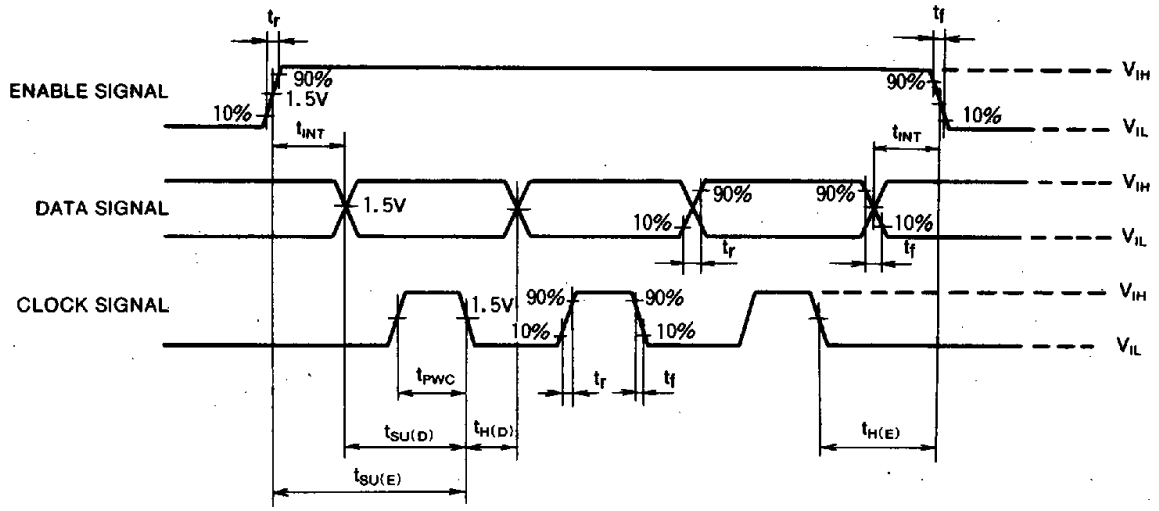
Therefore,the range of division N is 8,192~131,064.
The tuning freqrency fv.c.o. is given by the following expressions.

$$f_{V.C.O.}=f_{REF} \times N$$
$$=7.8125 \times 8 \cdot (32M+S)$$
$$=62.5(32M+S)[kHz]$$

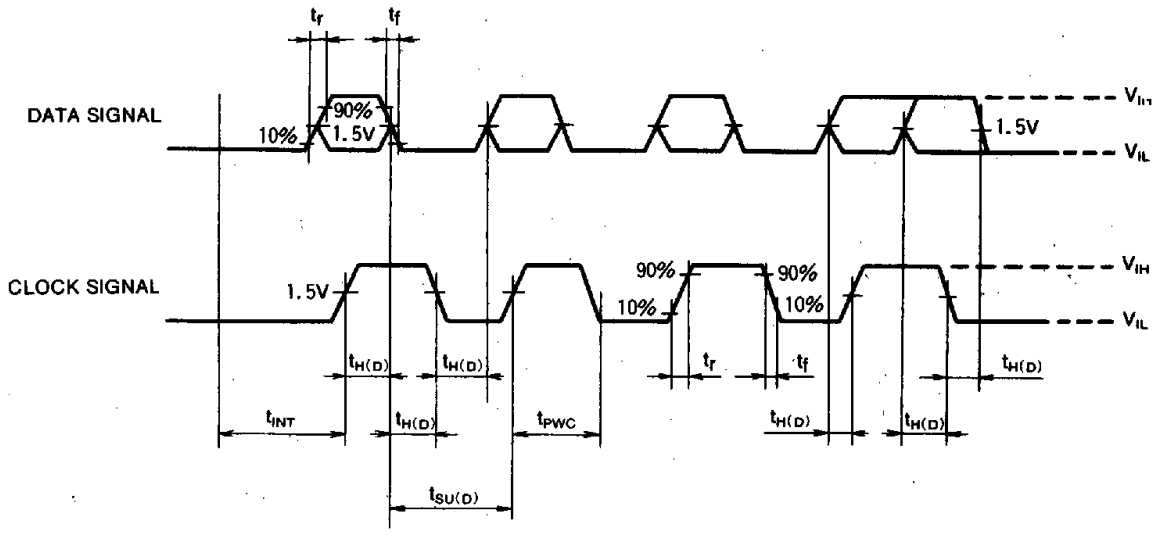
Therefore, the tuning frequency range is 64MHz~1,023.9375MHz.

TIMING DIAGRAM

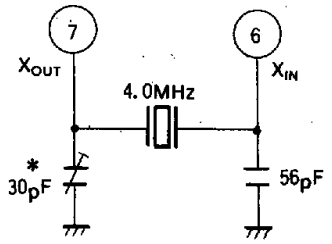
(1) When the control method selection pin SW is set to Vcc(V)



(2) When the control method selection pin SW is set to GND



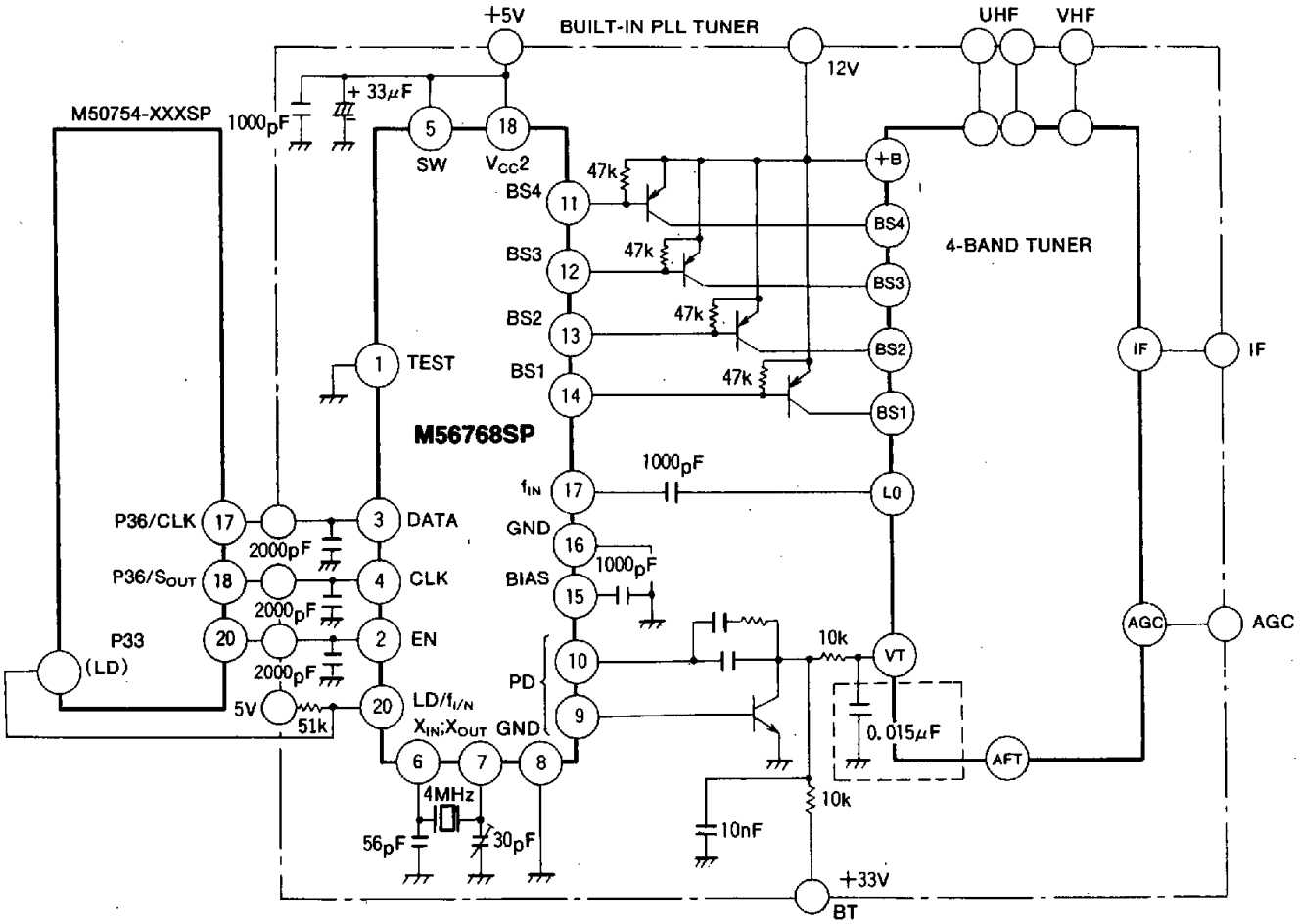
CRYSTAL OSCILLATATOR CONNECTION DIAGRAM



CRYSTAL OSCILLATOR CHARACTERISTICS
Actual resistance : less than 100Ω
Load capacitance : 20pF
*This trimmer is used to compensate for frequency variations of around ±20~30 ppm due to the crystal oscillator characteristics and oscillator circuit capacitance.

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VCR

APPLICATION EXAMPLE



Unit Resistance : Ω
Capacitance : F

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VCR

DESCRIPTION OF PIN

No.	Pin	Name	Description of function
①	TEST	Test input	Pin is used for testing, and is normally set low, in which case LD is selected and f_{REF} is set low. When set high, f_{REF} and $f_{I/N}$ outputs are selected and phase comparator output enters high impedance state.
②	EN	Enable input	Pin is normally set low. When set high,data and clock signals are read, and data is read into latch at falling edge of 18th clock signals pulse. Clock signal then becomes invalid.
③	DATA	Data input	Programmable divider division set input.
④	CLK	Clock input	When SW pin is set to V_{CC} or OPEN. data is read into shift register when clock signal drops from high to low. When SW pin is set to GND. data is read into shift register when clock signal rises from low to high.
⑤	SW	Control method selection pin	When SW pin is set to V_{CC} or OPEN. division ratio of programmable divider is set for enable input, data input and clock input pins. When SW pin is set to GND. division ratio of programmable divider is set for data input and clock input pins only.
⑥ ⑦	X_{IN} X_{OUT}	Crystal oscillator connect pin	4.0MHz crystal oscillator is connected.
⑧	GND_1	GND_1	Connect to 0V.
⑨ ⑩	PD2 PD1	Phase comparator output 2 Phase comparator output 1	When phase programmable divider division output ($f_{I/N}$) is advanced with respect to reference frequency (f_{REF}), output becomes high, and when programmable divider division output is delayed, it becomes low. When the two are in sync, output enters high-impedance state.
⑪ ⑫ ⑬ ⑭	BS4 BS3 BS2 BS1	Band-switching output pin	Open-collector band-switching outputs When band-switching data is high, output goes ON, when low, it goes OFF.
⑮	BIAS	Bias input	Prescaler bias pin. Capacitance of 1000pF is inserted between GND and this pin.
⑯	GND_2	GND2	Connect to 0V.
⑰	f_{IN}	Prescaler input pin	Prescaler input pin, to which V. C. O. frequency is applied.
⑱	V_{CC}	Supply voltage	Supply voltage pin, 5.0±0.5V is applied.
⑲	f_{REF}	Reference frequency output	When TEST input is a low, there is a constant low-level output. When high, reference frequency output (f_{REF}) is selected. Reference frequency is 7.8125kHz with open-collector output.
⑳	LD/$f_{I/N}$	Lock detector/ division output	When TEST input is low, lock detector output (LD) is selected. When high, programmable divider division output ($f_{I/N}$) is selected. Open-collector output. When PLL is locked. lock detector output (LD) becomes low.when PLL is unlocked, it becomes high.