SONY

SP8T GSM/UMTS Dual Mode Antenna Switch

CXG1198AEQ

Description

The CXG1198AEQ is one of a range of low insertion loss, high power MMIC antenna switches for GSM/UMTS dual-mode handset. The low insertion loss serves to extend the handset talk time.
The switch also contains on-chip logic circuits and built-in dual-LPF on GSM transmit paths for suppression of transmitter harmonics. The dual-LPF is mounted on the lead frame and enables the reduction of component count and simple PCB layout.
(Applications: GSM (Triple/Quad band)/UMTS (Dual band) dual-mode handset)

Features

- ◆ Low height (1.3mm Max.)
- ◆ Low insertion loss
  - 0.90dB (Typ.) on Tx2 (1910MHz)
  - 0.90dB (Typ.) on Rx4 (1990MHz)
  - 0.50dB (Typ.) on TRx (1980MHz)
- ◆ Built-in dual-LPF
  - Att –30dB (Typ.) @2fo (Tx1)
  - Att –30dB (Typ.) @2fo (Tx2)
- ◆ 3 CMOS compatible control lines
- ◆ Small package size
  - 28-pin LQFN (4.5mm × 3.2mm × 1.3mm)

Package

28-pin LQFN (Plastic)

Structure

GaAs Junction-gate PHEMT built-in logic circuits and dual-LPF
Sony PHEMT GaAs process is utilized for low insertion loss.

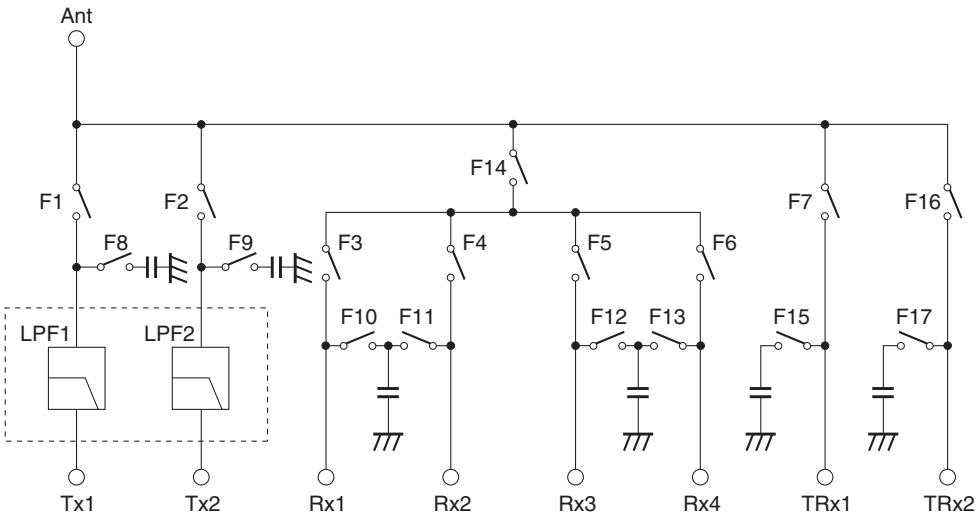
This IC is ESD sensitive device. Special handling precautions are required.

Absolute Maximum Ratings

(Ta = 25℃)

◆ Bias voltage	V_{DD}	7	V
◆ Control voltage (CTL-A/B/C)	Vctl	5	V
◆ Operating temperature	Topr	–30 to +90	℃
◆ Storage temperature	Tstg	–65 to +150	℃

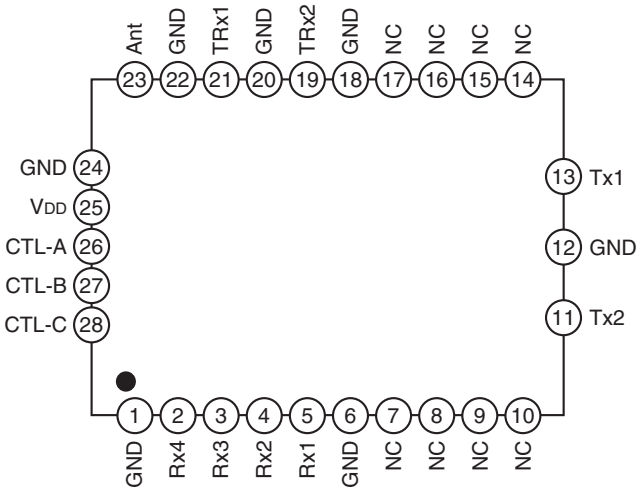
Block Diagram



Note) Built-in SW control circuit

Pin Configuration

(Top View)



Note) Each Rx pin can be used from 869 to 1990MHz frequency range.
User can select these Rx pins suitably.

Pin Description

Pin No.	Symbol	Pin No.	Symbol
1	GND	15	NC
2	Rx4	16	NC
3	Rx3	17	NC
4	Rx2	18	GND
5	Rx1	19	TRx2
6	GND	20	GND
7	NC	21	TRx1
8	NC	22	GND
9	NC	23	Ant
10	NC	24	GND
11	Tx2	25	V_{DD}
12	GND	26	CTL-A
13	Tx1	27	CTL-B
14	NC	28	CTL-C

Truth Table

Item	Vctl state			Switch state																
	A	B	C	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17
Tx1	H	H	L	H	L	L	L	L	L	L	L	H	H	H	H	H	L	H	L	H
Tx2	H	L	L	L	H	L	L	L	L	L	H	L	H	H	H	H	L	H	L	H
Rx1	L	L	L	L	L	H	L	L	L	L	H	H	L	H	H	H	H	H	L	H
Rx2	L	L	H	L	L	L	H	L	L	L	H	H	H	L	H	H	H	H	L	H
Rx3	L	H	H	L	L	L	L	H	L	L	H	H	H	H	L	H	H	H	L	H
Rx4	L	H	L	L	L	L	L	L	H	L	H	H	H	H	H	L	H	H	L	H
TRx1	H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	L	L	L	H
TRx2	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	L	H	H	L

Electrical Characteristics

(V_{DD} = 2.8V, Vctl = 2.8V, Ta = 25℃)

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	Tx1 – Ant	*1	—	0.80	1.00	dB
		Tx2 – Ant	*2	—	0.90	1.15	
		Ant – TRx1 (Tx)	*3	—	0.50	0.70	
		Ant – TRx2 (Tx)	*3	—	0.50	0.70	
		Ant – Rx1	*4	—	0.80	1.00	
		Ant – Rx2	*4	—	0.80	1.00	
		Ant – Rx3	*5	—	0.95	1.20	
		Ant – Rx4	*5	—	0.95	1.20	
		Ant – TRx1 (Rx)	*6	—	0.60	0.80	
		Ant – TRx2 (Rx)	*6	—	0.60	0.80	

*1 Frequency = 915MHz, Input signal is CW, Pin = +34dBm

*2 Frequency = 1910MHz, Input signal is CW, Pin = +32dBm

*3 Frequency = 1980MHz, Input signal is CW, Pin = +29dBm

*4 Frequency = 960MHz, Input signal is CW, Pin = –5dBm

*5 Frequency = 1990MHz, Input signal is CW, Pin = –5dBm

*6 Frequency = 2170MHz, Input signal is CW, Pin = –5dBm

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Isolation	ISO.	Active path: Tx1					dB
		Ant – Rx1	824 to 915MHz	27	—	—	
		Ant – Rx2		27	—	—	
		Ant – Rx3		30	—	—	
		Ant – Rx4		30	—	—	
		Ant – Tx2		25	—	—	
			1760 to 1830MHz	25	—	—	
		Ant – TRx1	824 to 915MHz	25	—	—	
		Ant – TRx2		25	—	—	
		Active path: Tx2					
		Ant – Rx1	1710 to 1785MHz 1850 to 1910MHz	20	—	—	
		Ant – Rx2		20	—	—	
		Ant – Rx3		32	—	—	
		Ant – Rx4		30	—	—	
		Ant – TRx1		20	—	—	
		Ant – TRx2		20	—	—	
		Active path: TRx1/TRx2					
		Ant – Rx1	810 to 855MHz 1920 to 1980MHz	20	—	—	
		Ant – Rx2		20	—	—	
		Ant – Rx3		20	—	—	
		Ant – Rx4		20	—	—	
		Ant – Tx1	824 to 915MHz	20	—	—	
		Ant – Tx2	1710 to 1785MHz 1850 to 1910MHz	20	—	—	
		Active path: TRx1					
		Ant – TRx2	810 to 855MHz	20	—	—	
			1920 to 1980MHz	20	—	—	
		Active path: TRx2					
		Ant – TRx1	810 to 855MHz	25	—	—	
			1920 to 1980MHz	20	—	—	
		Active path: Rx1					
		Ant – Tx1	824 to 915MHz	20	—	—	
		Ant – Tx2	1710 to 1785MHz 1850 to 1910MHz	20	—	—	
		Active path: Rx2					
		Ant – Tx1	824 to 915MHz	20	—	—	
		Ant – Tx2	1710 to 1785MHz 1850 to 1910MHz	20	—	—	
		Active path: Rx3					
		Ant – Tx1	824 to 915MHz	20	—	—	
		Ant – Tx2	1710 to 1785MHz 1850 to 1910MHz	20	—	—	
		Active path: Rx4					
		Ant – Tx1	824 to 915MHz	20	—	—	
		Ant – Tx2	1710 to 1785MHz 1850 to 1910MHz	30	—	—	

Item	Symbol	Path		Condition		Min.	Typ.	Max.	Unit
Harmonics		Tx1 – Ant	2nd Harmonic	1648 to 1698MHz 1760 to 1830MHz	CW, Pin = +34dBm	—	–40	–35	dBm
			3rd Harmonic	2472 to 2547MHz 2640 to 2745MHz		—	–38	–33	
		Tx2 – Ant	2nd Harmonic	3420 to 3570MHz 3760 to 3820MHz	CW, Pin = +32dBm	—	–40	–35	
			3rd Harmonic	5130 to 5355MHz 5550 to 5730MHz		—	–38	–33	
		TRx1 – Ant	2nd Harmonic	1620 to 1710MHz 3840 to 3960MHz	CW, Pin = +29dBm	—	–40	–35	
		TRx2 – Ant	3rd Harmonic	2430 to 2565MHz 5760 to 5940MHz		—	–38	–33	
Attenuation		Tx1 – Ant		1648 to 1830MHz	2fo	25	30	—	dB
				2472 to 2745MHz	3fo	25	30	—	
				3296 to 3660MHz	4fo	20	25	—	
				4120 to 4575MHz	5fo	20	25	—	
				4944 to 5490MHz	6fo	15	20	—	
				5768 to 6405MHz	7fo	15	20	—	
		Tx2 – Ant		3420 to 3820MHz	2fo	25	30	—	
				5130 to 5730MHz	3fo	25	30	—	

Supply voltage

(Ta = 25°C)

Item	Min.	Typ.	Max.	Unit
Bias voltage (V_{DD})	2.6	2.8	3.6	V

Control voltage

(Ta = 25°C)

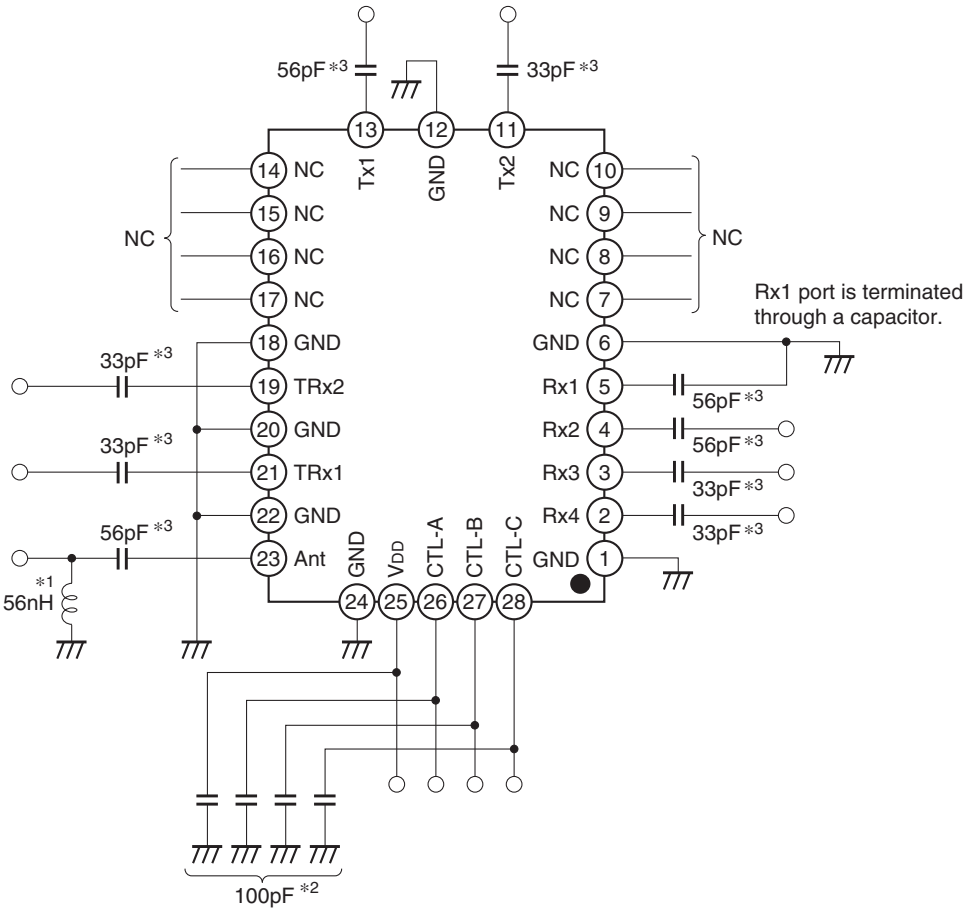
Item	State	Min.	Typ.	Max.	Unit
Control voltage (CTL-A/B/C)	High	2.0	2.8	3.6	V
	Low	0	—	0.5	

Current consumption

Item	Condition	Min.	Typ.	Max.	Unit
Bias current	V_{DD} = 2.8V	—	250	350	μA
Control current	Vctl (H) = 2.8V/1-wire	—	25	36	

Recommended Circuit 1

(For 3GSM + 2UMTS solution)

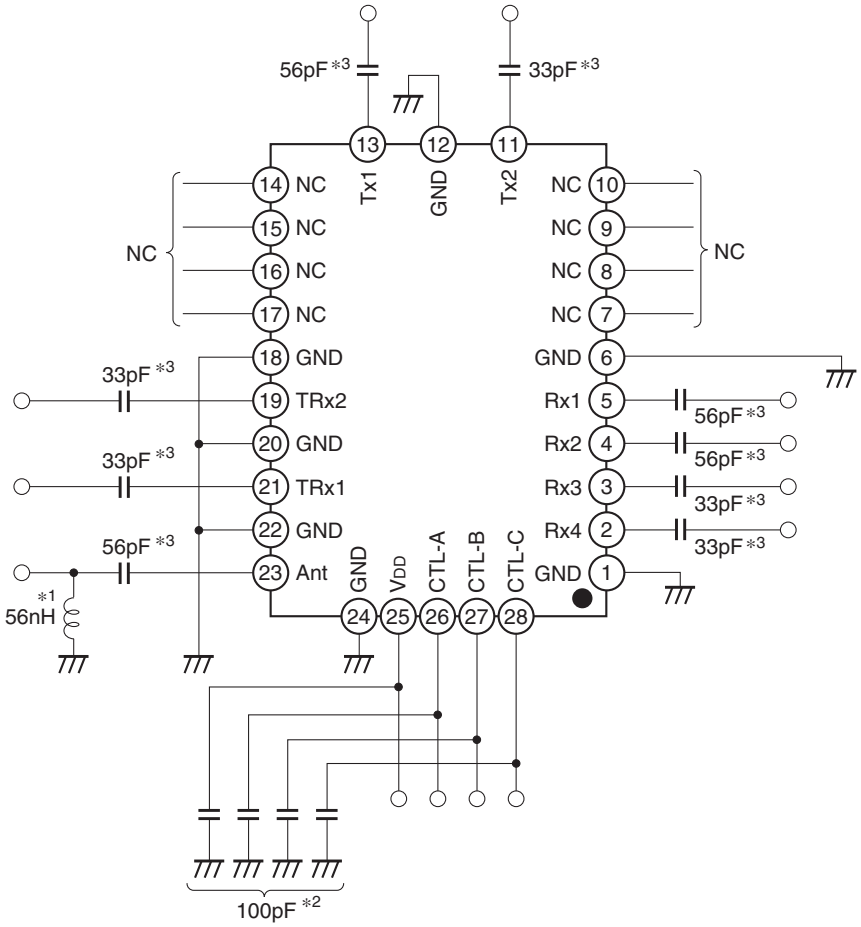


In this circuit, Rx2, Rx3 and Rx4 are used for GSM triple band receive path.
The Rx1 is not used in this example.
User can select these Rx paths suitably.

*1 Inductor (56nH) is recommended on Ant port for ESD protection.
*2 These capacitors are not mandatory.
*3 Capacitors are required on all RF ports for DC blocking.
Recommended capacitance is as follows.
For 800 to 960MHz signal: 56pF
For 1700 to 2200MHz signal: 33pF

Recommended Circuit 2

(For 4GSM + 2UMTS solution)

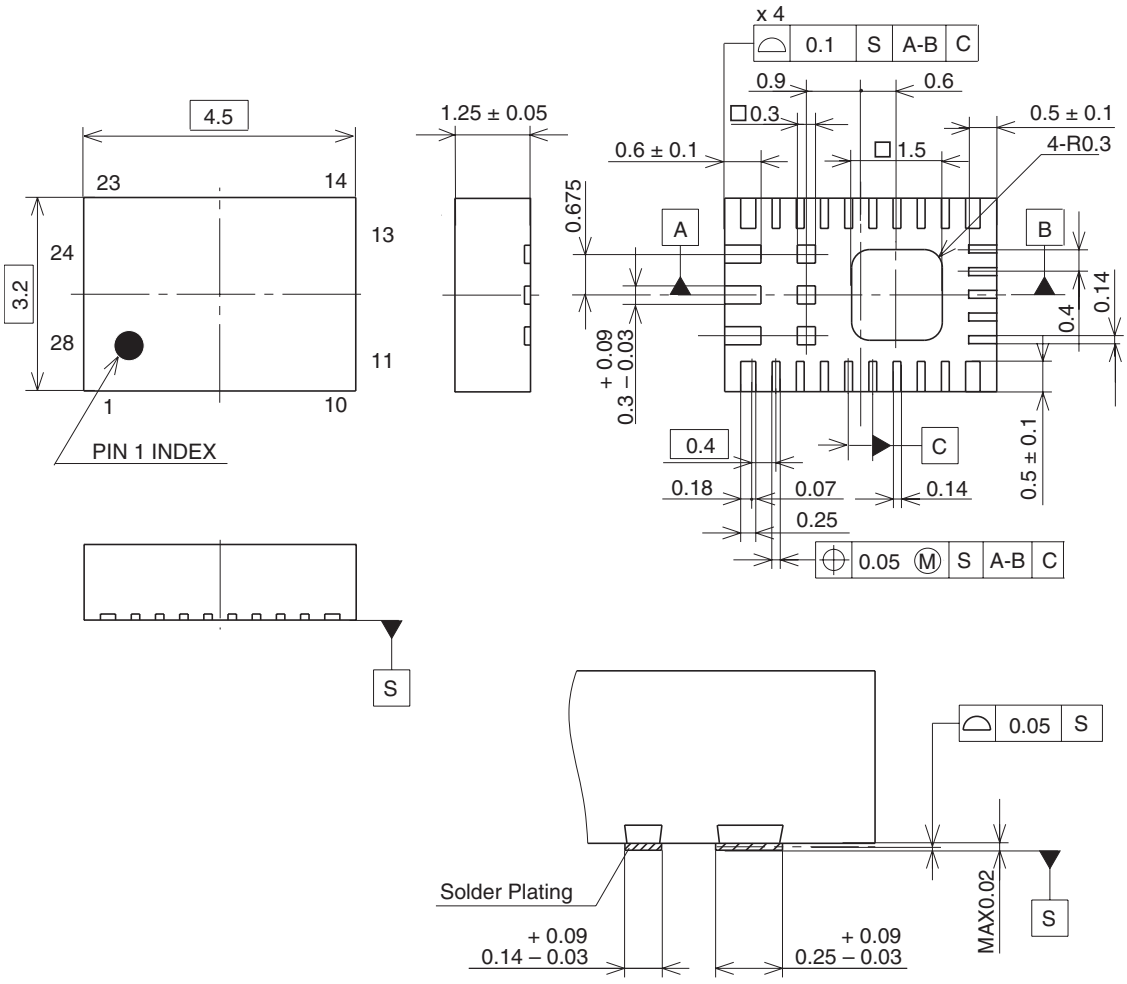


*1 Inductor (56nH) is recommended on Ant port for ESD protection.
*2 These capacitors are not mandatory.
*3 Capacitors are required on all RF ports for DC blocking.
Recommended capacitance is as follows.
For 800 to 960MHz signal: 56pF
For 1700 to 2200MHz signal: 33pF

Package Outline

(Unit: mm)

28PIN LQFN (PLASTIC)



TERMINAL SECTION

Note:Cutting burr of lead are 0.05mm MAX.

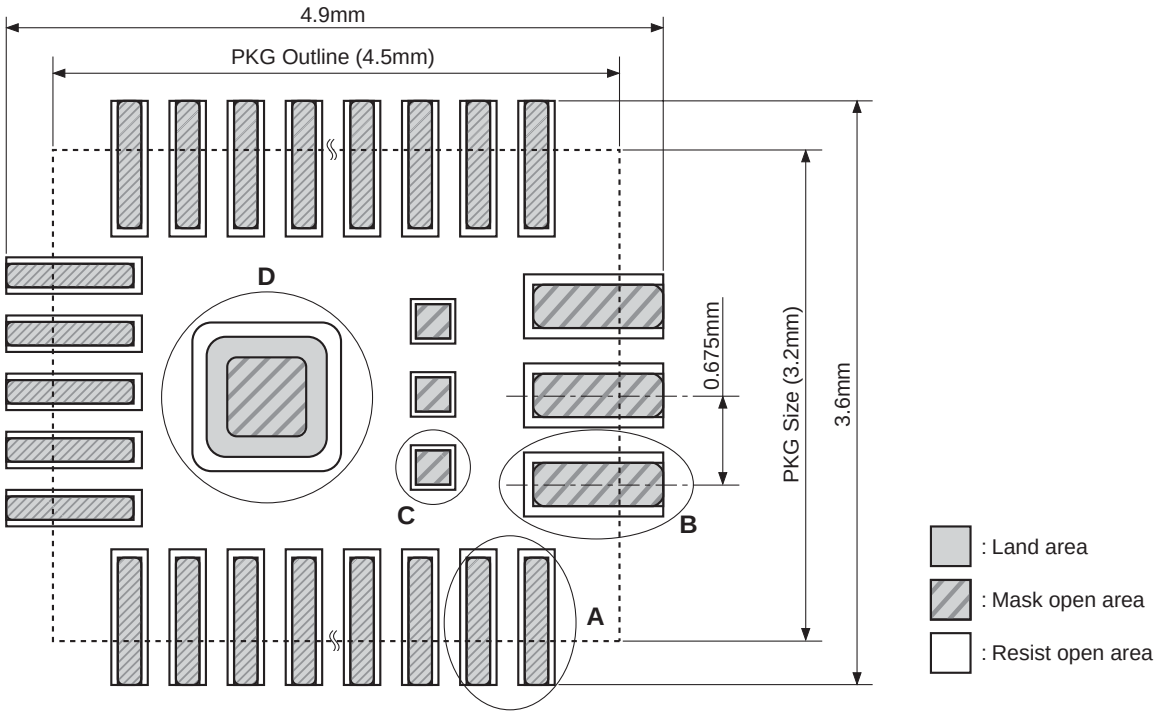
SONY CODE	LQFN-28P-01
EIAJ CODE	————
JEDEC CODE	————

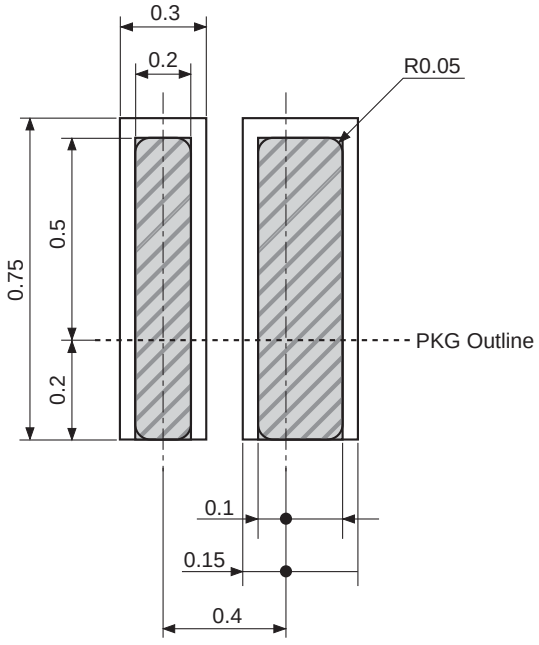
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.05g

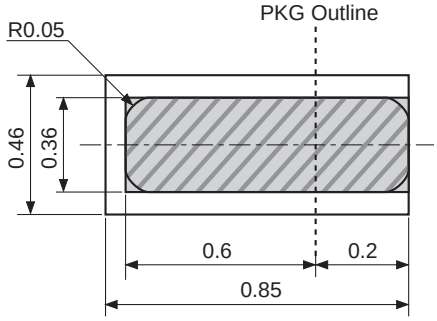
LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm

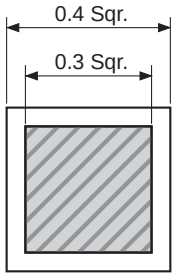




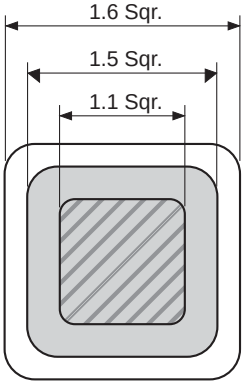
[Detail A]



[Detail B]



[Detail C]



[Detail D]

(Unit: mm)