Features

- **ARM7TDMI™ ARM® Thumb® Processor Core**
- **Two 16-bit Fixed-point OakDSPCore® Cores**
- **256 x 32-bit Boot ROM**
- **88K Bytes of Integrated Fast RAM for Each DSP**
- **Flexible External Bus Interface with Programmable Chip Selects**
- **Dual Codec Interface**
- **Multi-level Priority, Individually Maskable, Vectored Interrupt Controller**
- **Three 16-bit Timer/Counters**
- **Additional Watchdog Timer**
- **Two USARTs with FIFO and Modem Control Lines**
- **Industry Standard Serial Peripheral Interface (SPI)**
- **Up to 23 General-purpose I/O Pins**
- **On-chip DRAM Controller**
- **JTAG Debug Interface**
- **Software Development Suites Available for ARM7TDMI and OakDSPCore**
- **Supported by a Wide Range of Ready-to-use Application Software, including Multitasking Operating System, Networking, Modems, and Voice-processing Functions**
- **Available in 160-lead PQFP Package**
- **3.3V Power Supply**

Description

The Atmel AT75C310 Smart Internet Appliance Processor (SIAP) is a high-performance processor specially designed for Internet appliance applications, such as Internet telephony (Voice over Internet Protocol – VoIP). The AT75C310 is built around an ARM7TDMI microcontroller core running at 20 MIPS with two DSP co-processors running at 40 MIPS each – all three processors delivering unmatched performance for low power consumption.

In a typical standalone VoIP phone, one DSP handles the voice-processing functions (voice compression, acoustic echo cancellation, etc.), while the other one deals with the telephony functions (dialing, line echo cancellation, callerID detection, high-speed modem, etc.). In such an application, the power of the ARM7TDMI allows it to run the VoIP protocol stack as well as all the system control tasks.

Atmel provides the AT75C310 with three levels of software modules:

- a special port of the Linux kernel as the proposed operating system
- a comprehensive set of tunable DSP algorithms for modems and voice processing, specially tailored to be run by the DSP subsystems
- a broad range of application-level software modules such as H323 telephony or POP-3/SMTP e-mail services

Smart Internet Appliance Processor – Electrical and Mechanical Characteristics

AT75C310

Rev. 1370A–07/00

Absolute Maximum Ratings*

Operating Temperature (Commercial)	0°C to +70°C
Voltage on Any Input Pin with Respect to Ground-	0.5V to +4.0V
Maximum Operating Voltage	4.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	DC Supply		3.0	3.3	3.6	V
T_A	Ambient Temperature		0		70	°C
V_{IL}	Input Low Voltage	V_{DD} = 3.0V to 3.6V	-0.5		0.3 x V_{DD}	V
V_{IH}	Input High Voltage	V_{DD} = 3.0V to 3.6V	0.7 x V_{DD}		3.6	V
V_{OL}	Output Low Voltage	I_{OL} = 0.8 mA, V_{DD} = 3.3V			0.1	V
V_{OH}	Output High Voltage	I_{OH} = 0.8 mA, V_{DD} = 3.3V	V_{DD} - 0.1			V

AC Characteristics

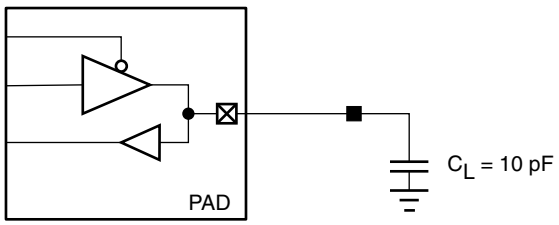
Conditions

The values are for full temperature range and worst-case process.

Environment Constraints

The output delays are valid for a capacitive load of 10 pF, as shown in Figure 1.

Figure 1. Output/Bidir Pad Capacitive Load



Memory Timing Waveforms

Figure 2. DRAM Read Cycle (Single Read)

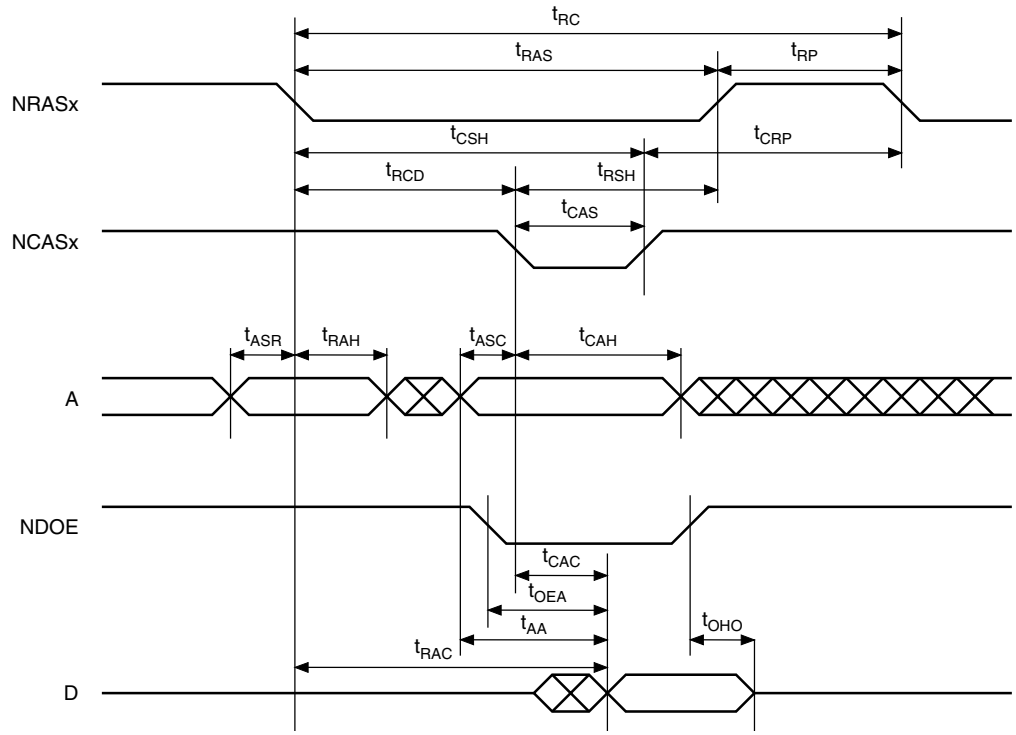


Table 1. DRAM Read Cycle (Single Read) Timings

Symbol	Parameter	Min (ns)	Max (ns)
t_{RC}	Read or Write Cycle Time	125.0	–
t_{RAS}	RAS Pulse Width	82.0	–
t_{RP}	RAS Precharge Time	42.0	–
t_{CSH}	CAS Hold Time	61.0	–
t_{CRP}	CAS to RAS Precharge Time	49.0	–
t_{RCD}	RAS to CAS Delay Time	41.0	–
t_{RSH}	RAS Hold Time	29.0	–
t_{CAS}	CAS Pulse Width	20.0	–
t_{ASR}	Row Address Setup Time	1.0	
t_{RAH}	Row Address Hold Time	22.0	
t_{ASC}	Column Address Setup Time	15.0	
t_{CAH}	Column Address Hold Time	21.0	
t_{CAC}	Access Time from CAS	–	22.0
t_{OEA}	Access Time from NDOE	–	34.0
t_{AA}	Access Time from Column Address	–	38.0
t_{RAC}	Access Time from RAS	–	63.0
t_{OHO}	Data Hold from NDOE	0	–

Figure 3. DRAM Read Cycle (Burst Read)

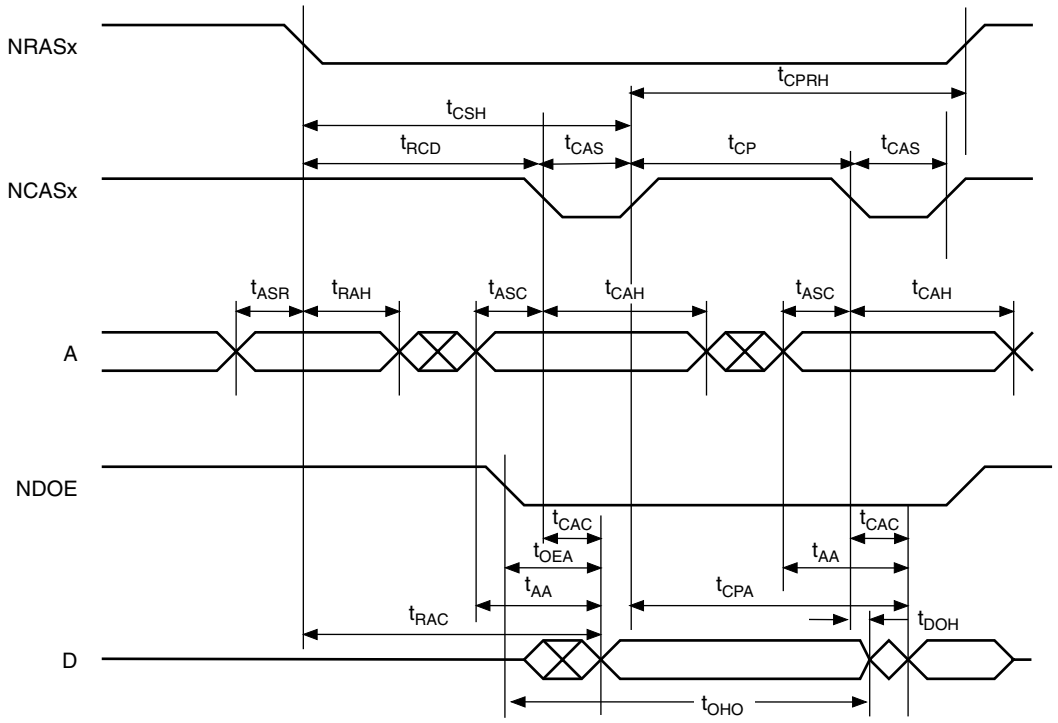


Table 2. DRAM Read Cycle (Burst Read) Timings

Symbol	Parameter	Min (ns)	Max (ns)
t_{CPRH}	RAS Hold Time from CAS Precharge	48.0	–
t_{CSH}	CAS Hold Time	61.0	–
t_{RCD}	RAS to CAS Delay Time	41.0	–
t_{CAS}	CAS Pulse Width	20.0	–
t_{CP}	CAS Precharge Time	19.0	–
t_{ASR}	Row Address Setup Time	1.5	
t_{RAH}	Row Address Hold Time	22.0	
t_{ASC}	Column Address Setup Time	15.0	
t_{CAH}	Column Address Hold Time	21.0	
t_{CAC}	Access Time from CAS	–	22.0
t_{OEA}	Access Time from NDOE	–	34.0
t_{AA}	Access Time from Column Address	–	38.0
t_{RAC}	Access Time from RAS	–	63.0
t_{CPA}	Access Time from CAS Precharge	–	43.0
t_{OHO}	Data Hold from NDOE	0	–
t_{DOH}	Data Hold from CAS Low	0	–

Figure 4. DRAM Write Cycle (Single Write)

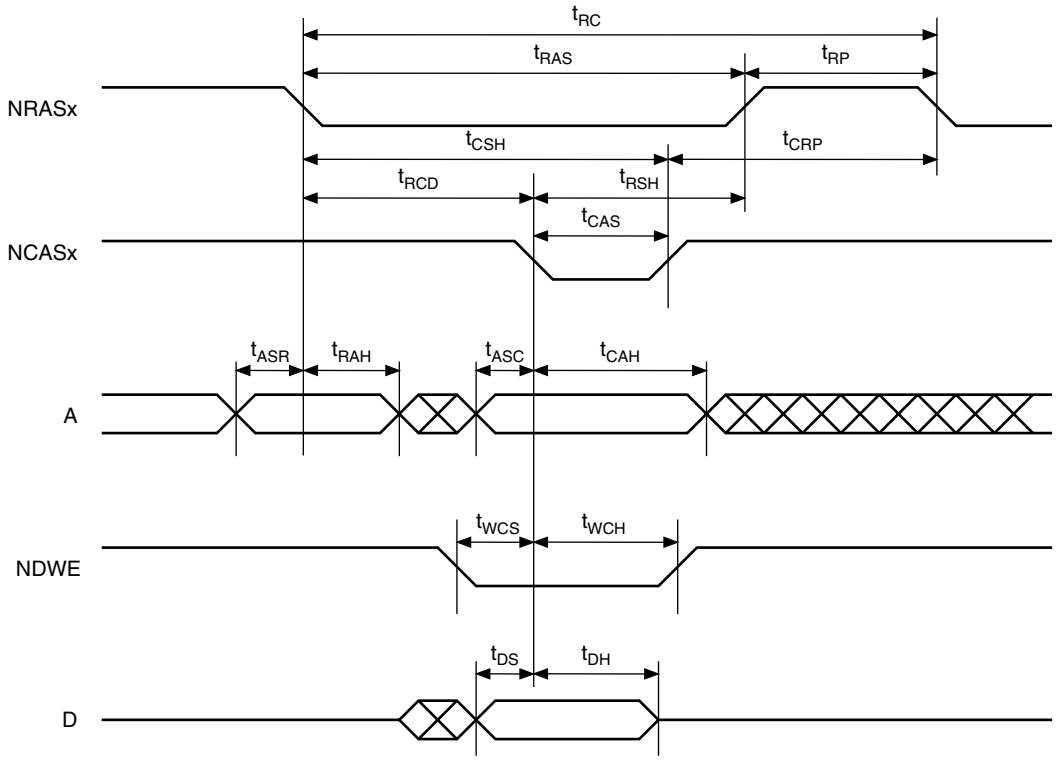


Table 3. DRAM Write Cycle (Single Write) Timings

Symbol	Parameter	Min (ns)	Max (ns)
t_{RC}	Read or Write Cycle Time	125.0	–
t_{RAS}	RAS Pulse Width	82.0	–
t_{RP}	RAS Precharge Time	42.0	–
t_{CSH}	CAS Hold Time	61.0	–
t_{CRP}	CAS to RAS Precharge Time	49.0	–
t_{RCD}	RAS to CAS Delay Time	41.0	–
t_{RSH}	RAS Hold Time	29.0	–
t_{CAS}	CAS Pulse Width	20.0	–
t_{ASR}	Row Address Setup Time	1.5	–
t_{RAH}	Row Address Hold Time	22.0	–
t_{ASC}	Column Address Setup Time	15.0	–
t_{CAH}	Column Address Hold Time	21.0	–
t_{WCS}	Write Command Setup Time	18.0	–
t_{WCH}	Write Command Hold Time	21.0	–
t_{DS}	Data Setup Time	8.0	–
t_{DH}	Data Hold Time	21.0	–

Figure 5. DRAM Refresh Cycle

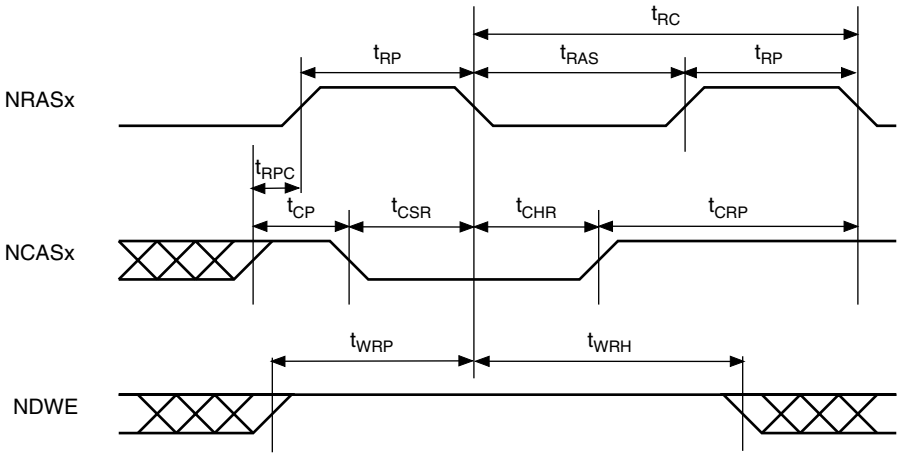


Table 4. DRAM Refresh Cycle Timings

Symbol	Parameter	Min (ns)	Max (ns)
t_{RC}	Cycle Time	125.0	–
t_{RAS}	RAS Pulse Width	82.0	–
t_{RP}	RAS Precharge Time	42.0	–
t_{CP}	CAS Precharge Time	19.0	–
t_{RPC}	RAS Precharge before CAS	33.0	–
t_{CSR}	CAS Setup before RAS	48.0	–
t_{CHR}	CAS Hold after RAS	32.0	–
t_{CRP}	CAS to RAS Precharge Time	49.0	–
t_{WRP}	Write Enable Setup Time (Refresh Cycle)	91.0	–
t_{WRH}	Write Enable Hold Time (Refresh Cycle)	32.0	–

Figure 6. Static Memory Read Cycle (Zero Wait State)

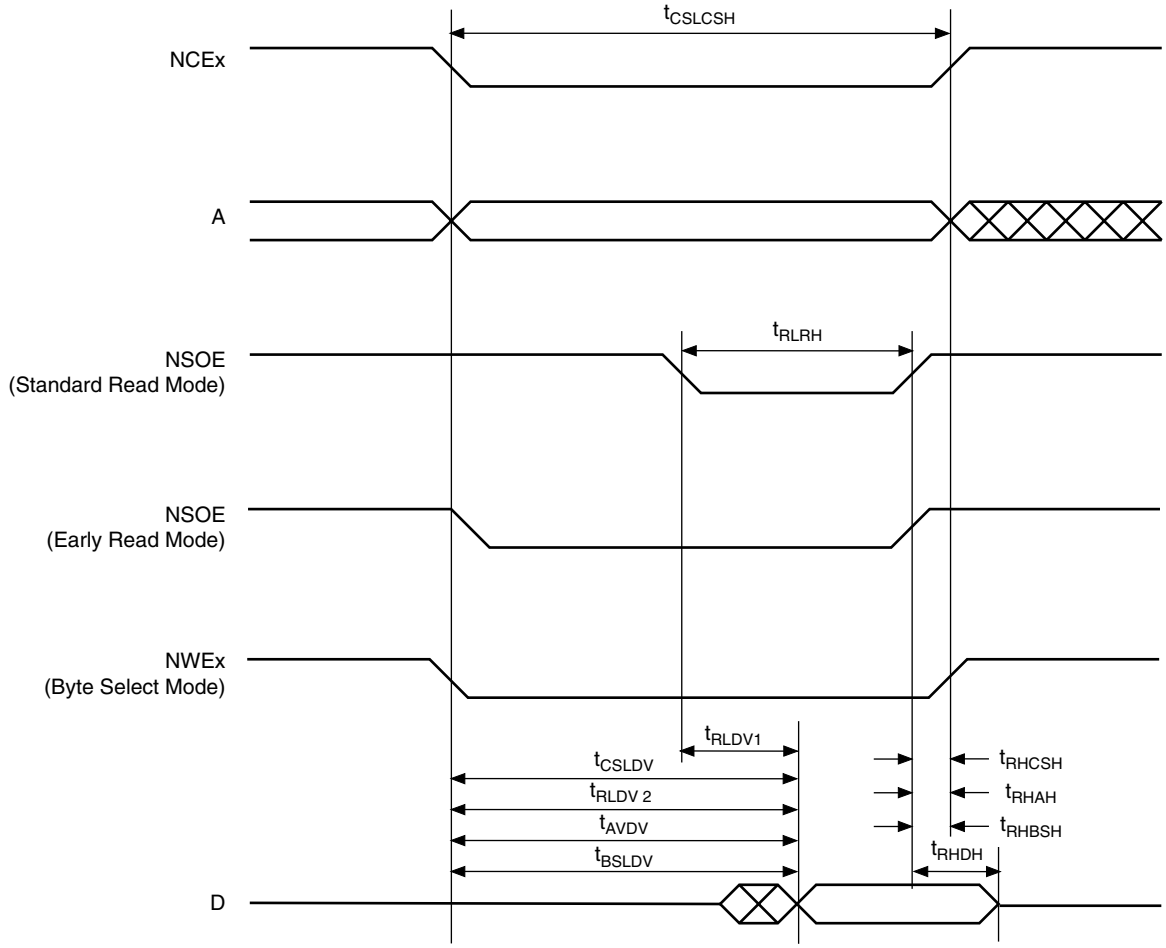


Table 5. Static Memory Read Cycle (Zero Wait State) Timings

Symbol	Parameter	Min (ns)	Max (ns)
t_{CSLCSH}	Chip Select Low to Chip Select High Time	40.0	–
t_{RLRH}	Read Strobe Low to Read Strobe High Time	19.0	–
t_{RLDV1}	Read Strobe Low to Data Valid Time – Standard Read Mode	–	6.0
t_{RLDV2}	Read Strobe Low to Data Valid Time – Early Read Mode	–	27.0
t_{CSLDV}	Chip Select Low to Data Valid	–	25.0
t_{AVDV}	Address Valid to Data Valid	–	24.0
t_{BSLDV}	Byte Select Low to Data Valid	–	26.0
t_{RHCSH}	Read Strobe High to Chip Select High	0	–
t_{RHAH}	Address Hold after Read Strobe High	0	–
t_{RHBSH}	Read Strobe High to Byte Select High	0	–
t_{RHDH}	Data Hold after Read Strobe High	0	–

Figure 7. Static Memory Write Cycle (Zero Wait State)

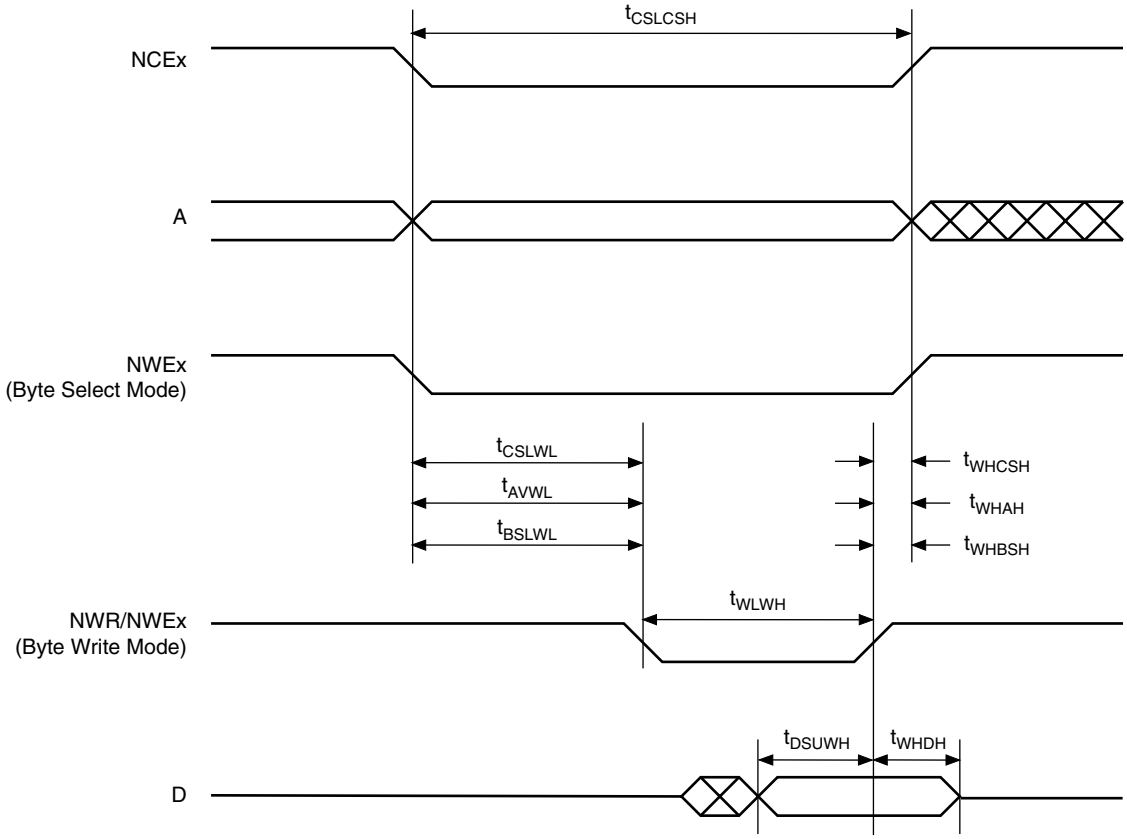


Table 6. Static Memory Write Cycle (Zero Wait State) Timings

Symbol	Parameter	Min (ns)	Max (ns)
t_{CSLCSH}	Chip Select Low to Chip Select High Time	40.0	–
t_{CSLWL}	Chip Select Low to Write Stobe Low Time	18.0	–
t_{AVWL}	Address Valid to Write Strobe Low Time	17.0	–
t_{BSLWL}	Byte Select Low to Write Strobe Low Time	19.0	–
t_{WHCSH}	Write Strobe High to Chip Select High Time	3.0	–
t_{WHAH}	Address Hold Time after Write Strobe High	4.0	–
t_{WHBSH}	Write Strobe High to Byte Strobe High Time	0	–
t_{WLWH}	Write Strobe Low to Write Strobe High Time	17.0	–
t_{DSUWH}	Data Setup Time before Write Strobe High	13.0	–
t_{WHDH}	Data Hold Time after Write Strobe High	3.0	–

Figure 8. Static Memory Write Cycle (One Wait State)

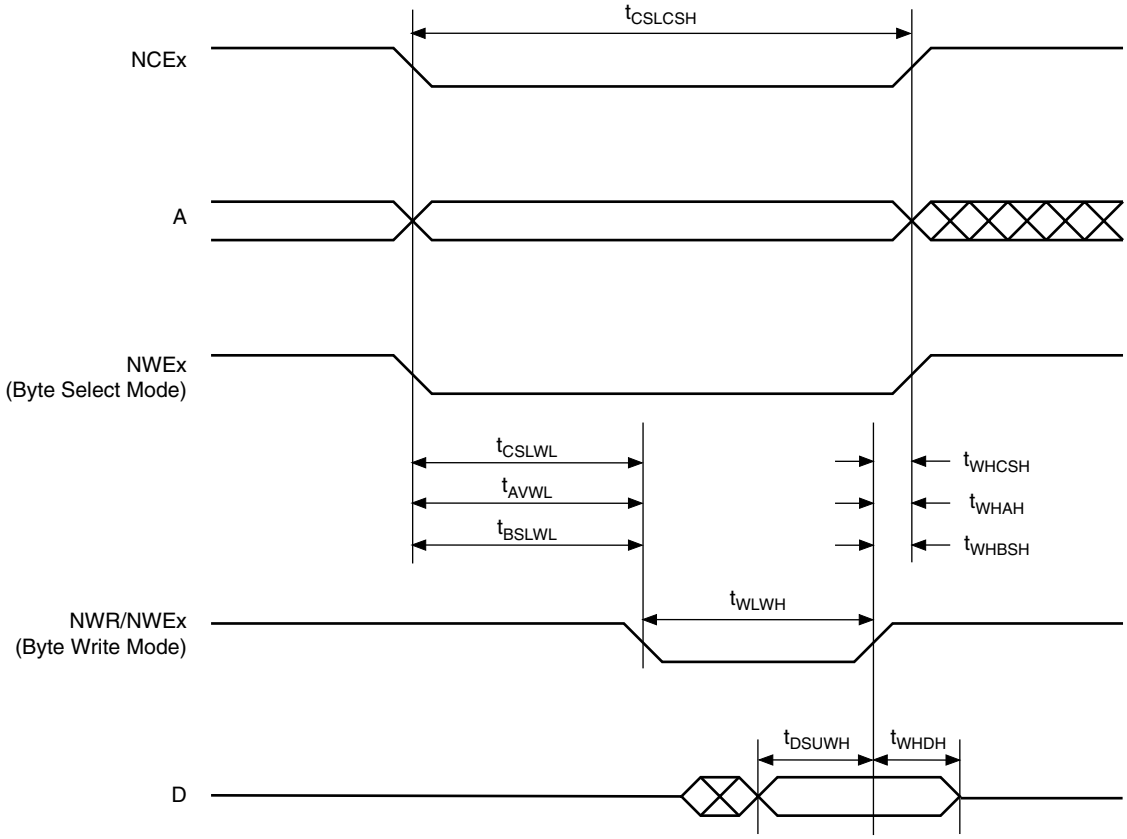


Table 7. Static Memory Write Cycle (One Wait State) Timings

Symbol	Parameter	Min (ns)	Max (ns)
t_{CSLCSH}	Chip Select Low to Chip Select High Time	82.0	–
t_{CSLWL}	Chip Select Low to Write Stobe Low Time	20.0	–
t_{AVWL}	Address Valid to Write Strobe Low Time	19.0	–
t_{BSLWL}	Byte Select Low to Write Strobe Low Time	20.0	–
t_{WHCSH}	Write Strobe High to Chip Select High Time	19.0	–
t_{WHAH}	Address Hold Time after Write Strobe High	20.0	–
t_{WHBSH}	Write Strobe High to Byte Strobe High Time	19.0	–
t_{WLWH}	Write Strobe Low to Write Strobe High Time	40.0	–
t_{DSUWH}	Data Setup Time before Write Strobe High	38.0	–
t_{WHDH}	Data Hold Time after Write Strobe High	20.0	–

Note: Additional wait states will extend the t_{WLWH} and t_{DSUWH} values by one clock period per wait state.

Figure 9. Static Memory Write Cycle (LCD Mode, Two Wait States)

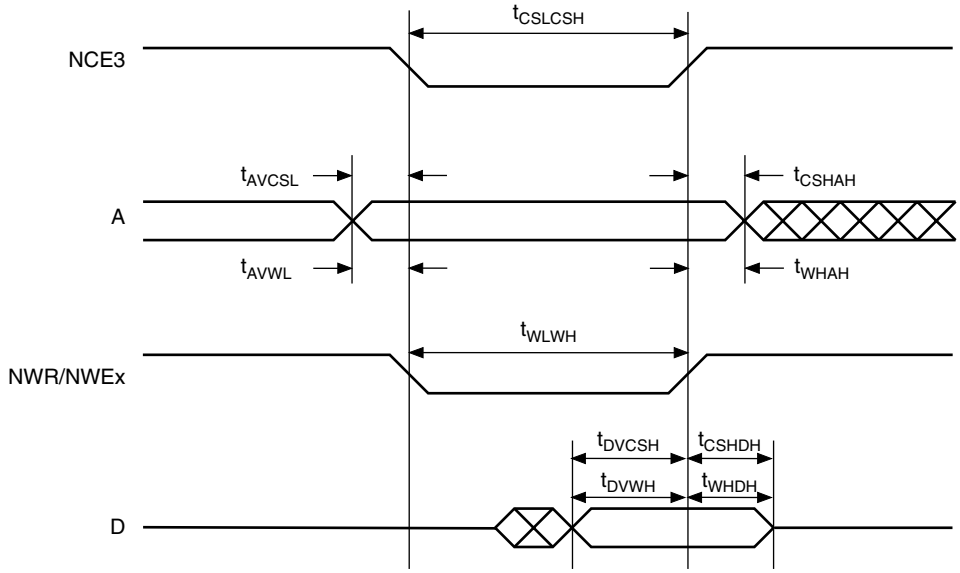


Table 8. Static Memory Write Cycle (LCD Mode, Two Wait States Timings

Symbol	Parameter	Min (ns)	Max (ns)
t_{CSLCSH}	Chip Select Low to Chip Select High Time	82.0	–
t_{AVCSL}	Address Valid to Chip Select Low Time	18.0	–
t_{AVWL}	Address Valid to Write Strobe Low Time	19.0	–
t_{CSHAH}	Address Hold Time after Chip Select High	21.0	–
t_{WHAH}	Address Hold Time after Write Strobe High	20.0	–
t_{WLWH}	Write Strobe Low to Write Strobe High Time	81.0	–
t_{DVCSH}	Data Setup Time before Chip Select High	79.0	–
t_{DVWH}	Data Setup Time before Write Strobe High	79.0	–
t_{CSHDH}	Data Hold Time after Write Chip Select High	21.0	–
t_{WHDH}	Data Hold Time after Write Strobe High	20.0	–

Figure 10. Static Memory Read Cycle (LCD Mode, Two Wait States)

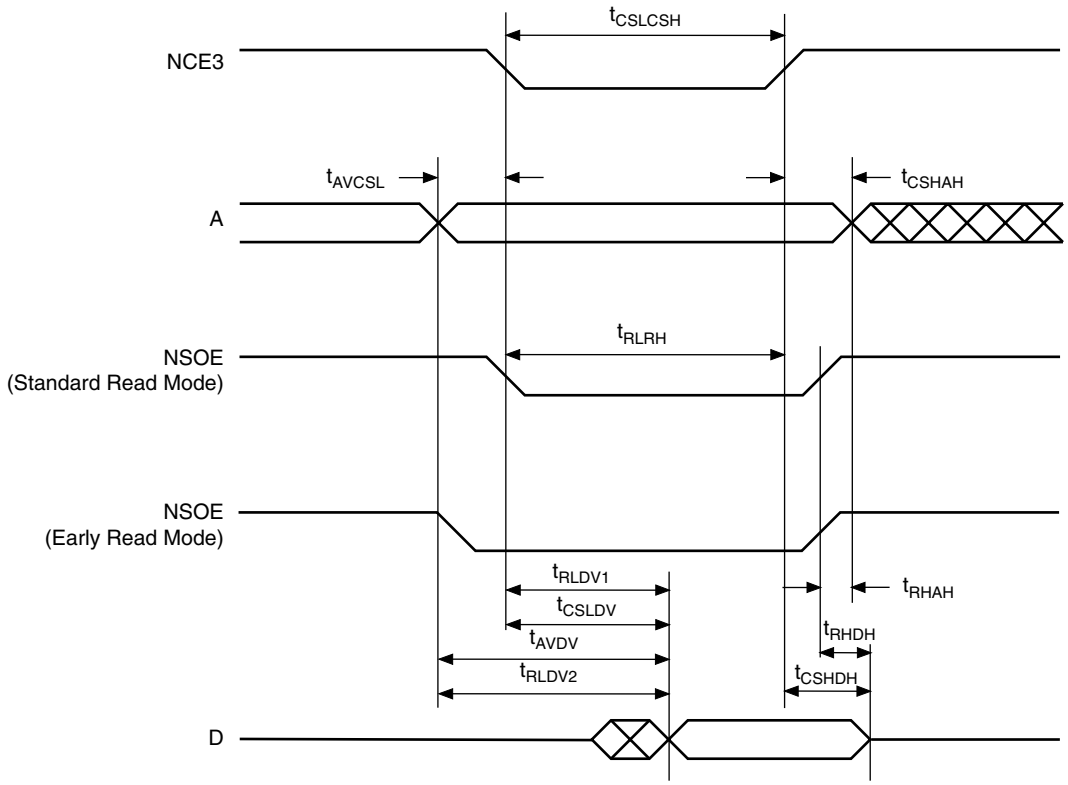


Table 9. Static Memory Read Cycle (LCD Mode, Two Wait States) Timings

Symbol	Parameter	Min (ns)	Max (ns)
t_{CSLCSH}	Chip Select Low to Chip Select High Time	82.0	–
t_{AVCSL}	Address Valid to Chip Select Low	18.0	–
t_{CSHAH}	Address Hold after Chip Select High	21.0	–
t_{RLRH}	Read Strobe Low to Read Strobe High Time	102.0	
t_{RLDV1}	Read Strobe Low to Data Valid Time – Standard Read Mode	–	89.0
t_{RLDV2}	Read Strobe Low to Data Valid Time – Early Read Mode	–	110.0
t_{CSLDV}	Chip Select Low to Data Valid	–	88.0
t_{AVDV}	Address Valid to Data Valid	–	107.0
t_{RHAH}	Address Hold after Read Strobe High	1.0	–
t_{RHDH}	Data Hold after Read Strobe High	0	–
t_{CSHDH}	Data Hold after Chip Select High	18.0	–

External Bus Master Timing

Figure 11. External Bus Master

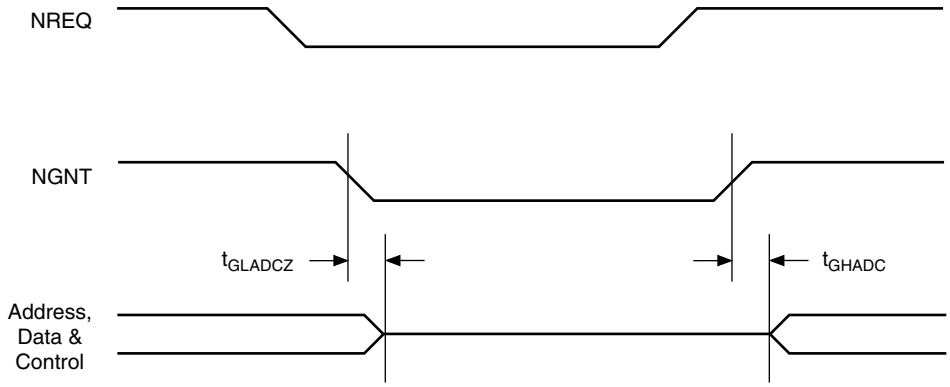


Table 10. External Bus Master Timings

Symbol	Parameter	Min (ns)	Max (ns)
t_{GLADCZ}	NGNT Low to Address, Data & Control Float	2.0	–
t_{GHADC}	NGNT High to Address, Data & Control Driven	0	–

Codec Timing Waveforms

Figure 12. FS and SCLK as Outputs

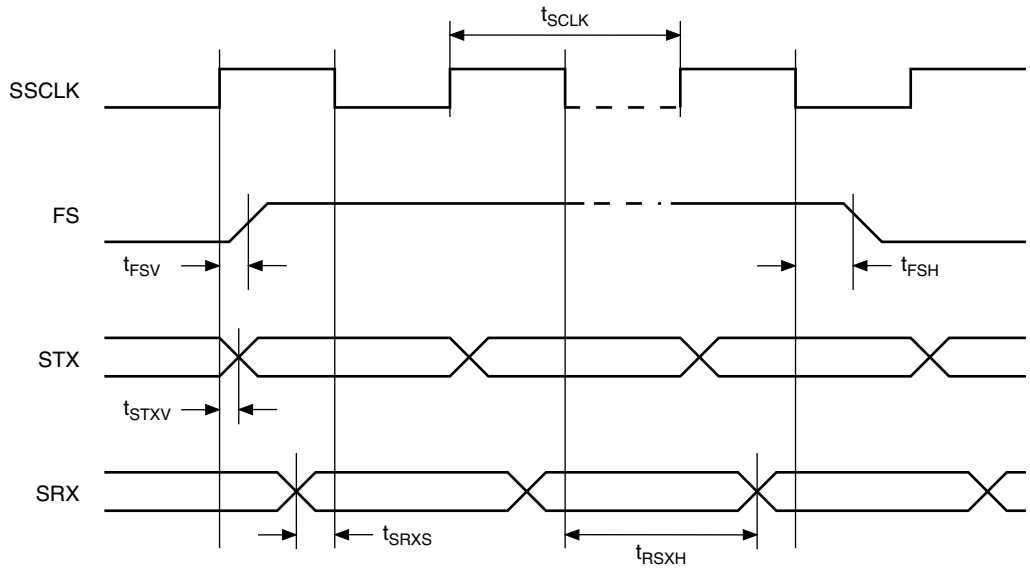


Table 11. FS and SCLK as Outputs Timings

Symbol	Parameter	Min (ns)	Max (ns)
t_{FSV}	FS Valid after TX Edge of SSCLK (Long PCM Type)	–	75.0
	FS Valid after TX Edge of SSCLK (All Other Types)	–	50.0
t_{FSH}	FS Output Hold after Last RX Edge of SSCLK (Long PCM)	49.0	–
	FS Output Hold after Last RX Edge of SSCLK (All Other Types)	25.0	–
t_{STXV}	STX Valid after TX Edge of SSCLK	22.0	25.0
t_{SRXS}	SRX Setup before RX Edge of SSCLK	50.0	–
t_{RSXH}	SRX Hold after RX Edge of SSCLK	0	–
t_{SCLK}	SSCLK Generated Period	100.0	6375.0

Note: All timings based on worst-case conditions of Codec A or B interface and so apply to both.

Figure 13. FS and SCLK as Inputs

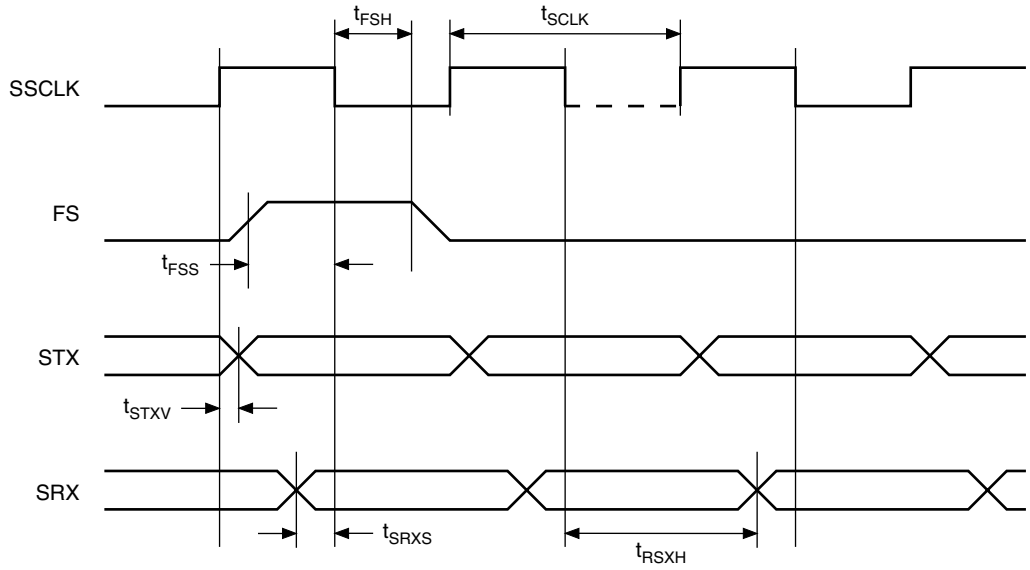


Table 12. FS and SCLK as Inputs Timings

Symbol	Parameter	Min (ns)	Max (ns)
t_{FSS}	FS Setup before RX Edge of SSCLK	75.0	–
t_{FSH}	FS Hold after First RX Edge of SSCLK	0	–
t_{STXV}	STX Valid after TX Edge of SSCLK	50.0	80.0
t_{SRXS}	SRX Setup before RX Edge of SSCLK	25.0	–
t_{RSXH}	SRX Hold after RX Edge of SSCLK	25.0	–
t_{SCLK}	SSCLK Input Period	200.0	–

Packaging Information

Figure 14. SQFP Package Drawing

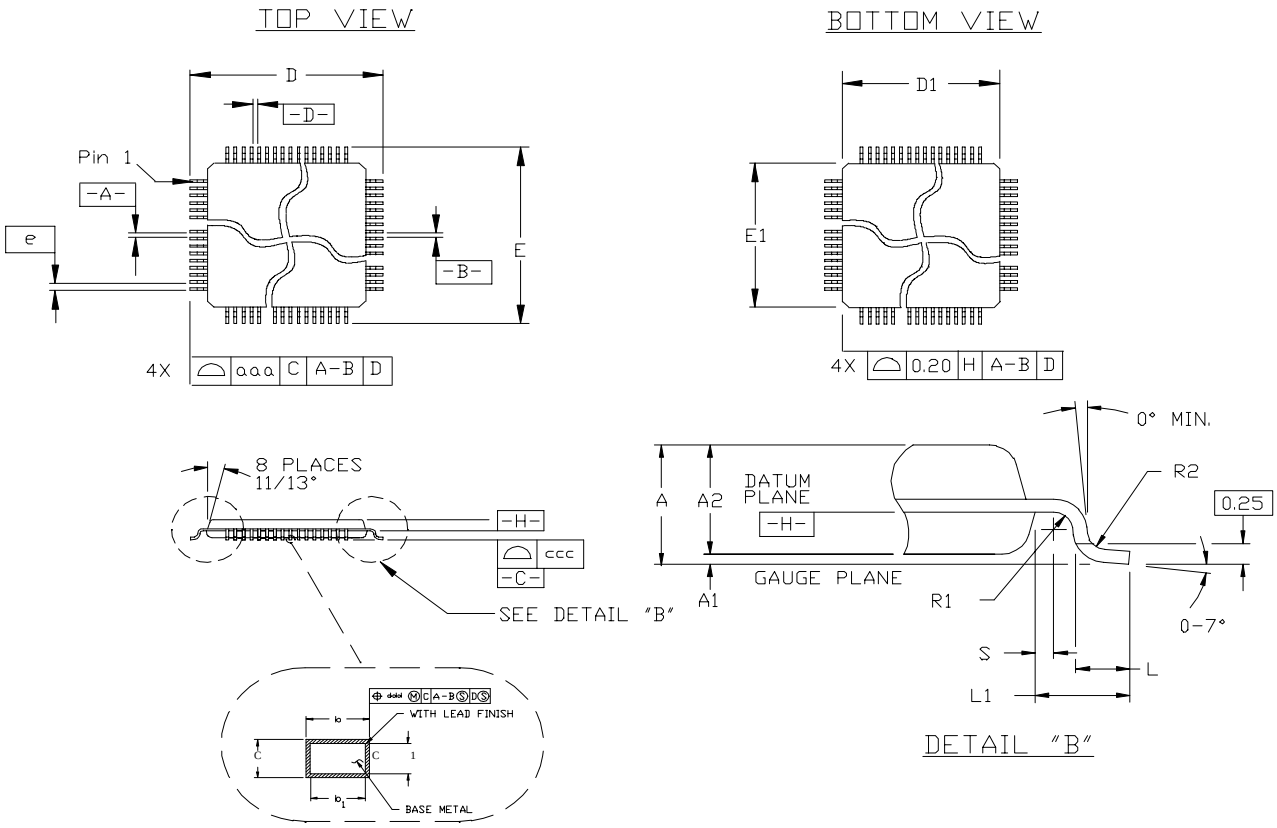


Table 13. Package Dimensions for 160-lead SQFP Package (mm)

Symbol	Min	Nom	Max	Symbol	Min	Nom	Max
c	0.11		0.23	A	4.10		
c1	0.11	0.15	0.19	A1	0.25		0.50
L	0.65	0.88	1.03	A2	3.20	3.40	3.60
L1		1.60 REF		b	0.29		0.45
R2	0.13		0.3	b1	0.29	0.35	0.41
R1	0.13			D		31.20	
S	0.4			D1		28.00	
Tolerances of Form and Position				E		31.20	
aaa		0.25		E1		28.00	
ccc			0.1	e		0.65	
				ddd		0.12	

Thermal Resistance

Thermal Resistance = 33C°/W

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
20	3.3V	AT75C310-Q160	PQFP160	Commercial (0° to 70°C)

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe
Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686-677
FAX (44) 1276-686-697

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Fax-on-Demand
North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

BBS
1-(408) 436-4309

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