NEC

MOS INTEGRATED CIRCUIT
μPD16818

MONOLITHIC DUAL H BRIDGE DRIVER CIRCUIT

DESCRIPTION

The μPD16818 is a monolithic dual H bridge driver IC which uses N-channel power MOS FETs in its output stage. By employing the power MOS FETs for the output stage, this driver circuit has a substantially improved saturation voltage and power consumption as compared with conventional driver circuits that use bipolar transistors.

In addition, the drive current can be adjusted by an external resistor in power-saving mode.

The μPD16818 is therefore ideal as the driver circuit of a 2-phase excitation, bipolar-driven stepping motor for the head actuator of an FDD.

FEATURES

- Compatible with 3V-/5V- supply voltage
- Pin compatible with μPD16803
- Low ON resistance (sum of ON resistors of top and bottom MOS FETs)
  R_{ON1}= 1.2 Ω (V_M = 3.0 V)
  R_{ON2} = 1.0 Ω (V_M = 5.0 V)
- Low current consumption: I_{DD} = 0.4 mA TYP. (V_{DD} = 2.7 V to 3.6 V)
- Stop mode function that turns OFF all output MOS FETs
- Drive current can be set in power-saving mode (set by external resistor)
- Compact surface mount package

ORDERING INFORMATION

Part Number	Package
μPD16818GS	20-pin plastic SOP (7.62 mm (300))

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter		Symbol	Condition	Rating	Unit
Supply voltage	Motor block	V_M		–0.5 to +7.0	V
	Control block	V_{DD}		–0.5 to +7.0	
Power consumption	μPD16818GS	P_{D1}		1.0 Note 1	W
		P_{D2}		1.25 Note 2	
Instantaneous H bridge drive current		$I_{D(pulse)}$	PW ≤ 5 ms, Duty ≤ 40 %	±1.0 Note 2	A
Input voltage		V_{IN}		–0.5 to V_{DD} + 0.5	V
Operating temperature range		T_A		0 to 60	°C
Operation junction temperature		$T_{J(MAX)}$		150	°C
Storage temperature range		T_{stg}		–55 to +150	°C

Notes 1. IC only

2. When mounted on a glass epoxy printed circuit board (100 mm × 100 mm × 1 mm)

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RECOMMENDED OPERAING CONDITIONS

Parameter			Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	Motor block		V_M	2.7		6.0	V
	Control block		V_{DD}	2.7		6.0	
Rx pin connection resistance			R_X	2			kΩ
H bridge drive current (V_{DD} = V_M = 3 V)**Note**		μPD16818GS	I_{DR}			430	mA
Charge pump capacitor capacitance			C_1-C_3	5		20	nF
Operating temperature			T_A	0		60	°C

Note When mounted on a glass epoxy printed circuit board (100 mm × 100 mm × 1 mm)

ELECTRICAL SPECIFICATIONS (Within recommended operating conditions unless otherwise specified)

V_{DD} = V_M = 4.0 V to 6.0 V

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
OFF V_M pin current	I_M	INC pin low V_M = V_{DD} = 6 V			1.0	μA
V_{DD} pin current	I_{DD}	**Note 1**		1.0	2.0	mA
High-level input current	I_{IH1}	T_A = 25 °C, V_{IN} = V_{DD}			1.0	μA
(IN_1, IN_2, INC)		0 ≤ T_A ≤ 60 °C, V_{IN} = V_{DD}			2.0	
Low-level input current	I_{IL1}	T_A = 25 °C, V_{IN} = 0			–0.15	mA
(IN_1, IN_2, INC)		0 ≤ T_A ≤ 60 °C, V_{IN} = 0			–0.2	
PS pin high-level input current	I_{IH2}	T_A = 25 °C, V_{IN} = V_{DD}			0.15	mA
		0 ≤ T_A ≤ 60 °C, V_{IN} = V_{DD}			0.2	
PS pin low-level input voltage	I_{IL2}	T_A = 25 °C, V_{IN} = 0			–1.0	μA
		0 ≤ T_A ≤ 60 °C, V_{IN} = 0			–2.0	
Input pull-up resistance	R_{INU}	T_A = 25 °C	35	50	65	kΩ
(IN_1, IN_2, INC)		0 ≤ T_A ≤ 60 °C	25		75	
PS pin input pull-down resistance	R_{IND}	T_A = 25 °C	35	50	65	kΩ
		0 ≤ T_A ≤ 60 °C	25		75	
Control pin high-level input voltage	V_{IH}		3.0		V_{DD} + 0.3	V
Control pin low-level input voltage	V_{IL}		–0.3		0.8	V
H bridge ON resistance**Note 2**	R_{ON2}	V_{DD} = V_M = 5 V		1.0	2.0	Ω
R_{ON} relative accuracy	ΔR_{ON}	Excitation direction <1>, <3>			±15	%
		Excitation direction <2>, <4>**Note 3**			±5	
Charge pump circuit turn ON time	t_{ONG}	V_{DD} = V_M = 5 V C_1 = C_2 = C_3 = 10nF R_M = 20 Ω		0.3	2.0	ms
H bridge turn ON time	t_{ONH}				2.0	μs
H bridge turn OFF time	t_{OFFH}				5.0	μs

Notes 1. When IN_1 = IN_2 = INC = "H", PS = "L"

2. Sum of ON resistances of top and bottom MOS FETs

3. For the excitation direction, refer to **FUNCTION TABLE**.

ELECTRICAL SPECIFICATIONS (Within recommended operating conditions unless otherwise specified)

V_{DD} = V_M = 2.7 V to 3.6 V

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
OFF V_M pin current	I_M	INC pin low V_M = V_{DD} = 3.6 V			1.0	μA
V_{DD} pin current	I_{DD}	**Note 1**		0.4	1.0	mA
High-level input current	I_{IH1}	T_A = 25 °C, V_{IN} = V_{DD}			1.0	μA
(IN_1, IN_2, INC)		0 ≤ T_A ≤ 60 °C, V_{IN} = V_{DD}			2.0	
Low-level input current	I_{IL1}	T_A = 25 °C, V_{IN} = 0			–0.09	mA
(IN_1, IN_2, INC)		0 ≤ T_A ≤ 60 °C, V_{IN} = 0			–0.12	
PS pin high-level input current	I_{IH2}	T_A = 25 °C, V_{IN} = V_{DD}			0.09	mA
		0 ≤ T_A ≤ 60 °C, V_{IN} = V_{DD}			0.12	
PS pin low-level input voltage	I_{IL2}	T_A = 25 °C, V_{IN} = 0			–1.0	μA
		0 ≤ T_A ≤ 60 °C, V_{IN} = 0			–2.0	
Input pull-up resistance	R_{INU}	T_A = 25 °C	35	50	65	kΩ
(IN_1, IN_2, INC)		0 ≤ T_A ≤ 60 °C	25		75	
PS pin input pull-down resistance	R_{IND}	T_A = 25 °C	35	50	65	kΩ
		0 ≤ T_A ≤ 60 °C	25		75	
Control pin high-level input voltage	V_{IH}		2.0		V_{DD} + 0.3	V
Control pin low-level input voltage	V_{IL}		–0.3		0.8	V
H bridge ON resistance**Note 2**	R_{ON1}	V_{DD} = V_M = 3 V		1.2	2.4	Ω
R_{ON} relative accuracy	ΔR_{ON}	Excitation direction <1>, <3>			±15	%
		Excitation direction <2>, <4>**Note 3**			±5	
Vx voltage in power-saving mode**Note 4**	V_X	V_{DD} = V_M = 3 V R_X = 270 kΩ	1.0	1.2	1.4	V
Vx relative accuracy in power-saving mode	ΔV_X	Excitation direction <1>, <3>			±5	%
		Excitation direction <2>, <4>			±5	
Charge pump circuit turn ON time	t_{ONG}	V_{DD} = V_M = 3 V		0.3	2.0	ms
H bridge turn ON time	t_{ONH}	C_1 = C_2 = C_3 = 10nF			2.0	μs
H bridge turn OFF time	t_{OFFH}	R_M = 20 Ω			5.0	μs

Notes 1. When IN_1 = IN_2 = INC = “H”, PS = “L”

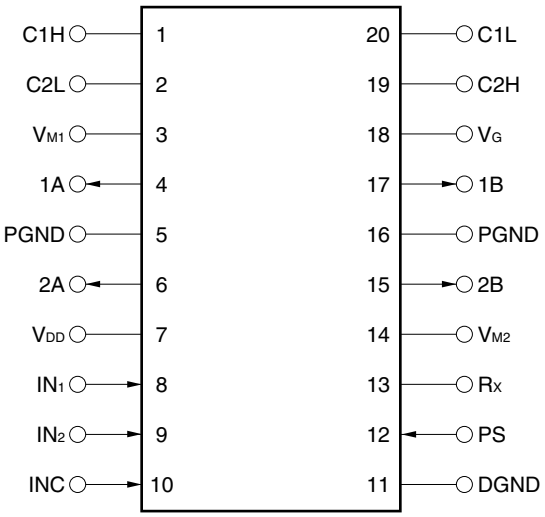
2. Sum of ON resistances of top and bottom MOS FETs

3. For the excitation direction, refer to **FUNCTION TABLE**.

4. Vx is a voltage at point A (FORWARD) or B (REVERSE) of the H bridge in FUNCTION TABLE.

PIN CONFIGURATION (Top View)

20-pin plastic SOP (7.62 mm (300))

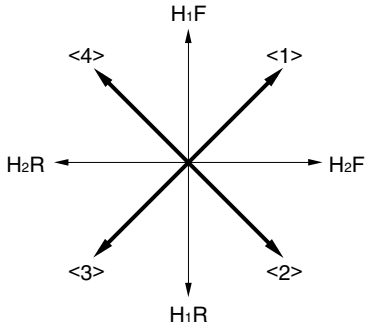


FUNCTION TABLE

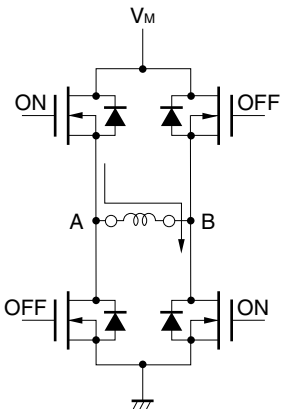
Excitation Direction	INC	IN1	IN2	H1	H2
<1>	H	H	H	F	F
<2>	H	L	H	R	F
<3>	H	L	L	R	R
<4>	H	H	L	F	R
–	L	×	×	Stop	

F: FORWARD

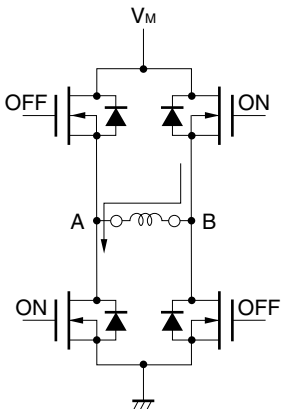
R: REVERSE



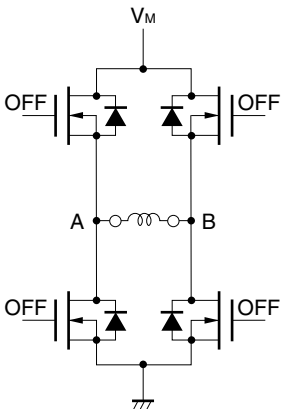
FORWARD



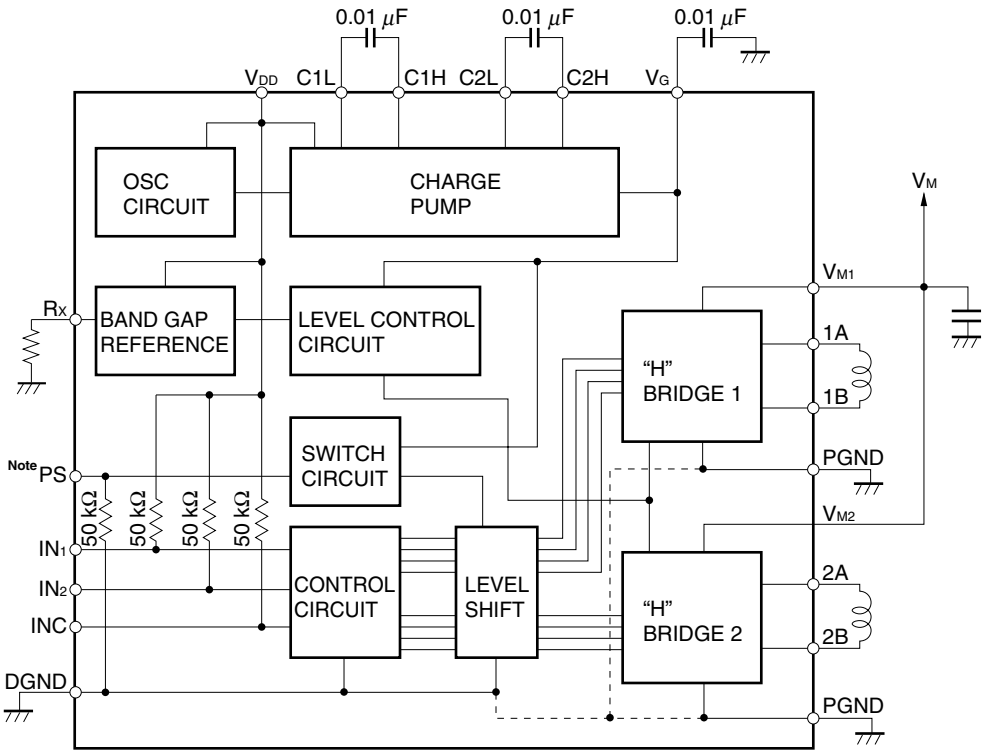
REVERSE



STOP



BLOCK DIAGRAM

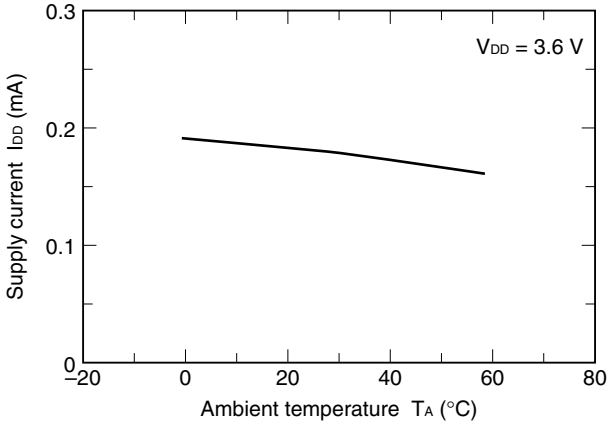


Note The power-saving mode is set when the PS pin goes high. In this mode, the voltage of the charge pump circuit is lowered and the ON resistance of the H bridge driver transistor increases, limiting the current.

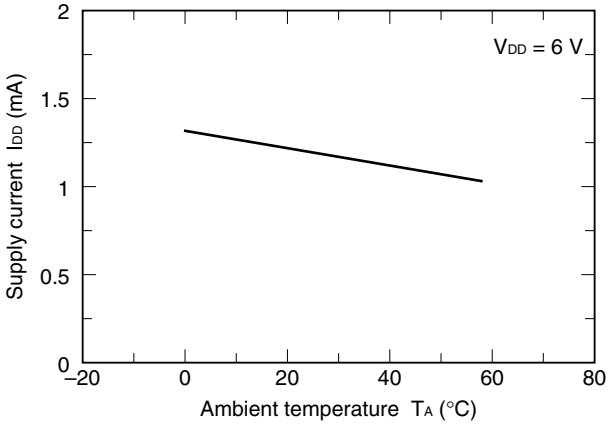
Remark ------ is connected in diffusion layer.

CHARACTERISTIC CURVES

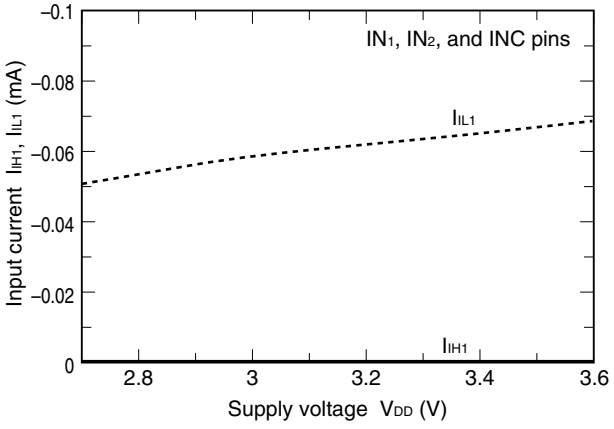
I_{DD} vs. T_A Characteristics



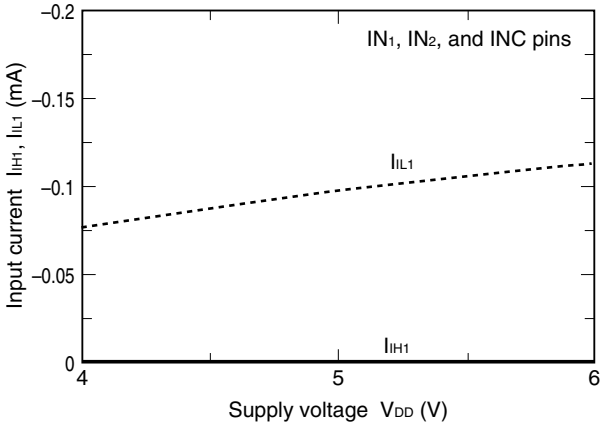
I_{DD} vs. T_A Characteristics



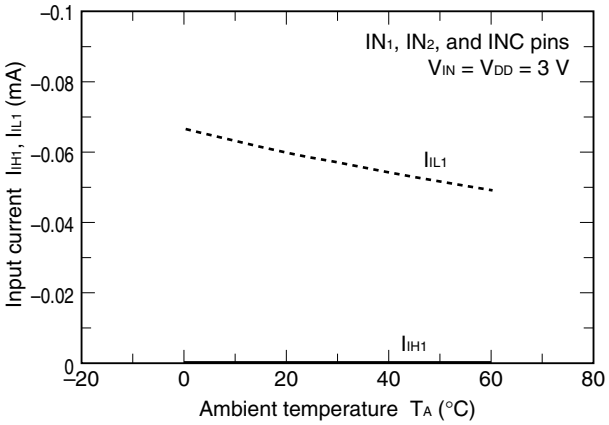
I_{IHL1} vs. V_{DD} Characteristics



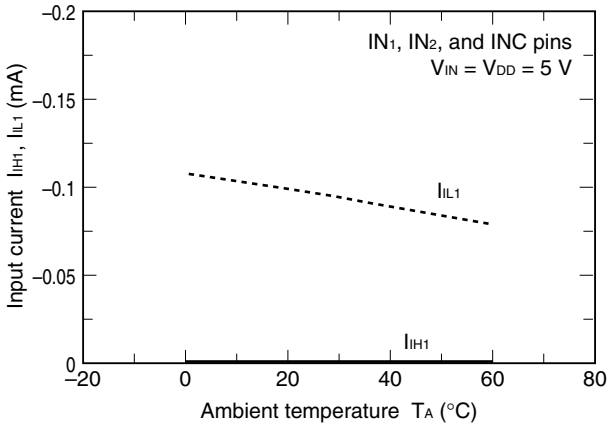
I_{IHL1} vs. V_{DD} Characteristics



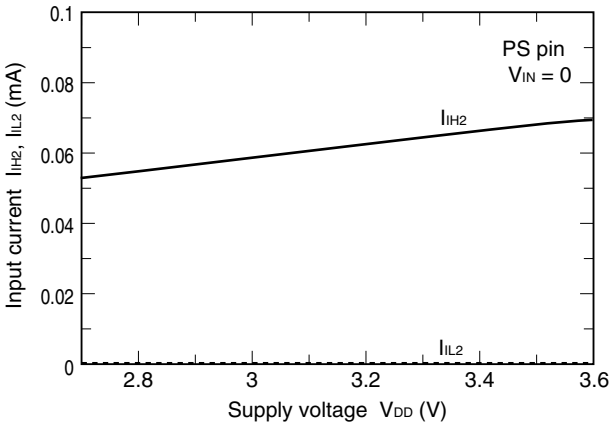
I_{IHL1} vs. T_A Characteristics



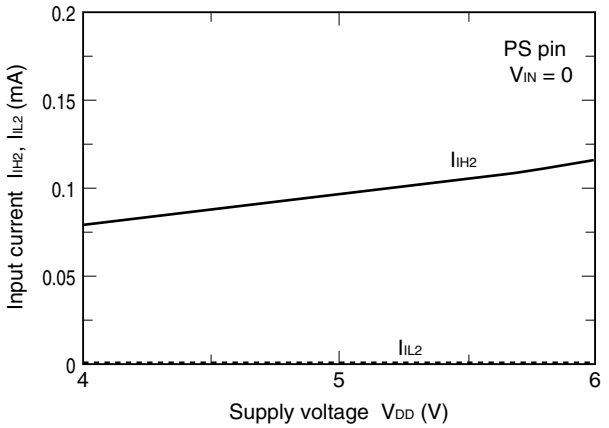
I_{IHL1} vs. T_A Characteristics



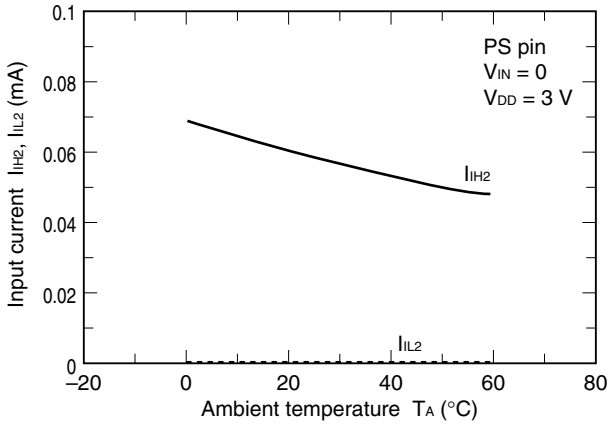
I_{IHL2} vs. V_{DD} Characteristics



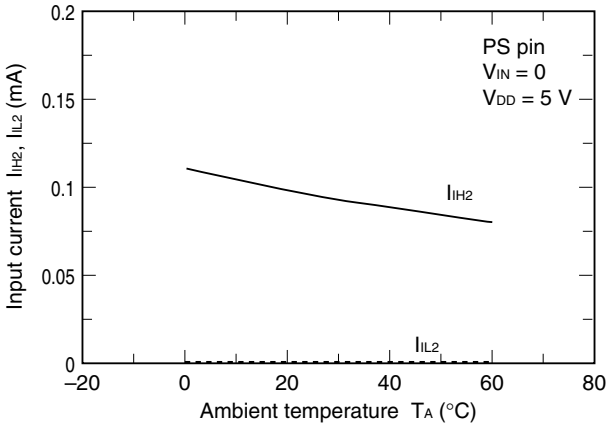
I_{IHL2} vs. V_{DD} Characteristics



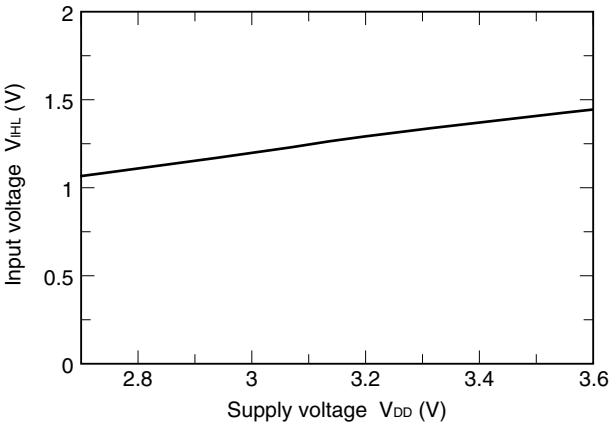
I_{IHL2} vs. T_A Characteristics



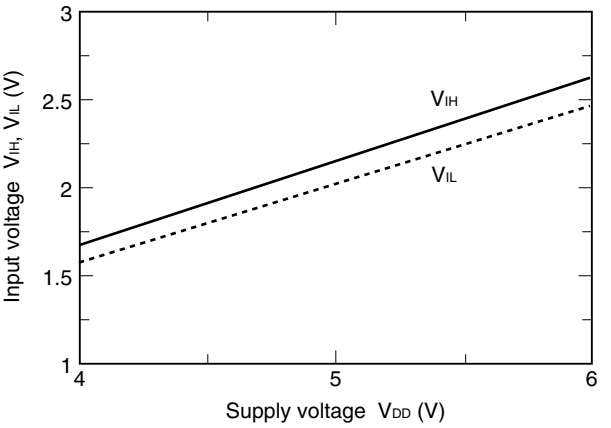
I_{IHL2} vs. T_A Characteristics



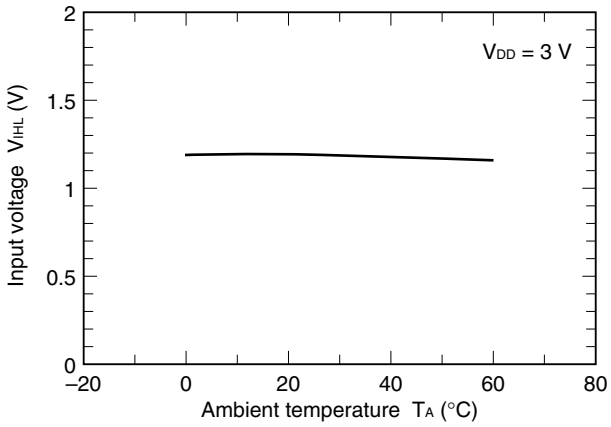
V_{IHL} vs. V_{DD} Characteristics



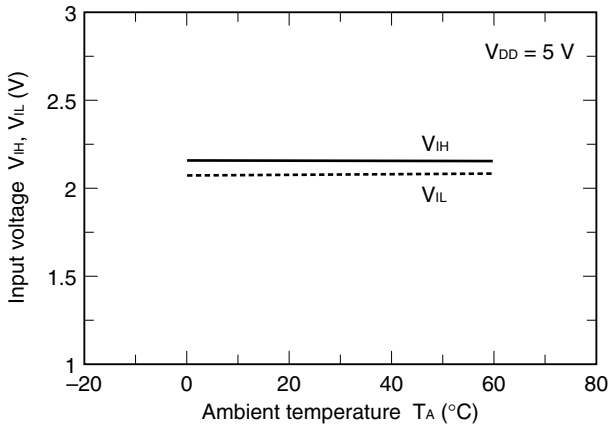
V_{IHL} vs. V_{DD} Characteristics



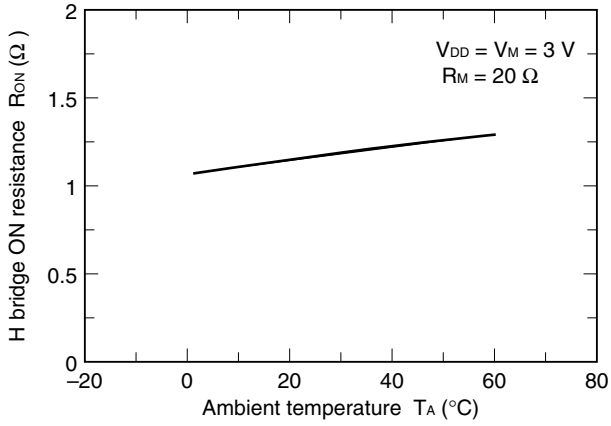
V_{IHL} vs. T_A Characteristics



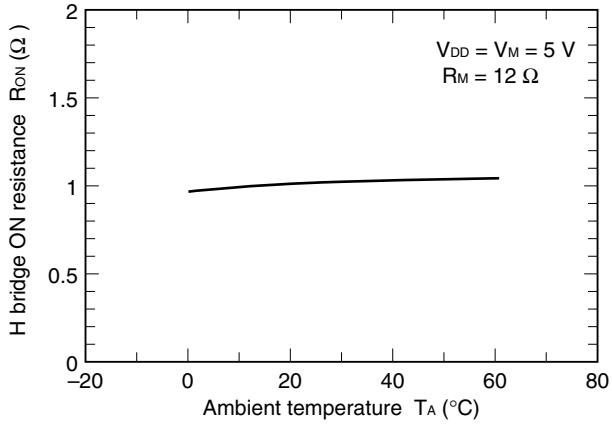
V_{IHL} vs. T_A Characteristics



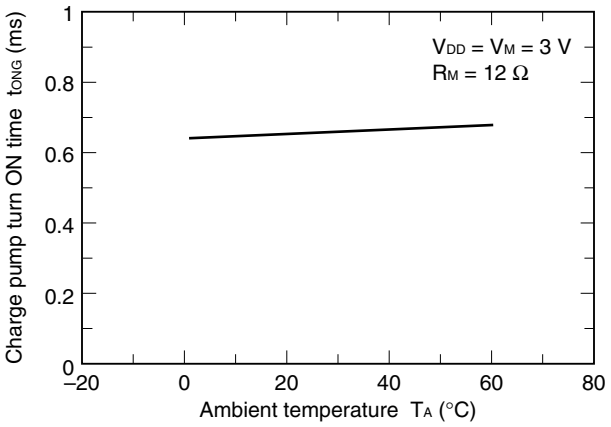
R_{ON} vs. T_A Characteristics



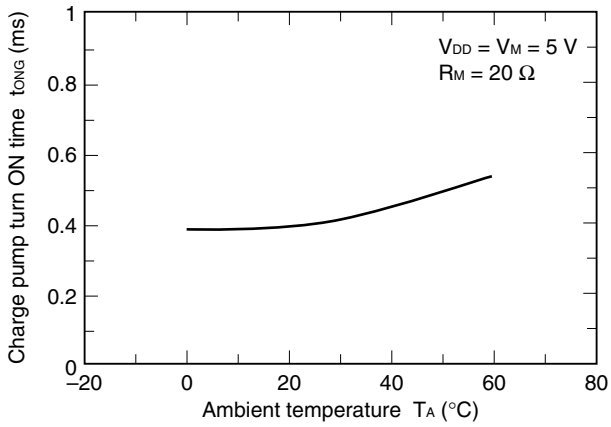
R_{ON} vs. T_A Characteristics



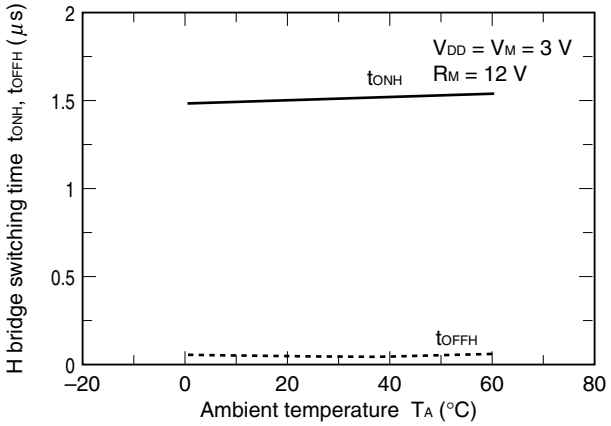
tONG vs. TA Characteristics



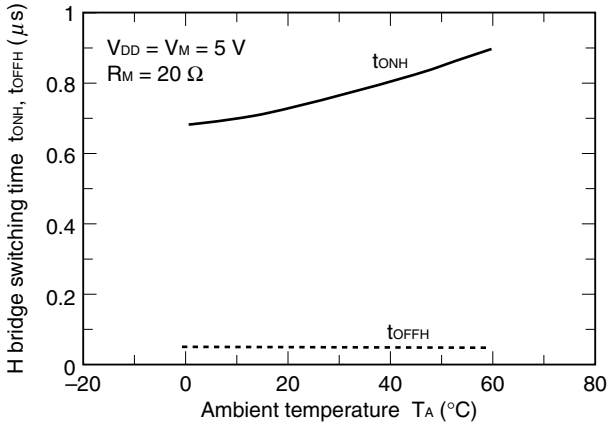
tONG vs. TA Characteristics



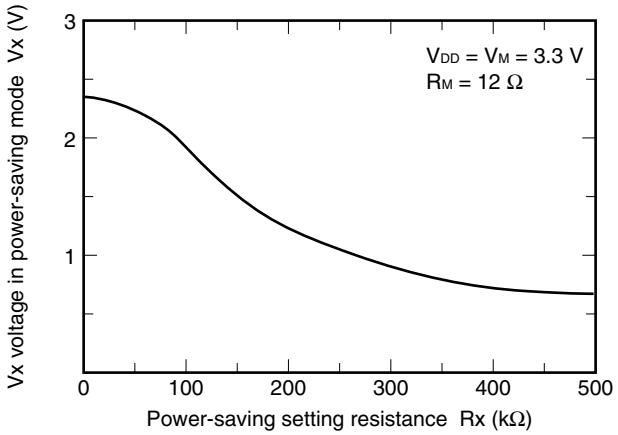
tONH, tOFFH vs. TA Characteristics



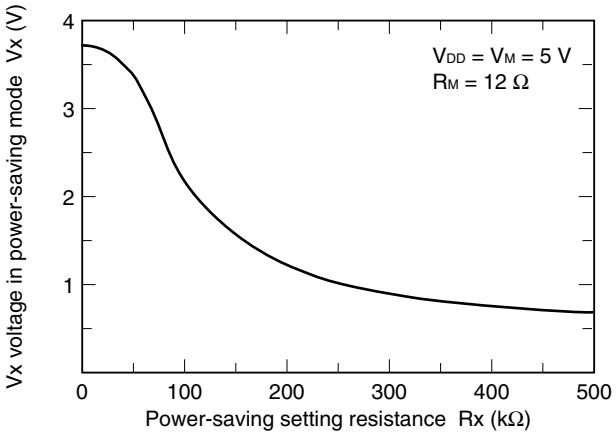
tONH, tOFFH vs. TA Characteristics



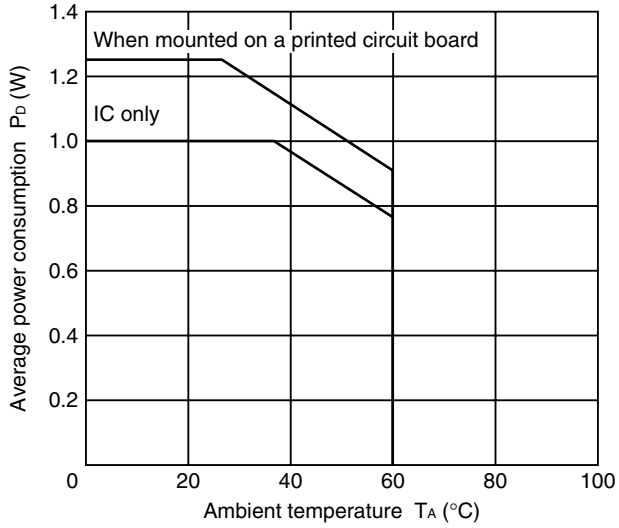
Vx vs. Rx Characteristics



Vx vs. Rx Characteristics

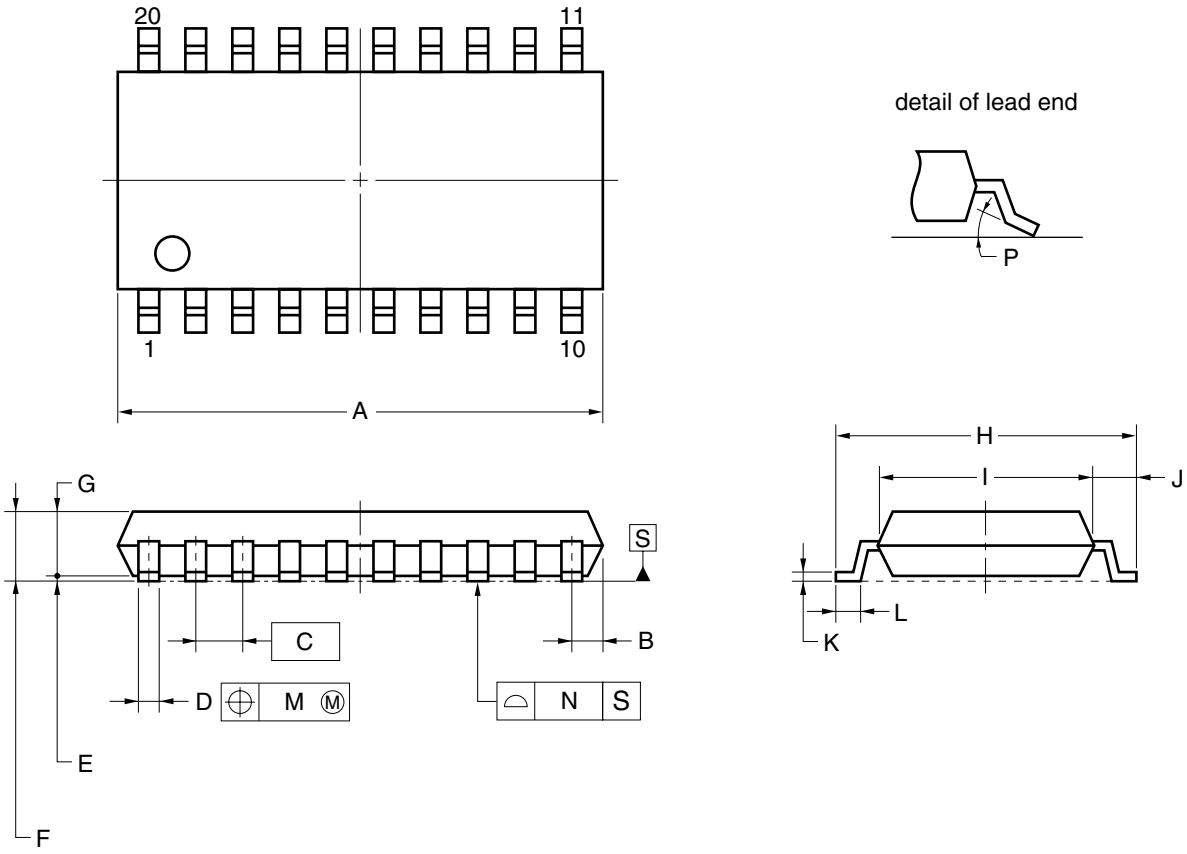


PD vs. TA Characteristics (μPD16818GS)



PACKAGE DRAWING

20-PIN PLASTIC SOP (7.62 mm (300))



NOTE

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	12.7±0.3
B	0.78 MAX.
C	1.27 (T.P.)
D	$0.42^{+0.08}_{-0.07}$
E	0.1±0.1
F	1.8 MAX.
G	1.55±0.05
H	7.7±0.3
I	5.6±0.2
J	1.1
K	$0.22^{+0.08}_{-0.07}$
L	0.6±0.2
M	0.12
N	0.10
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P20GM-50-300B, C-7

RECOMMENDED SOLDERING CONDITIONS

The μPD16818 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Surface Mount Type

μPD16818GS 20-pin plastic SOP (7.62 mm (300))

Soldering Method	Soldering Conditions	Symbol of Recommended Soldering
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds MAX.(210°C MIN.), Number of times: 3 MAX., Number of days: None[Note], Flux: Rosin-based flux with little chlorine component (chlorine: 0.2 Wt% MAX.)	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 seconds MAX.(200°C MIN.), Number of times: 3 MAX., Number of days: None[Note], Flux: Rosin-based flux with little chlorine component (chlorine: 0.2 Wt% MAX.)	VP15-00-3
Wave soldering	Package peak temperature: 260°C, Time: 10 seconds MAX., Preheating temperature: 120 °C MAX., Number of times: 1, Flux: Rosin-based flux with little chlorine component (chlorine: 0.2 Wt% MAX.)	WS60-00-1

Note Number of days in storage after the dry pack has been opened. The storage conditions are at 25 °C, 65 % RH MAX.

Caution Do not use two or more soldering methods in combination.

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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