DATA SHEET

PTN3500
Maintenance and control device

Product specification
Supersedes data of 2000 Nov 22

2001 Jan 17

Philips
Semiconductors

PHILIPS

Maintenance and control device PTN3500

FEATURES

- I^2C to parallel port expander
- Internal 256x8 E^2PROM
- Self timed write cycle (5 ms typ.)
- Four byte page write operation
- Controlled pull-up on address lines
- Low voltage V_{CC} range of +2.5 V to +3.6 V
- 5 V – tolerant I/Os
- Low standby current (< 60 μA)
- Power on Reset
- Supports Live Insertion
- Compatible with SMBus specification version 1.1
- High E^2PROM endurance and data retention
- Available in SO16 and TSSOP16 package options

PIN CONFIGURATION

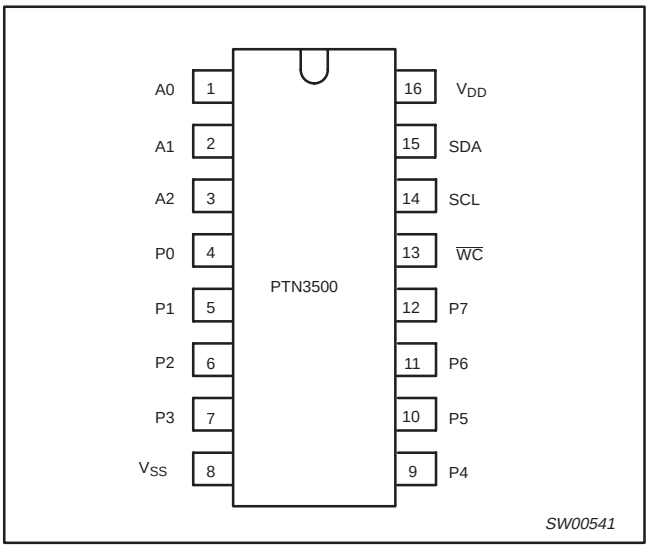


Figure 1.

DESCRIPTION

The PTN3500 is a general purpose maintenance and control device. It features an on-board E^2PROM that can be used to store error codes or board manufacturing data for read–back by application software for diagnostic purposes.

The eight quasi bidirectional data pins can be independently assigned as inputs or outputs to monitor board level status or activate indicator devices such as LEDs.

The PTN3500 has three address pins allowing up to 8 devices to share the common two wire I^2C software protocol serial data bus.

The PTN3500 supports live insertion to facilitate usage in removable cards on backplane systems.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1,2,3	A0:2	Address Lines
4,5,6,7	P0:3	Quasi–bidirectional i/o pins
8	V_{SS}	Supply Ground
9,10,11,12	P4:7	Quasi–bidirectional i/o pins
13	$\overline{WC}$	Write Control Pin. Should be tied LOW.
14	SCL	I^2C Serial Clock
15	SDA	I^2C Serial Data
16	V_{DD}	Supply Voltage

ORDERING INFORMATION

Type number	Package		
	Name	Description	Version
PTN3500D	SO16	Plastic small-outline package; 16 leads; body width 7.5 mm	SOT162-1
PTN3500DH	TSSOP16	Plastic thin shrink small-outline package; 16 leads; body width 4.4 mm	SOT403-1

FUNCTIONAL DIAGRAM

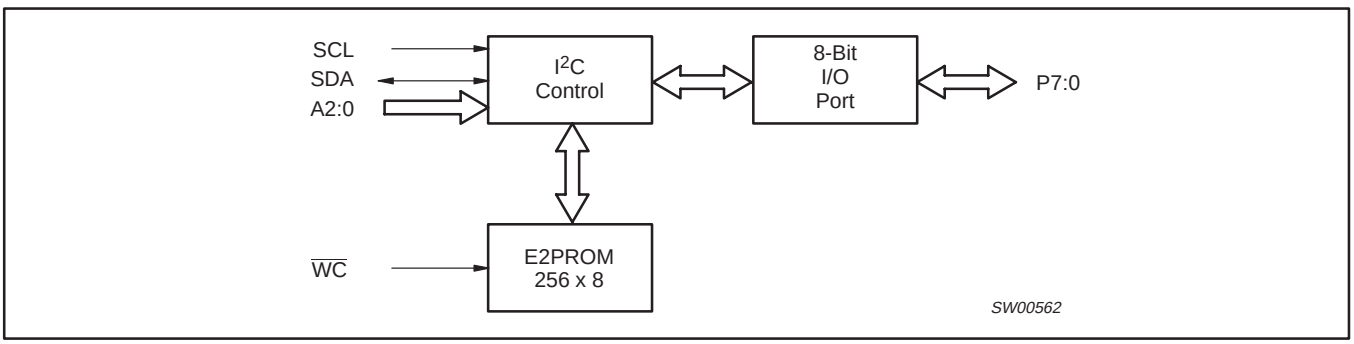


Figure 2.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock phase. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (See Figure 3).

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Figure 4).

System configuration

A device generating a message is a “transmitter”, a device receiving is the “receiver”. The device that controls the message is the “master” and the devices which are controlled by the master are the “slaves” (see Figure 5).

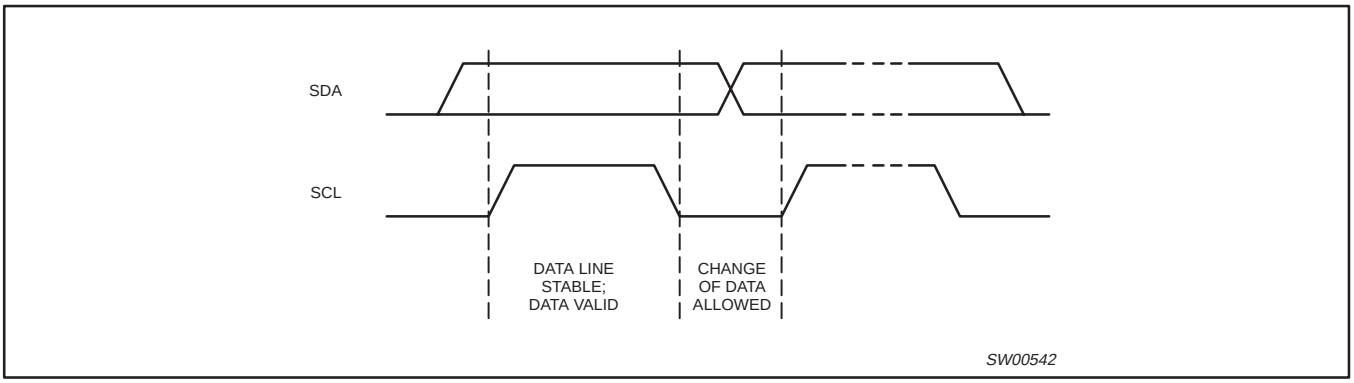


Figure 3. Bit transfer

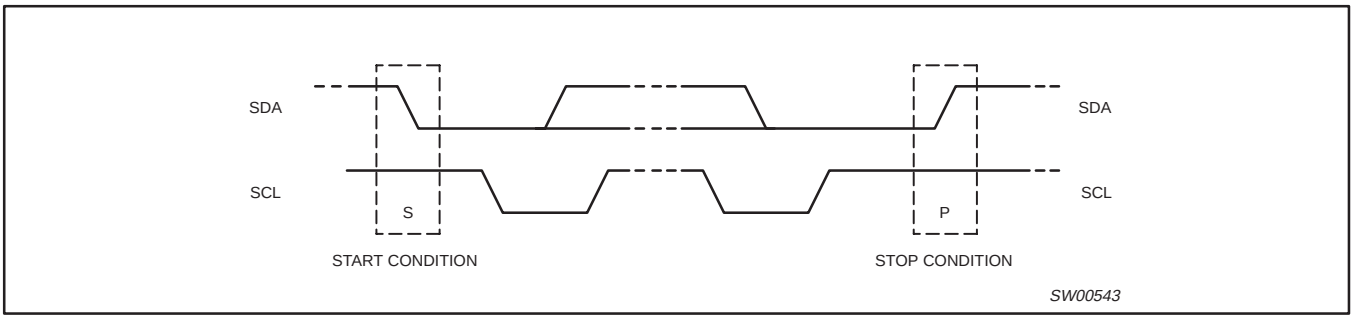


Figure 4. Definition of start and stop conditions

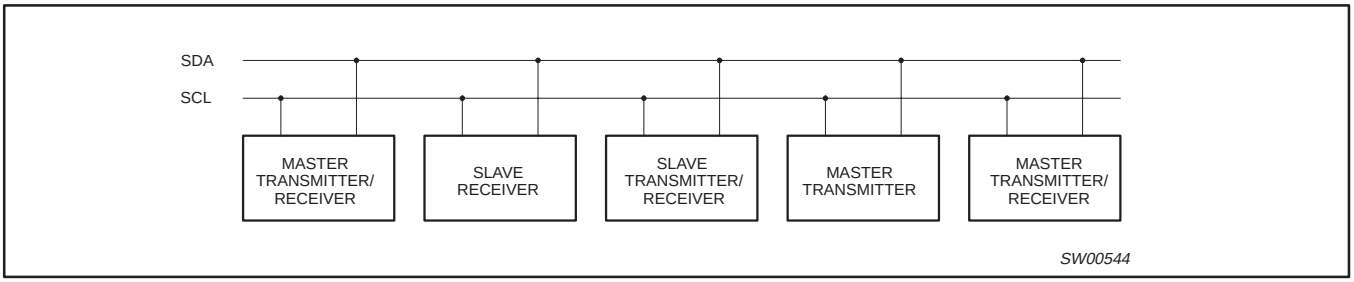


Figure 5. System configuration

Acknowledge (see Figure 6)

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set–up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

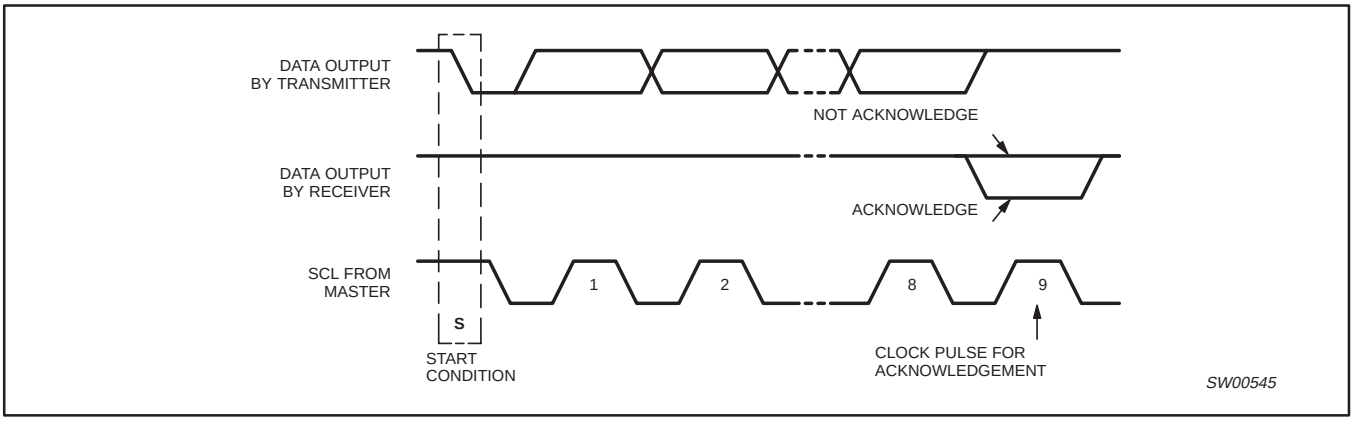


Figure 6. Acknowledgment on the I^2C-bus

FUNCTIONAL DESCRIPTION

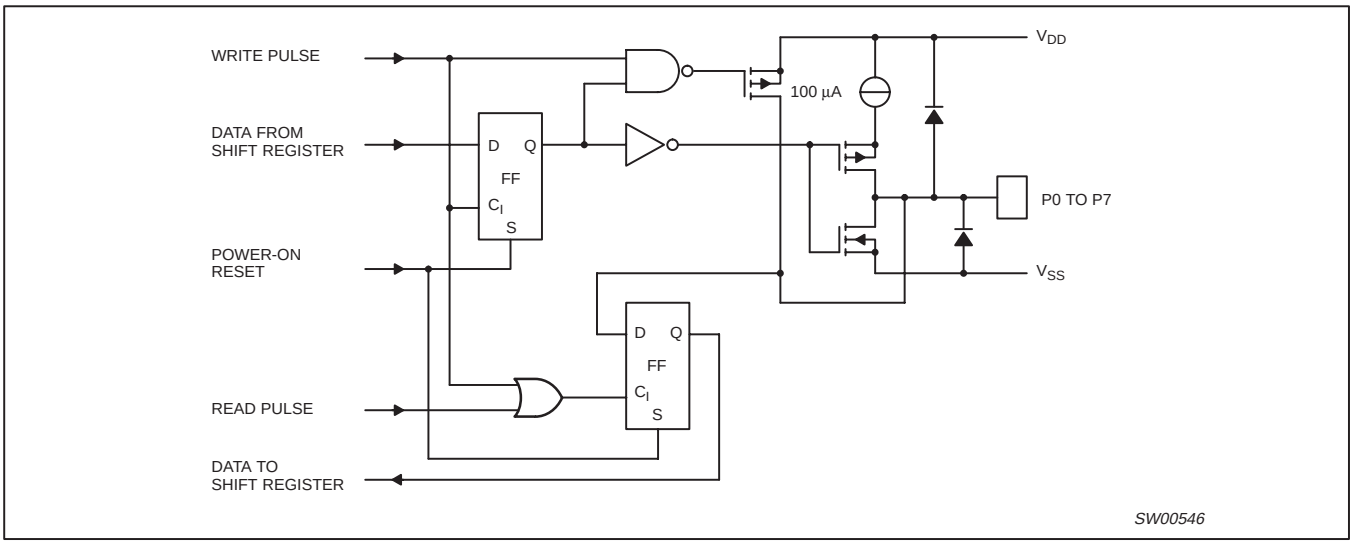


Figure 7. Simplified schematic diagram of each I/O

Addressing

For addressing, see Figure 8.

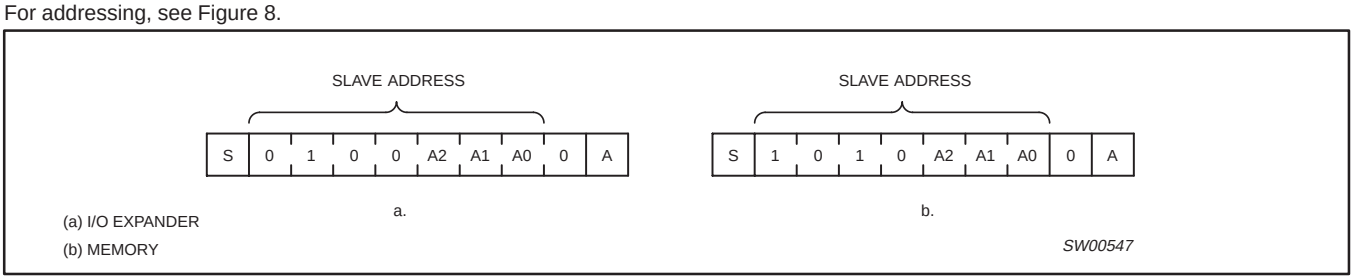


Figure 8. PTN3500 slave addresses

Asynchronous Start

Following any Start condition on the bus, a minimum of 9 SCL clock cycles must be completed before a Stop condition can be issued. The device does not support a Stop or a repeated Start condition during this time period.

I/O OPERATIONS (see also Figure 7)

Each of the PTN3500's eight I/Os can be independently used as an input or output. Input I/O data is transferred from the port to the microcontroller by the READ mode (See Figure 10). Output data is transmitted to the port by the I/O WRITE mode (see Figure 9).

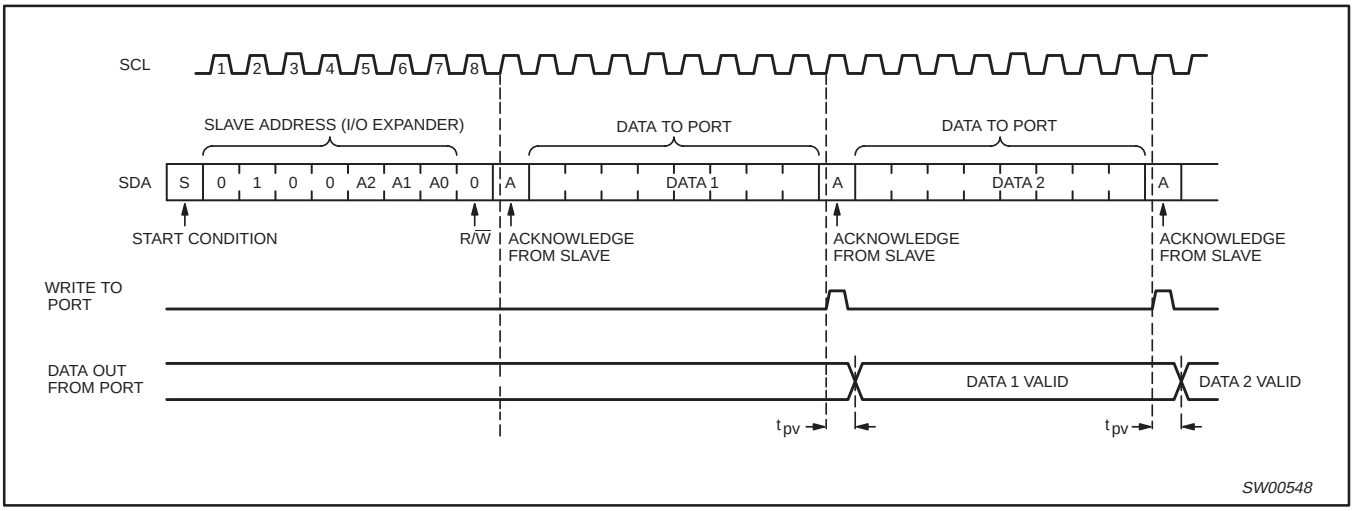


Figure 9. I/O WRITE mode (output)

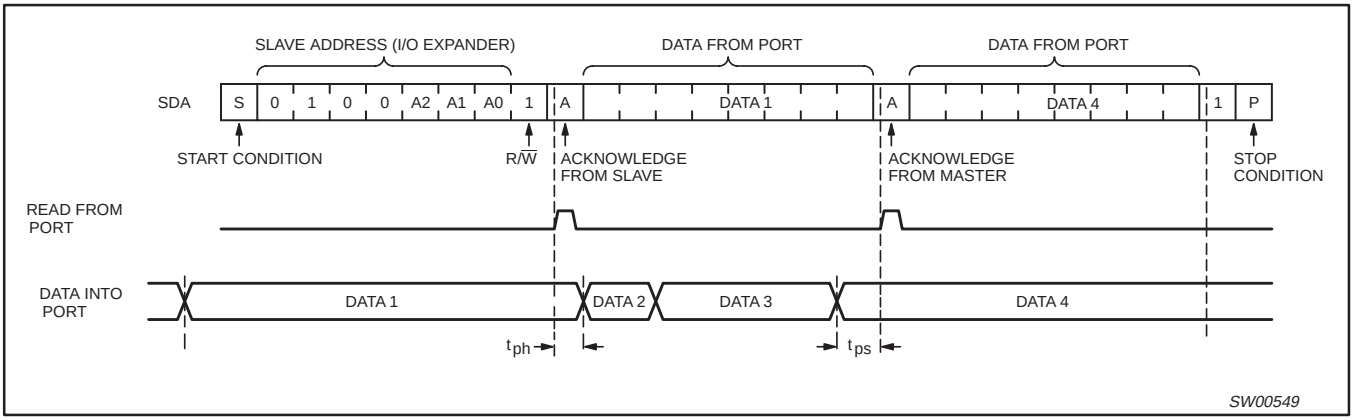


Figure 10. I/O READ mode (input)

Quasi-bidirectional I/Os (see Figure 11)

A quasi-bidirectional I/O can be used as an input or output without the use of a control signal for data direction. At power-on the I/Os are HIGH. In this mode, only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The I/Os should be HIGH before being used as inputs.

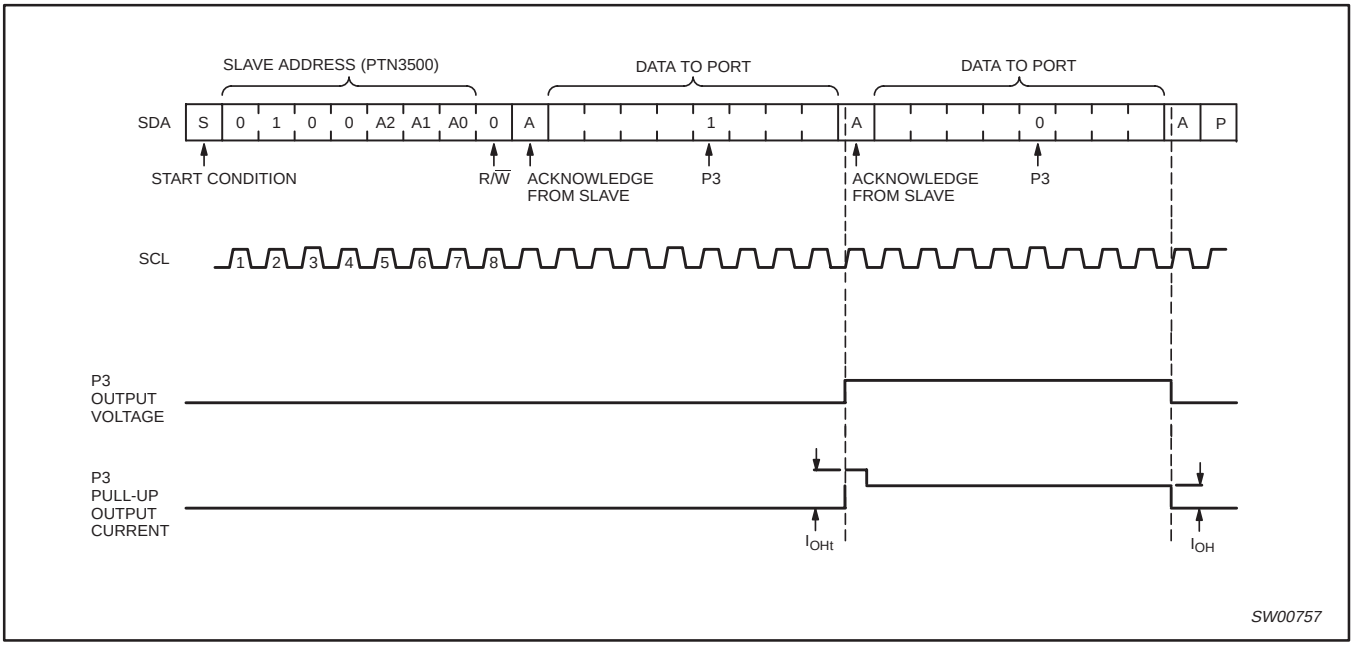


Figure 11. Transient pull-up current I_{OHt} while P3 changes from LOW-to-HIGH and back to LOW

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{pv}	Output data valid; $C_L \leq 100$ pF			4	µs
t_{ps}	Input data setup time; $C_L \leq 100$ pF	0			µs
t_{ph}	Input data hold time; $C_L \leq 100$ pF	4			µs

MEMORY OPERATIONS

Write operations

Write operations require an additional address field to indicate the memory address location to be written. The address field is eight bits long, providing access to any one of the 256 words of memory. There are two types of write operations, byte write and page write.

Byte Write (see Figure 12)

To perform a byte write the start condition is followed by the memory slave address and the R/$\overline{W}$ bit set to 0. The PTN3500 will respond with an acknowledge and then consider the next eight bits sent as the word address and the eight bits after the word address as the data. The PTN3500 will issue an acknowledge after the receipt of both the word address and the data. To terminate the data transfer the master issues the stop condition, initiating the internal write cycle to the non-volatile memory. Only write and read operations to the Quasi-bidirectional I/O are allowed during the internal write cycle.

Page Write (see Figure 13)

A page write is initiated in the same way as the byte write. If after sending the first word of data, the stop condition is not received the PTN3500 considers subsequent words as data. After each data word the PTN3500 responds with an acknowledge and the two least significant bits of the memory address field are incremented. Should the master not send a stop condition after four data words the address counter will return to its initial value and overwrite the data previously written. After the receipt of the stop condition the inputs will behave as with the byte write during the internal write cycle.

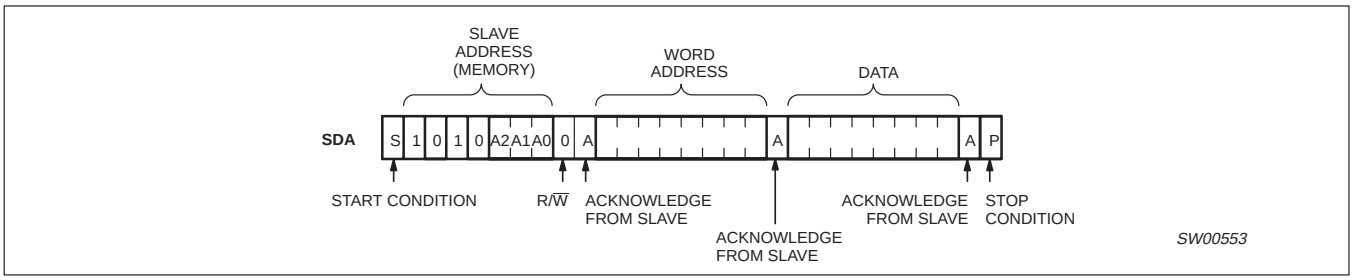


Figure 12. Byte write

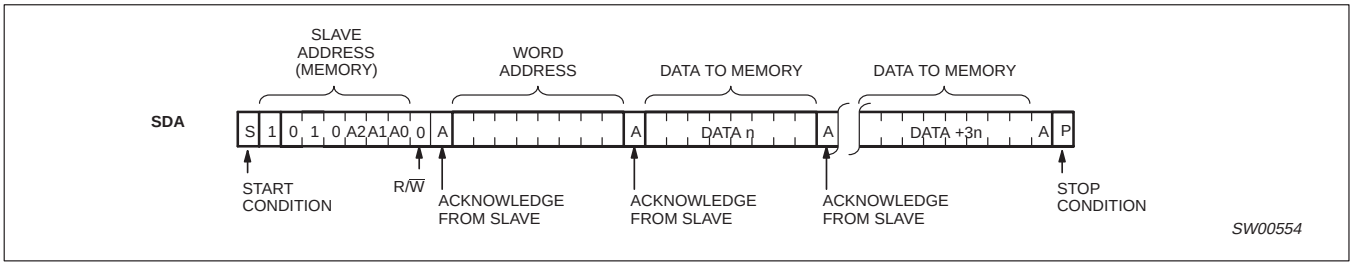


Figure 13. Page Write

Read operations

PTN3500 read operations are initiated in an identical manner to write operations with the exception that the memory slave address' R/$\overline{W}$ bit is set to a one. There are three types of read operations; current address, random and sequential.

Current Address Read (see Figure 14)

The PTN3500 contains an internal address counter that increments after each read or write access, as a result if the last word accessed was at address n then the address counter contains the address n+1.

When the PTN3500 receives its memory slave address with the R/$\overline{W}$ bit set to one it issues an acknowledge and uses the next eight clocks to transmit the data contained at the address stored in the address counter. The master ceases the transmission by issuing the stop condition after the eighth bit. There is no ninth clock cycle for the acknowledge.

Random Read (see Figure 15)

The PTN3500's random read mode allows the address to be read from to be specified by the master. This is done by performing a dummy write to set the address counter to the location to be read.

The master must perform a byte write to the address location to be read, but instead of transmitting the data after receiving the acknowledge from the PTN3500 the master reissues the start condition and memory slave address with the R/$\overline{W}$ bit set to one. The PTN3500 will then transmit an acknowledge and use the next eight clock cycles to transmit the data contained in the addressed location. The master ceases the transmission by issuing the stop condition after the eighth bit, omitting the ninth clock cycle acknowledge.

Sequential Read (see Figure 16)

The PTN3500 sequential read is an extension of either the current address read or random read. If the master doesn't issue a stop condition after it has received the eighth data bit, but instead issues an acknowledge, the PTN3500 will increment the address counter and use the next eight cycles to transmit the data from that location. The master can continue this process to read the contents of the entire memory. Upon reaching address 255 the counter will return to address 0 and continue transmitting data until a stop condition is received. The master ceases the transmission by issuing the stop condition after the eighth bit, omitting the ninth clock cycle acknowledge.

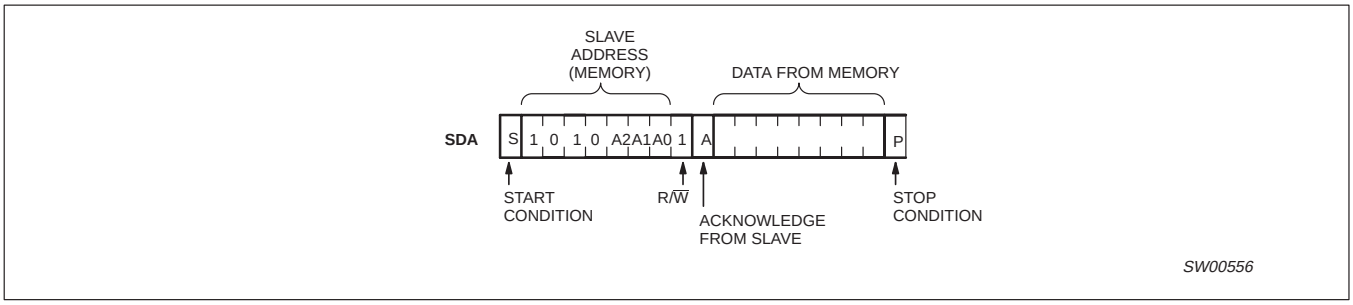


Figure 14. Current Address Read

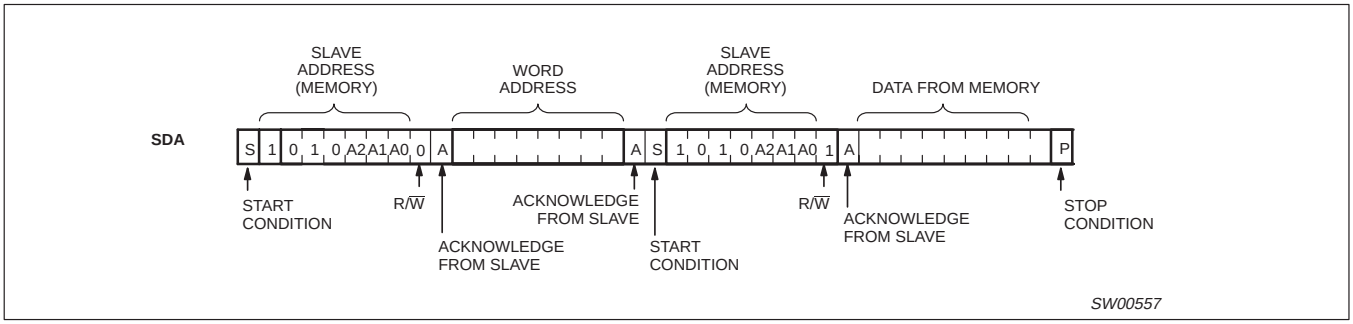


Figure 15. Random Read

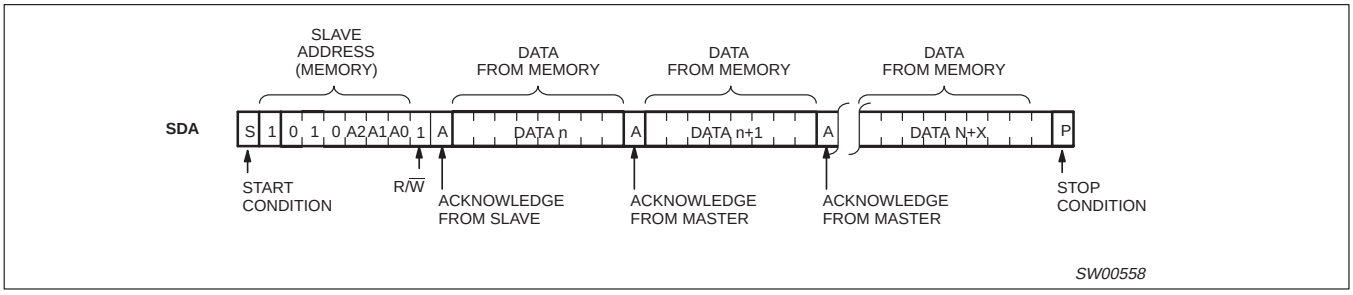


Figure 16. Sequential Read

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{CC}	Supply Voltage	–0.5	4.0	V
V_I	Input Voltage	V_{SS} – 0.5	5.5	V
I_I	DC Input Current	–20	20	mA
I_O	DC Output Current	–25	25	mA
I_{DD}	Supply Current	–100	100	mA
I_{SS}	Supply Current	–100	100	mA
P_{tot}	Total Power Dissipation		400	mW
P_O	Total Power Dissipation per Output		100	mW
T_{STG}	Storage Temperature	–65	+150	°C
T_{AMB}	Operating Temperature	–40	+85	°C
V_{ESD}	Electrostatic Discharge:			
	Human Body Model, 1.5 kΩ, 100 pF	–	>2000	V
	Machine Model, 0 Ω, 200 pF	–	>200	V

DC ELECTRICAL CHARACTERISTICS

T_{amb} = –40°C to +85°C unless otherwise specified; V_{CC} = 3.3 V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Supply					
V_{DD}	Supply Voltage	2.5	3.3	3.6	V
I_{DDQ}	Standby Current; A0, A1, A2, $\overline{WC}$ = HIGH			60	µA
I_{DD1}	Supply Current Read			1	mA
I_{DD2}	Supply Current Write			2	mA
V_{POR}	Power on Reset Voltage			2.4	V
Input SCL; input, output SDA					
V_{IL}	Input LOW voltage	–0.5		0.3 V_{DD}	V
V_{IH}	Input HIGH voltage	0.7 V_{DD}		5.5	V
I_{OL}	Output LOW current @ V_{OL} = 0.4 V	3			mA
I_L	Input leakage current @ $V_I = V_{DD}$ or V_{SS}	–1		1	µA
C_I	Input capacitance @ $V_I = V_{SS}$			7	pF
I/O Expander Port					
V_{IL}	Input LOW voltage	–0.5		0.3 V_{DD}	V
V_{IH}	Input HIGH voltage	0.7 V_{DD}		5.5	V
$I_{IHL(max)}$	Input current through protection diodes	–400		400	µA
I_{OL}	Output LOW current @ V_{OL} = 1 V	10	25		mA
I_{OH}	Output HIGH current @ $V_{OH} = V_{ss}$	30	100	300	µA
I_{OHt}	Transient pull-up current		2		mA
C_I	Input Capacitance			10	pF
C_O	Output Capacitance			10	pF
Address Inputs (A0, A1, A2), $\overline{WC}$ input					
V_{IL}	Input LOW voltage	–0.5		0.3 V_{DD}	V
V_{IH}	Input HIGH voltage	0.7 V_{DD}		5.5	V
I_L	Input leakage current @ $V_I = V_{DD}$	–1		1	µA
	Input leakage (pull-up) current @ $V_I = V_{SS}$	10	25	100	µA

I²C-BUS TIMING CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
I²C-bus timing (see Figure 17; Note 1)					
f_{SCL}	SCL clock frequency	–	–	400	kHz
t_{SW}	tolerable spike width on bus	–	–	50	ns
t_{BUF}	bus free time	1.3	–	–	µs
$t_{SU;STA}$	START condition set–up time	0.6	–	–	µs
$t_{HD;STA}$	START condition hold time	0.6	–	–	µs
t_r	SCL and SDA rise time	–	–	0.3	µs
t_f	SCL and SDA fall time	–	–	0.3	µs
$t_{SU;DAT}$	data set–up time	250	–	–	ns
$t_{HD;DAT}$	data hold time	0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid	–	–	1.0	µs
$t_{SU;STO}$	STOP condition set–up time	0.6	–	–	µs

NOTE:
1. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

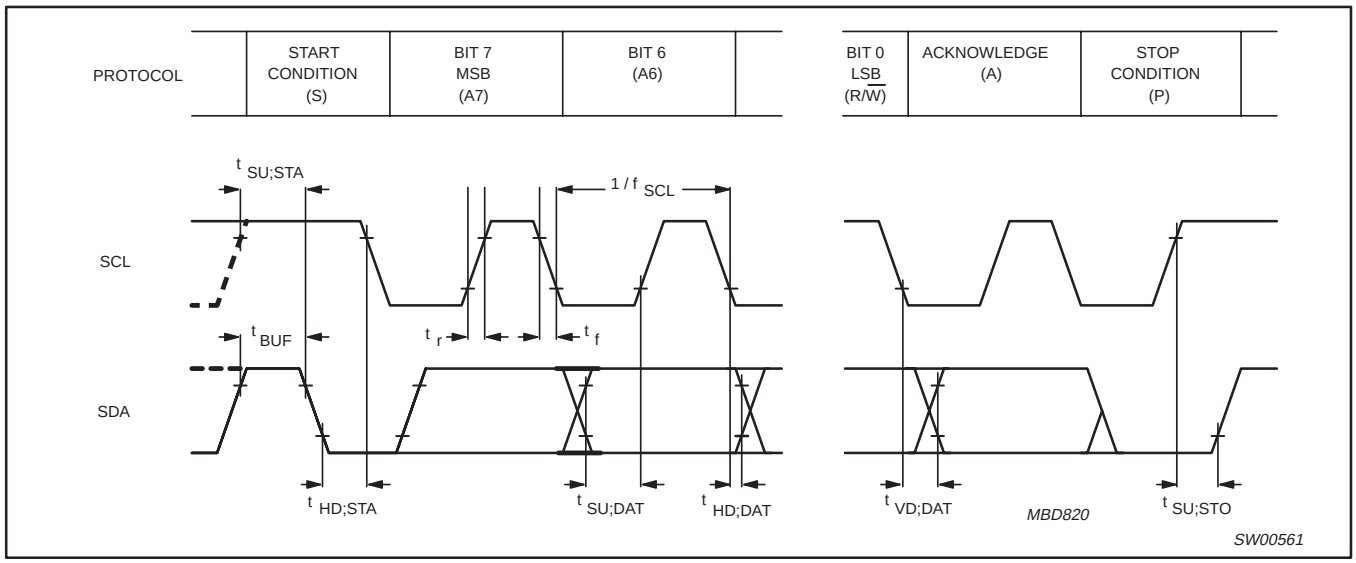


Figure 17.

POWER-UP TIMING

SYMBOL	PARAMETER	MAX.	UNIT
t_{PUR}[1]	Power-up to Read Operation	1	ms
t_{PUW}[1]	Power-up to Write Operation	5	ms

NOTE:
1. t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are guaranteed by design.

WRITE CYCLE LIMITS

SYMBOL	PARAMETER	MIN.	TYP. (5)	MAX.	UNIT
t_{WR}[1]	Write Cycle Time	–	5	10	ms

NOTE:
1. t_{WR} is the maximum time that the device requires to perform the internal write operation.

Write Cycle Timing

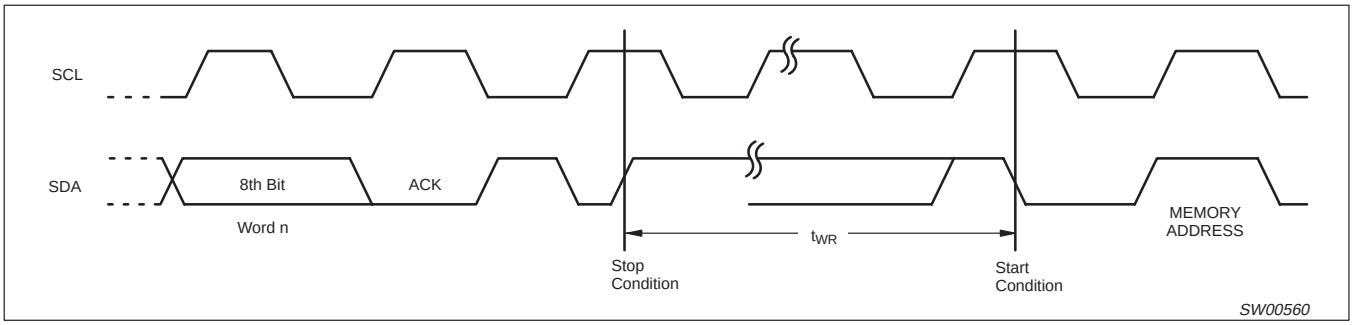


Figure 18.

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *IC Package Databook* (order code 9398 652 90011).

DIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260°C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature (T_{stg} max). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300°C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400°C, contact may be up to 5 seconds.

SO and SSOP

Reflow soldering

Reflow soldering techniques are suitable for all SO and SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250°C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45°C.

Wave soldering

Wave soldering is not recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369–1) or SSOP20 (SOT266–1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260°C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150°C within 6 seconds. Typical dwell time is 4 seconds at 250°C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

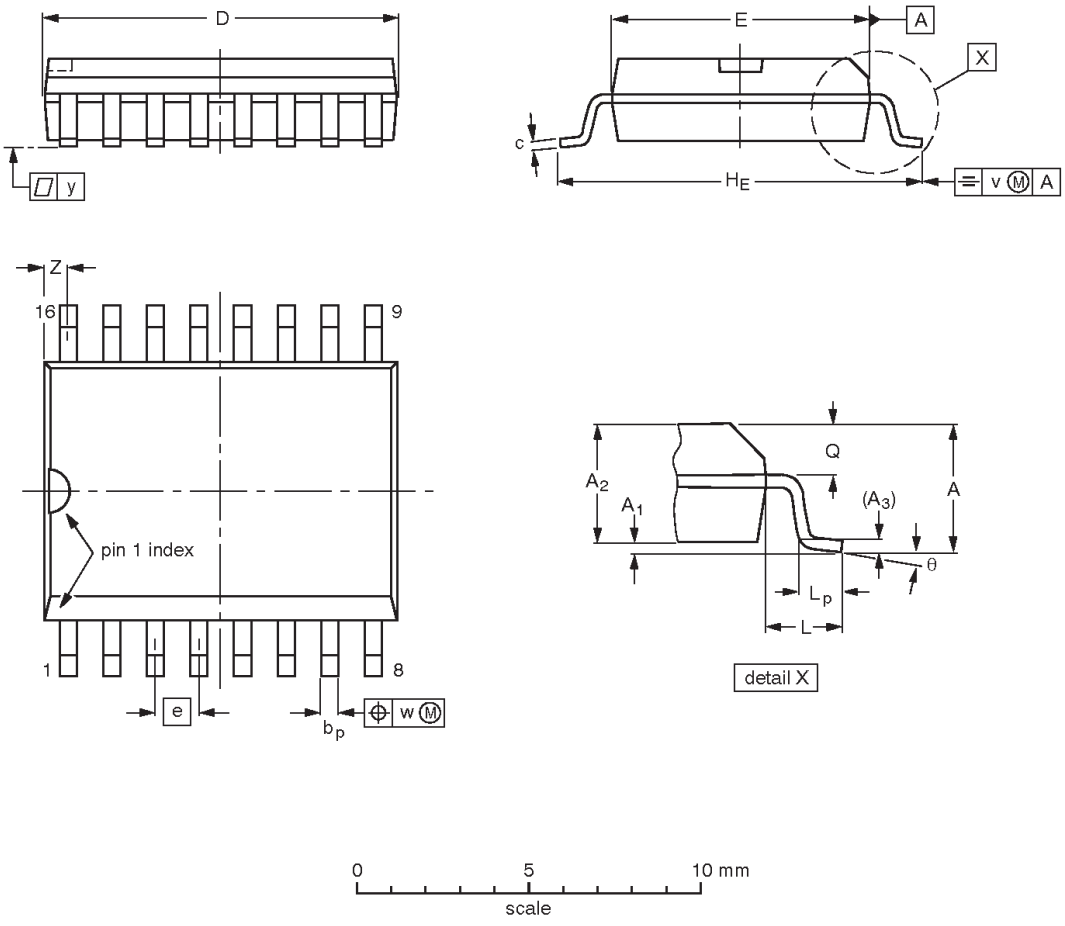
Repairing soldered joints

Fix the component by first soldering two diagonally opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320°C.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

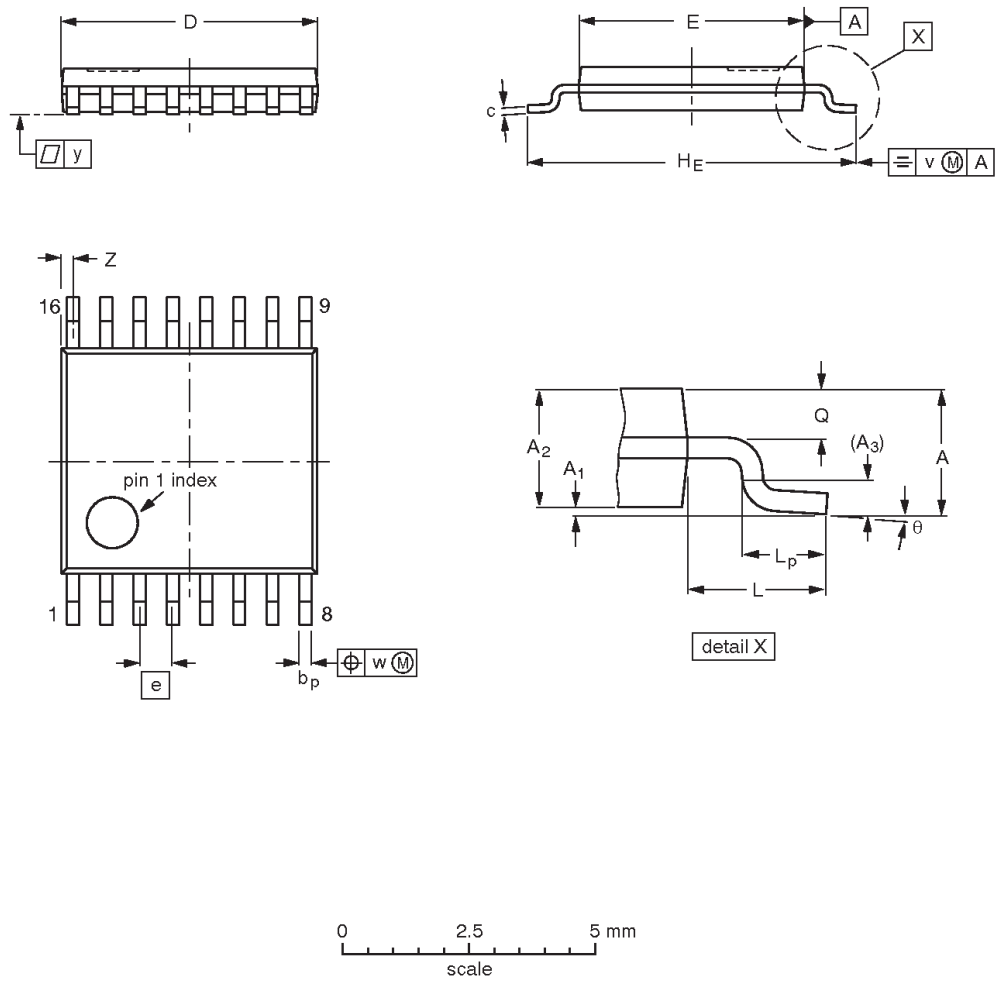
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013				~~97-05-22~~ 99-12-27

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~95-04-04~~ 99-12-27

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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