DS07-13716-2E

16-bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90440G Series

MB90443G/F443G/V440G

■ DESCRIPTION

The MB90440G series with FULL-CAN*2 and FLASH ROM is a line of general-purpose, Fujitsu 16-bit microcontrollers specially designed for automotive and industrial applications. Its main features are three on board CAN Interfaces (generic type) , which conform to V2.0 Part A and Part B, supporting very flexible message buffering. Thus, more functions than a normal full CAN approach is available.

While inheriting the AT architecture of the F²MC*1 family, the instruction set for the F²MC-16LX CPU core incorporates additional instructions for high-level languages, supports extended addressing modes, and contains enhanced multiplication and division instructions as well as a substantial collection of improved bit manipulation instructions. In addition, the MB90440G series has as on-chip 32-bit accumulator, which enables processing of long-word data.

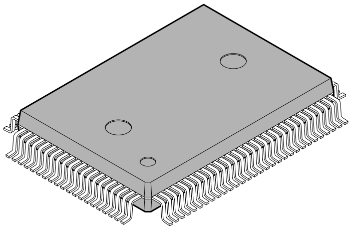
The peripheral resources integrated in the MB90440G series include; an 8/10-bit A/D converter, UARTs (SCI) , I/O extended serial interface, 8/16-bit PPG timer, input/output timer (input capture (ICU) , output compare (OCU)) .

*1 : F²MC stands for FUJITUS Flexible Microcontroller, a registered trademark of FUJITSU LIMITED.

*2 : Controller Area Network (CAN) is a license of Robert Bosch GmbH..

■ PACKAGE

100-pin Plastic QFP



FPT-100P-M06

■ FEATURES

- **Clock**

  Internal PLL clock multiplication circuit
  Base oscillation divided into two or multiplied by one to four
  Minimum execution time : 62.5 ns (4 MHz oscillation, PLL clock multiplication multiplier = 4, V_{CC} = 5.0 V)
  32 kHz subsystem clock

- **Instruction set optimized for controller applications**

  Supported data types : bit, byte, word, and long-word types
  Standard addressing modes : 23 types
  Singed multiplication/division and extended RET1 instructions
  32-bit accumulator enhancing high-precision operations

- **Enhanced high level language (C) and multi-tasking support instructions**

  Use of a system stack pointer
  Symmetrical instruction set and barrel shift instructions

- **Program patch function (for two address pointers)**
- **Enhanced execution speed : 4 byte instruction queue**
- **Enhanced interrupt function : 8 priority levels programmable and 34 causes**
- **Automatic data transmission function independent of CPU operation**

  Extended intelligent I/O service function (EI^2OS)

- **Internal ROM size and type**

  FLASH ROM : 128 Kbytes
  Internal RAM size : 6 Kbyte and 14 Kbyte (evaluation chip)

- **FLASH ROM**

  Supports automatic programming function, Embedded Algorithm*
  Writing command/erase command/erase suspend and resume command
  Algorithms completion flag
  Hardwire reset vector to show the fixed boot code sector
  Can be erased by each sector
  Sector protection by external programming voltage

- **Low-power consumption (stand-by) modes**

  Sleep mode (CPU operating clock stops)
    Stop mode (Main oscillation stops)
  CPU intermittent operation mode
    Watch mode
  Time-base timer mode

- **General-purpose I/O ports : 81 ports**
- **Timers**

  Watchdog timer : 1 channel
  8/16-bit PPG timer : 8/16-bit × 4 channels
  16-bit reload timer : 2 channels

* : Embedded Algorithm is a trademark of Advanced Micro Devices, Inc.

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- **16-bit I/O timers**

  16-bit free-run timers : 1 channel
  16-bit input capture : 8 channels
  16-bit output compare : 4 channels

- **Extended I/O serial interfaces : 1 channel**
- **UART0**

  Full-duplex, double-buffered (8 bit)
  Can be used for clock synchronous and asynchronous transfer (with start/stop bit)

- **UART1 (SCI)**

  Full-duplex, double-buffered (8 bit)
  Can be used for clock synchronous and asynchronous serial transfer (extended I/O serial)

- **External interrupt inputs : 8 channels**

  Extended intelligent I/O service (EI^2OS) is started by external input and external interrupt generation module

- **Delayed interrupt generation module : interrupt request for task switching**
- **8/10 bit A/D converter : 8 channels**

  8/10-bit resolution selectable
  Can be started by external trigger input
  Conversion time : 6.12 µs

- **FULL-CAN interface**

  3 channels
  Conform to V2.0 Part A and Part B
  Supports very flexible message buffering (mail-box and FIFO buffering can be mixed)

- **External bus interface : maximum 16 Mbyte address space**

■ PRODUCT LINEUP

The following table provides a quick outlook of the MB90440G Series

Parameter \ Part number	MB90443G (under development)	MB90F443G	MB90V440G
CPU	F²MC-16LX CPU		
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, 1/2 when PLL stops) Minimum instruction execution time : 62.5 ns (4 MHz osc. PLL ×4)		
ROM size	Mask ROM 128 Kbytes	Flash memory 128 Kbytes	External
RAM size	6 Kbytes	6 Kbytes	14 Kbytes
Operating*1 voltage range	5 V ± 10%		
Temperature range	–40 °C to +105 °C		
Package	QFP100		PGA-256
Voltage dedicated for emulator*2	—		No
UART0	Full duplex double buffer Supports clock asynchronous/synchronous (with start/stop bits) transfer Baud rate : 4808/5208/9615/10417/19230/38460/62500/500000 bps (asynchronous) 500 K/1 M/2 Mbps (synchronous) at System clock = 16 MHz		
UART1 (SCI)	Full duplex double buffer Asynchronized (start/stop bits synchronized) and CLK-synchronous communication Baud rate : 601 bps to 250 kbps (asynchronous) 31.25 kbps to 2 Mbps (synchronous)		
Serial IO	Transfer can be started from MSB or LSB Supports internal clock synchronized transfer and external clock synchronized transfer Supports positive-edge and negative-edge clock synchronization Baud rate : 31.25 K/62.5 K/125 K/500 K/1 M/2 Mbps at System clock = 16 MHz		
8/10 bit A/D Converter	10-bit or 8-bit resolution 8 input channels Conversion time : 6.12 µs (per one channel)		
16-bit Reload Timer (2 channels)	Operation clock frequency : $fsys/2^1$, $fsys/2^3$, $fsys/2^5$ (fsys = System clock frequency) Supports External Event Count function		
16-bit I/O Timer	Signals an interrupt during overflow Supports Timer Clear during a match with Output Compare (Channel 0) Operation clock freq. : $fsys/2^2$, $fsys/2^4$, $fsys/2^6$, $fsys/2^8$ (fsys = System clock freq.)		
16-bit Output Compare (4 channels)	Signals an interrupt during a match with 16-bit I/O Timer Four 16-bit compare registers A pair of compare registers can be used to generate an output signal		

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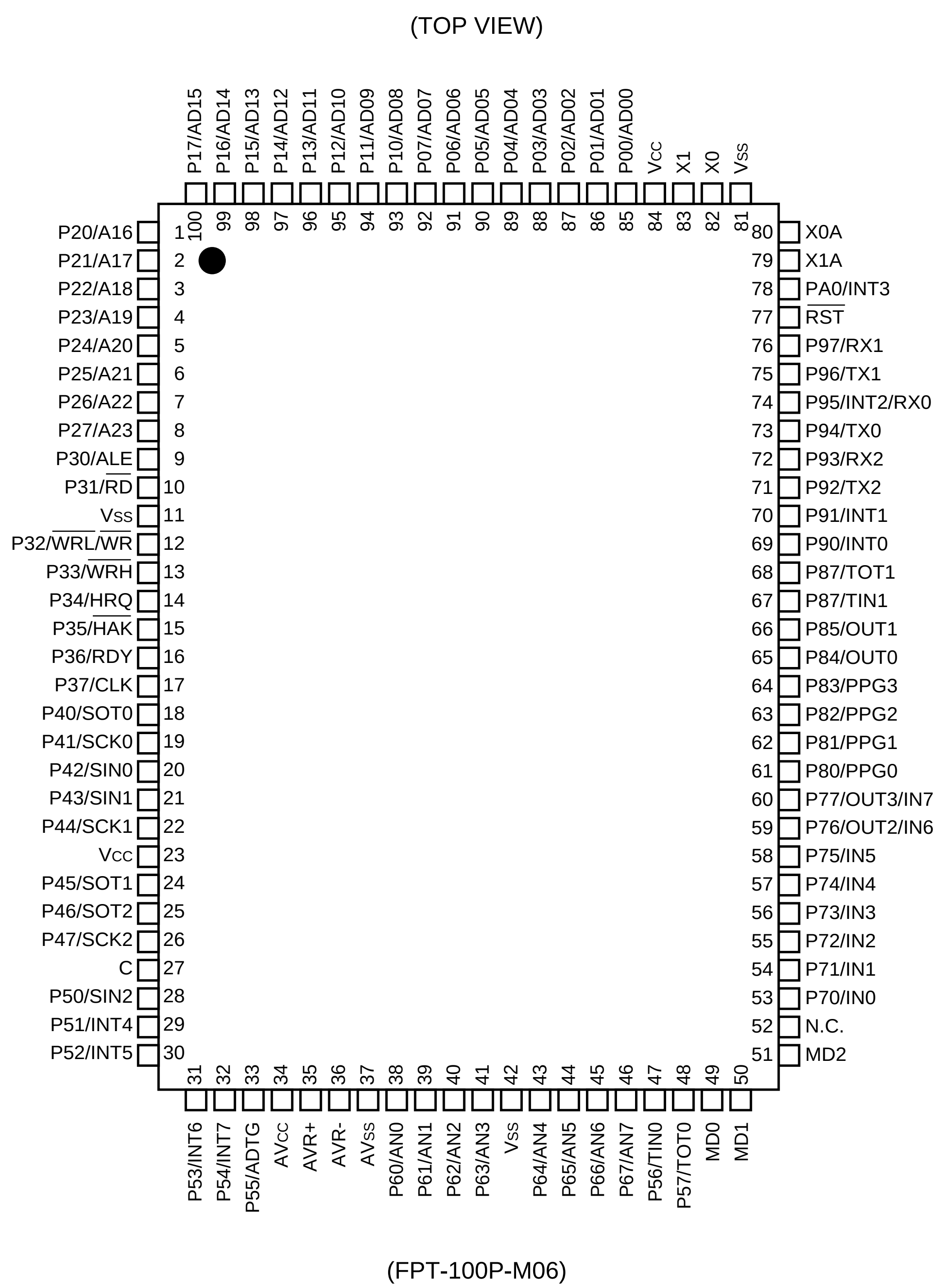
Parameter \ Part number	MB90443G (under development)	MB90F443G	MB90V440G
16-bit Input Capture (8 channels)	Rising edge, falling edge or rising & falling edge sensitive Four 16-bit capture registers Signals an interrupt upon external event		
8/16-bit Programmable Pulse Generator (4 channels)	Supports 8-bit and 16-bit operation modes Eight 8-bit reload counters Eight 8-bit reload registers for L pulse width Eight 8-bit reload registers for H pulse width A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter 4 output pins Operation clock frequency. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 µs@fosc = 4 MHz (fsys = System clock frequency, fosc = Oscillation clock frequency)		
CAN Interface 3 channels :	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Supports prioritized 16 message buffers for data and ID Flexible configuration of acceptance filtering : Full bit compare / Full bit mask / Two partial bit masks Supports up to 1 Mbps		
External Interrupt (8 channels)	Can be programmed edge detection or level detection		
External bus interface	The external access used selective 8-bit bus or 16-bit bus is available. (External bus mode)		
I/O Ports	Virtually all external pins can be used as general purpose I/O All push-pull outputs and schmitt trigger inputs Bit-wise programmable as input/output or peripheral signal		
32 kHz Subclock	Sub-clock for low power operation		
Flash Memory	Supports automatic programming, Embedded Algorithm™ Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 10 years Boot block configuration Erase can be performed on each block Block protection with external programming voltage		

*1 : Values with conditions such as the operating frequency (See section "■ ELECTRICAL CHARACTERISTICS") .

*2 : DIP switch S2 when using emulation pad MB2145-507.
The details are referred to hardware manual of MB2145-507.

■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin No.	Pin name	Circuit type	Function
82 83	X0 X1	A (Oscillation)	High speed oscillator input pins
80 79	X0A X1A	A (Oscillation)	Low speed oscillator input pins
77	$\overline{\text{RST}}$	B	External reset request input
52	N.C.	—	not connected
85 to 92	P00 to P07	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
	AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
93 to 100	P10 to P17	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
	AD08 to AD15		I/O pins for 8 higher bits of the external address/data bus. This function is enabled when the external bus is enabled.
1 to 8	P20 to P27	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
	A16 to A23		I/O pins of 8 bits for A16 to A23 ot the external address bus. This function is enabled when the external bus is enabled.
9	P30	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
	ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
10	P31	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
	$\overline{\text{RD}}$		Read strobe output pin for the data bus. This function is enabled when the external bus is enabled.
12	P32	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the $\overline{\text{WR}}$/$\overline{\text{WRL}}$ pin output is disabled.
	$\overline{\text{WRL}}$ $\overline{\text{WR}}$		Write strobe output pin for the data bus. This function is enabled when the external bus is in enable mode and the $\overline{\text{WR}}$/$\overline{\text{WRL}}$ pin output is enabled. $\overline{\text{WRL}}$ is used as a write-strobe output pin for 8 lower bits of the data bus in 16-bit access while $\overline{\text{WR}}$ is used as a write-strobe output pin for 8 bits of the data bus in 8-bit access.
13	P33	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode or external bus 8-bit mode or when $\overline{\text{WRH}}$ pin output is disabled.
	$\overline{\text{WRH}}$		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{\text{WRH}}$ output pin is enabled.

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Pin No.	Pin name	Circuit type	Function
14	P34	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when hold function is disabled.
	HRQ		Hold request input pin. This function is enabled when the external bus is in enable mode and the hold function is enabled.
15	P35	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when hold function is disabled.
	$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when the external bus is in enable mode and the hold function is enabled.
16	P36	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the external ready function is disabled.
	RDY		Ready input pin. This function is enabled when the external bus is in enable mode and the external ready function is enabled.
17	P37	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when CLK output is disabled.
	CLK		CLK output pin. This function is enabled when the external bus is in enable mode and CLK output is enabled.
18	P40	G	General I/O port. This function is enabled when serial data output of UART0 is disabled.
	SOT0		Serial data output pin for UART0. This function is enabled when UART0 enables serial data output.
19	P41	G	General I/O port. This function is enabled when clock output of UART0 is disabled.
	SCK0		Serial clock I/O pin for UART0. This function is enabled when UART0 enables serial clock output.
20	P42	G	General I/O port. This function is always enabled.
	SIN0		Serial data input pin for UART0. Set the corresponding DDR register to input if this function is used.
21	P43	G	General I/O port. This function is always enabled.
	SIN1		Serial data input pin for UART1. Set the corresponding DDR register to input if this function is used.
22	P44	G	General I/O port. This function is enabled when serial clock output of UART1 is disabled.
	SCK1		Serial clock I/O pin for UART1. This function is enabled when UART1 enables serial clock output.
24	P45	G	General I/O port. This function is enabled when serial data output of UART1 is disabled.
	SOT1		Serial data output pin for UART1. This function is enabled when UART1 enables serial data output.

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Pin No.	Pin name	Circuit type	Function
25	P46	G	General I/O port. This function is enabled when the extended serial I/O interface disables serial data output.
	SOT2		Serial data output pin for the extended serial I/O interface. This function is enabled when the extended serial I/O interface enables serial data output.
26	P47	G	General I/O port. This function is enabled when the extended serial I/O interface disables serial clock output.
	SCK2		Serial clock I/O pin for the extended serial I/O interface. This function is enabled when the extended serial I/O interface enables serial clock output.
28	P50	D	General I/O port. This function is always enabled.
	SIN2		Serial data input pin for the extended serial I/O interface. Set the corresponidng DDR register to input if this function is used.
29 to 32	P51 to P54	D	General I/O ports. This function is always enabled.
	INT4 to INT7		External interrupt request input pins for INT4 to INT7. Set the corresponding DDR register to input if this function is used.
33	P55	D	General I/O port. This function is always enabled.
	ADTG		External trigger input pin for the 8/10-bit A/D converter. Set the corresponding DDR register to input if this function is used.
38 to 41	P60 to P63	E	General I/O ports. The function is enabled when the analog input enable register specifies port.
	AN0 to AN3		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies A/D.
43 to 46	P64 to P67	E	General I/O ports. The function is enabled when the analog input enable register specifies port.
	AN4 to AN7		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies A/D.
47	P56	D	General I/O port. This function is always enabled.
	TIN0		Event input pin for the 16-bit reload timers 0. Set the corresponding DDR register to input if this function is used.
48	P57	D	General I/O port. This function is enabled when the 16-bit reload timers 0 disables output.
	TOT0		Output pin for the 16-bit reload timers 0. This function is enabled when the 16-bit reload timers 0 enables output.
53 to 58	P70 to P75	D	General I/O ports. This function is always enabled.
	IN0 to IN5		Trigger input pins for input captures ICU0 to ICU5. Set the corresponding DDR register to input if this function is used.

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Pin No.	Pin name	Circuit type	Function
59 to 60	P76 to P77	D	General I/O ports. This function is enabled when the OCU disables output.
	OUT2 to OUT3		Event output pins for output compares OCU2 and OCU3. This function is enabled when the OCU enables output.
	IN6 to IN7		Trigger input pins for input captures ICU6 and ICU7. Set the corre-sponiding DDR register to input and prohibit the OCU output if this function is used.
61 to 64	P80 to P83	D	General I/O ports. This function is enabled when 8/16-bit PPG timer disables waveform output.
	PPG0 to PPG3		Output pins for 8/16-bit PPG timer. This function is enabled when 8/16-bit PPG timer enables waveform output.
65 to 66	P84 to P85	D	General I/O ports. This function is enabled when the OCU disables output.
	OUT0 to OUT1		Event output pins for output compares OCU0 and OCU1. This func-tion is enabled when the OCU enables output.
67	P86	D	General I/O port. This function is always enabled.
	TIN1		Input pin for the 16-bit reload timers 1. Set the corresponding DDR register to input if this function is used.
68	P87	D	General I/O port. This function is enabled when the 16-bit reload timers 0 disables output.
	TOT1		Output pin for the 16-bit reload timers 1. This function is enabled when the reload timers 1 enables output.
69 to 70	P90 to P91	D	General I/O ports. This function is always enabled.
	INT0 to INT1		External interrupt request input pins for INT0 to INT3. Set the cor-responding DDR register to input if this function is used.
71	P92	D	General I/O port. This function is enabled when CAN2 disables out-put.
	TX2		TX output pin for CAN2. This function is enabled when CAN2 en-ables output.
72	P93	D	General I/O port. This function is always enabled.
	RX2		RX input pin for CAN2 interface. When the CAN function is used, output from the other functions must be stopped.
73	P94	D	General I/O port. This function is enabled when CAN0 disables out-put.
	TX0		TX output pin for CAN0. This function is enabled when CAN0 en-ables output.
74	P95	D	General I/O port. This function is always enabled.
	INT2		External interrupt request input pin for INT2. Set the corresponding DDR register to input if this function is used.
	RX0		RX input pin for CAN0 interface. When the CAN function is used, output from the other functions must be stopped.

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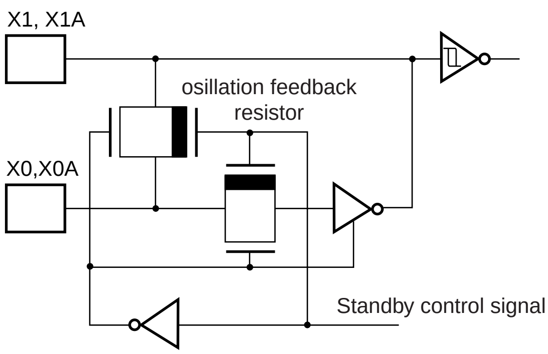
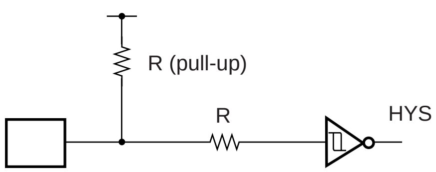
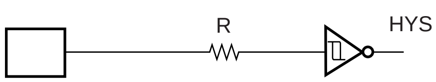
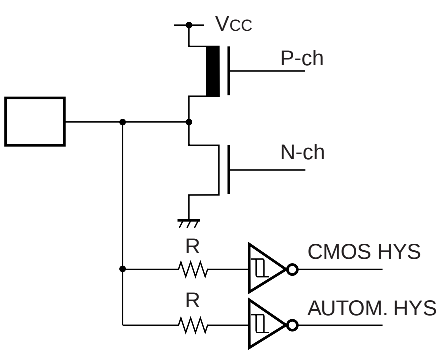
Pin No.	Pin name	Circuit type	Function
75	P96	D	General I/O port. This function is enabled when CAN1 disables output.
	TX1		TX output pin for CAN1. This function is enabled when CAN1 enables output.
76	P97	D	General I/O port. This function is always enabled.
	RX1		RX input pin for CAN1 interface. When the CAN function is used, output from the other functions must be stopped.
78	PA0	D	General I/O port. This function is always enabled.
	INT3		External interrupt request input pin for INT2. Set the corresponding DDR register to input if this function is used.
34	AV_{CC}	Power supply	Power supply pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AV_{CC} is applied to V_{CC}.
37	AV_{SS}	Power supply	Dedicated ground pin for the A/D Converter
35	AVRH	Power supply	External reference voltage pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV_{CC}.
36	AVRL	Power supply	External reference voltage pin for the A/D Converter
49 to 50	MD0 to MD1	C	Input pins for specifying the operating mode. The pins must be directly connected to V_{CC} or Vss.
51	MD2	F	Input pin for specifying the operating mode. The pin must be directly connected to V_{CC} or Vss.
27	C	—	This is the power supply stabilization capacitor pin. It should be connected externally to an 0.1 µF ceramic capacitor.
23, 84	V_{CC}	Power supply	Voltage (5.0 V) input pin
11, 42 81	V_{SS}	Power supply	Voltage (0.0 V) input pin

■ INPUT LEVELS

The input level of ports P00 to P37 can be selected to be either TTL- or CMOS - level. The initial setting is TTL - level. These settings are global for all P00 to P37, it is not possible to set different levels to each port.

The input level of ports P40 to PA0 can be selected to be either CMOS- or AUTOMOTIVE - level. The initial setting is CMOS - level. This settings can be done for each port individually.

■ I/O CIRCUIT TYPE

Circuit type	Circuit	Remarks
A		• Oscillation feedback resistor : 1 MΩ approx. (High speed oscillator) 10MΩ approx. (Low speed oscillator)
B		• CMOS hysteresis input . Pull-up resistor : 50 kΩ approx.
C		• CMOS hysteresis input
D		• CMOS level output • CMOS hysteresis input • Automotive hysteresis input (See "■ INPUT LEVELS".)

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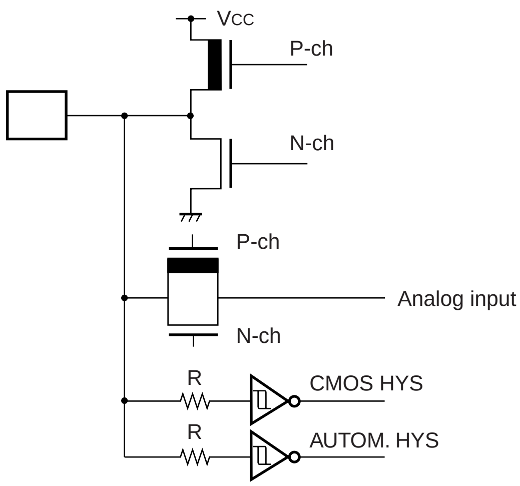
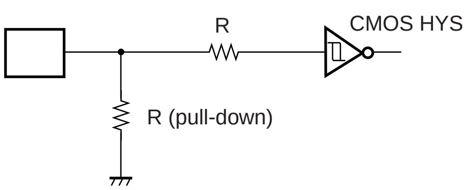
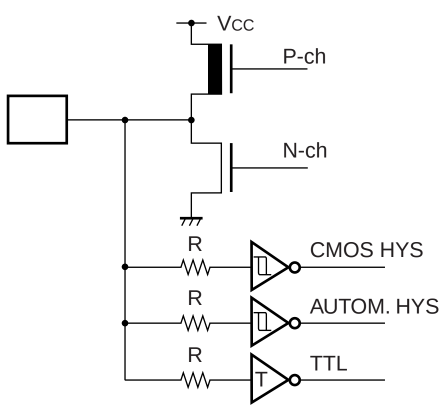
Circuit type	Circuit	Remarks
E		• CMOS level output • CMOS hysteresis input • Automotive hysteresis input (See "■ INPUT LEVELS".) • Analog input
F		• CMOS hysteresis input • Pull-down resistor : 50 kΩ approx. (except FLASH devices)
G		• CMOS level output • CMOS hysteresis input • Automotive hysteresis input (See "■ INPUT LEVELS".) • TTL input (FLASH devices in flash write mode only)

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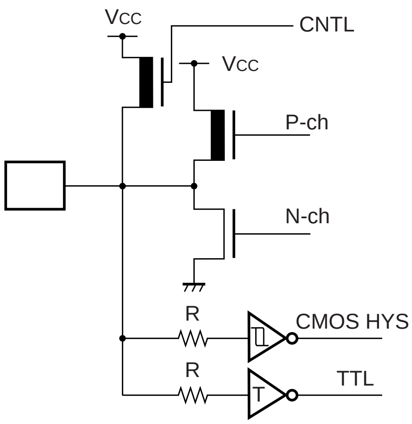
Circuit type	Circuit	Remarks
H		• CMOS level output • CMOS hysteresis input • TTL hysteresis input (See "■ INPUT LEVELS".) • Programmable pullup resistor : 50 kΩ approx.

■ HANDLING DEVICES

1. Preventing Latch-up

CMOS IC chips may suffer latch-up under the following conditions :

(1) A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
(2) A voltage higher than the rated voltage is applied to between V_{CC} and Vss.
(3) The AV_{CC} power supply is applied before the V_{CC} voltage.

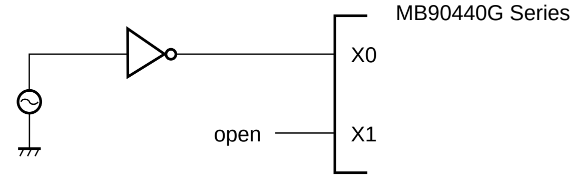
Latch-up may increase the power supply current drastically, causing thermal damage to the device.
Always take sufficient precautions in using semiconductor devices to avoid this possibility.
Also be careful not to let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage (V_{CC}) when the analog system power-supply is turned on and off.

2. Handling Unused Input Pins

Do not leave unused input pins open, as doing so may cause misoperation of the device or latch-up leading to permanent damage. Unused input pins should be pulled up or pulled down through at least 2 kΩ resistance.
Unused I/O pins may be left open in output state, but if such pins are in input state they should be handled in the same way as input pins.

3. Use of the External Clock

To use the external clock, drive only the X0 pin and leave the X1 pin open.
A diagram of how to use an external clock is shown below.

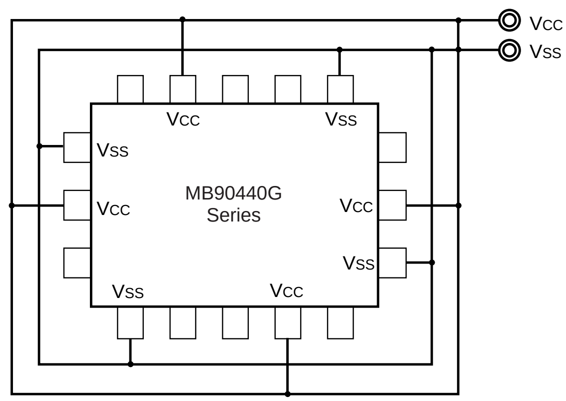


4. Precautions for when not using a Sub Clock Signal

If the X0A and X1A pins are not connected to an oscillator, apply pull-down treatment to the X0A pin and leave the X1A pin open.

5. Power Supply Pins (V_{CC}/V_{SS})

In products with multiple V_{CC} or V_{SS} pins, the pins of a same potential are internally connected in the device to avoid abnormal operations including latch-up. However, connect the pins external power and ground lines to lower the electro-magnetic emission level to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.
Make sure to connect V_{CC} and V_{SS} pins via lowest impedance to power lines.
It is recommended to provide a bypass capacitor of around 0.1 µF between V_{CC} and V_{SS} pins near the device.



6. Pull-up/down resistors

The MB90440G Series does not support internal pull-up/down resistors (except pull-up resistors of port 0 to port 3) . Use external components needed.

7. Crystal Oscillator Circuit

Noises around X0 or X1 pins may cause abnormal operations. Make sure to provide bypass capacitors via the shortest distances from X0 and X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuits do not cross the lines of other circuits.
It is highly recommended to provide a printed circuit board artwork surrounding X0 and X1 pins with a ground area for stabilizing the operation.

8. Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D and D/A converters power supply (AV_{CC}, AVRH, AVRL) and analog inputs (AN0 to AN7) after turning on the digital power supply (V_{CC}) .
Turn off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that AVRH does not exceed AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable) .

9. Connection of Unused Pins of A/D Converter

Connect unused pins of A/D and D/A converters to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = V_{SS}$.

10. N.C. Pin

The N.C. (internally connected) pin must be opened for use.

11. Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 µs or more (0.2 V to 2.7 V) .

12. Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

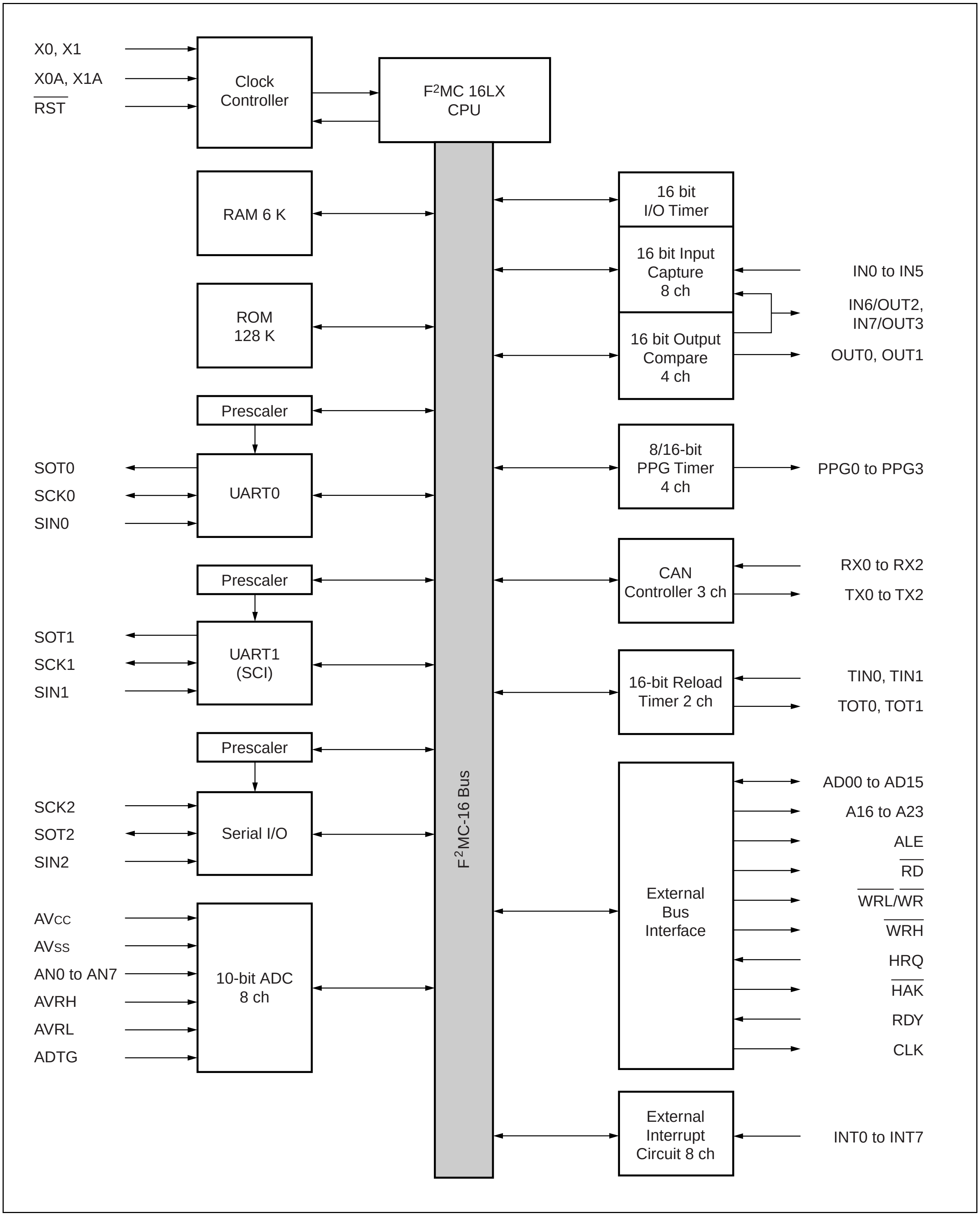
13. Using REALOS

The use of (EI^2OS) is not possible with the REALOS real time operation system.

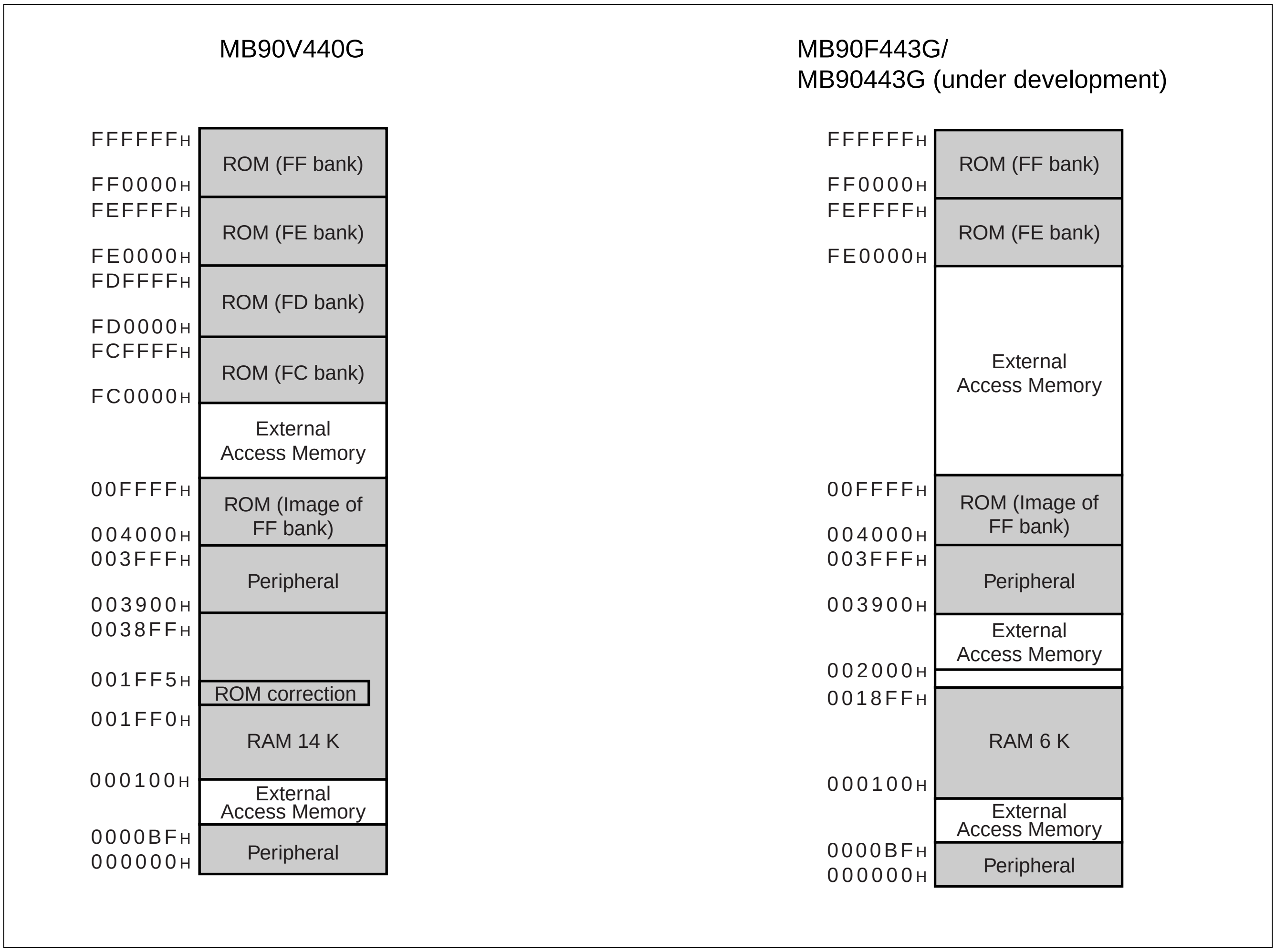
14. Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected in the microcontroller, it may attempt to continue the operation using the free-running frequency of the automatic oscillating circuit in the PLL circuitly even if the oscillator is out of place or the clock input is stopped. Performance of this operation, however, cannot be guaranteed.

■ BLOCK DIAGRAM



■ MEMORY MAP



Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same address, the table in ROM can be referenced without using the far specification in the pointer declaration.
For example, an attempt to access $00C000_H$ accesses the value at $FFC000_H$ in ROM.
The ROM area in bank FF exceeds 48 Kbytes, and its entire image cannot be shown in bank 00.
The image between $FF4000_H$ and $FFFFFF_H$ is visible in bank 00, while the image between $FF4000_H$ and $FFFFFF_H$ is visible only in bank FF. Thus, it is recommended that the ROM data table be stored in the area of $FF4000_H$ and $FFFFFF_H$.

■ I/O MAP

Address	Register	Abbreviation	Read/ Write	Resource name	Initial value
00$_H$	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXX$_B$
01$_H$	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXX$_B$
02$_H$	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXX$_B$
03$_H$	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXX$_B$
04$_H$	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXX$_B$
05$_H$	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXX$_B$
06$_H$	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXX$_B$
07$_H$	Port 7 data register	PDR7	R/W	Port 7	XXXXXXXX$_B$
08$_H$	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXX$_B$
09$_H$	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXX$_B$
0A$_H$	Port A data register	PDRA	R/W	Port A	_______X$_B$
0B$_H$	Port input levels select register	PILR	R/W	Ports	00000000$_B$
0C$_H$	CAN2 RX/TX pin switching register	CANSWR	R/W	CAN1/2	______00$_B$
0D$_H$ to 0F$_H$	Reserved				
10$_H$	Port 0 direction register	DDR0	R/W	Port 0	00000000$_B$
11$_H$	Port 1 direction register	DDR1	R/W	Port 1	00000000$_B$
12$_H$	Port 2 direction register	DDR2	R/W	Port 2	00000000$_B$
13$_H$	Port 3 direction register	DDR3	R/W	Port 3	00000000$_B$
14$_H$	Port 4 direction register	DDR4	R/W	Port 4	00000000$_B$
15$_H$	Port 5 direction register	DDR5	R/W	Port 5	00000000$_B$
16$_H$	Port 6 direction register	DDR6	R/W	Port 6	00000000$_B$
17$_H$	Port 7 direction register	DDR7	R/W	Port 7	00000000$_B$
18$_H$	Port 8 direction register	DDR8	R/W	Port 8	00000000$_B$
19$_H$	Port 9 direction register	DDR9	R/W	Port 9	00000000$_B$
1A$_H$	Port A direction register	DDRA	R/W	Port A	_______0$_B$
1B$_H$	Analog input enable register	ADER	R/W	Port 6, A/D	11111111$_B$
1C$_H$	Port 0 pullup control register	PUCR0	R/W	Port 0	00000000$_B$
1D$_H$	Port 1 pullup control register	PUCR1	R/W	Port 1	00000000$_B$
1E$_H$	Port 2 pullup control register	PUCR2	R/W	Port 2	00000000$_B$
1F$_H$	Port 3 pullup control register	PUCR3	R/W	Port 3	00000000$_B$
20$_H$	Serial mode control register 0	UMC0	R/W	UART0	00000100$_B$
21$_H$	Serial status register 0	USR0	R/W		00010000$_B$
22$_H$	Serial input/output data register 0	UIDR0/UODR0	R/W		XXXXXXXX$_B$
23$_H$	Rate and data register 0	URD0	R/W		0000000X$_B$

(Continued)

Address	Register	Abbreviation	Read/ Write	Resource name	Initial value
24_H	Serial mode register 1	SMR1	R/W	UART1	00000000_B
25_H	Serial control register 1	SCR1	R/W		00000100_B
26_H	Serial input/output data register 1	SIDR1/SODR1	R/W		$XXXXXXXX_B$
27_H	Serial status register 1	SSR1	R/W		00001_00$_B$
28_H	UART1 prescaler control register	U1CDCR	R/W		0___1111$_B$
29_H	Serial edge selection registor	SES1	R/W		_______0$_B$
$2A_H$	Reserved				
$2B_H$	Serial I/O prescaler	SCDCR	R/W	Serial I/O	0___1111$_B$
$2C_H$	Serial mode control register	SMCS	R/W		____0000$_B$
$2D_H$	Serial mode control register	SMCS	R/W		00000010_B
$2E_H$	Serial Data register	SDR	R/W		$XXXXXXXX_B$
$2F_H$	Serial edge selection registor 2	SES2	R/W		_______0$_B$
30_H	External interrupt enable register	ENIR	R/W	External interrupt circuit	00000000_B
31_H	External interrupt request register	EIRR	R/W		$XXXXXXXX_B$
32_H	External request level setting register	ELVR	R/W		00000000_B
33_H					00000000_B
34_H	A/D control status register 0	ADCS0	R/W	A/D converter	00000000_B
35_H	A/D control status register 1	ADCS1	R/W		00000000_B
36_H	A/D data register 0	ADCR0	R		$XXXXXXXX_B$
37_H	A/D data register 1	ADCR1	R/W		00001_XX$_B$
38_H	PPG0 operation mode control register	PPGC0	R/W	16-bit Progra-mable Pulse Generator 0/1	0_000__1$_B$
39_H	PPG1 operation mode control register	PPGC1	R/W		0_000001$_B$
$3A_H$	PPG0 and PPG1 clock selection register	PPG01	R/W		000000__$_B$
$3B_H$	Reserved				
$3C_H$	PPG2 operation mode control register	PPGC2	R/W	16-bit Progra-mable Pulse Generator 2/3	0_000__1$_B$
$3D_H$	PPG3 operation mode control register	PPGC3	R/W		0_000001$_B$
$3E_H$	PPG2 and PPG3 clock selection register	PPG23	R/W		000000__$_B$
$3F_H$	Reserved				
40_H	PPG4 operation mode control register	PPGC4	R/W	16-bit Progra-mable Pulse Generator 4/5	0_000__1$_B$
41_H	PPG5 operation mode control register	PPGC5	R/W		0_000001$_B$
42_H	PPG4 and PPG5 clock selection register	PPG45	R/W		000000__$_B$
43_H	Reserved				

(Continued)

Address	Register	Abbrevia-tion	Read/ Write	Resource name	Initial value
44$_H$	PPG6 operation mode control register	PPGC6	R/W	16-bit Programable Pulse Generator 6/7	0_000__1$_B$
45$_H$	PPG7 operation mode control register	PPGC7	R/W		0_000001$_B$
46$_H$	PPG6 and PPG7 clock selection register	PPG67	R/W		000000__$_B$
47$_H$ to 4B$_H$	Reserved				
4C$_H$	Input capture control status 0/1	ICS01	R/W	Input capture 0/1	00000000$_B$
4D$_H$	Input capture control status 2/3	ICS23	R/W	Input capture 2/3	00000000$_B$
4E$_H$	Input capture control status 4/5	ICS45	R/W	Input capture 4/5	00000000$_B$
4F$_H$	Input capture control status 6/7	ICS67	R/W	Input capture 6/7	00000000$_B$
50$_H$	Timer control status register 0	TMCSR0	R/W	16-bit reload timer 0	00000000$_B$
51$_H$					____0000$_B$
52$_H$	Timer register 0/reload register 0	TMR0/ TMRLR0	R/W		XXXXXXXX$_B$
53$_H$					XXXXXXXX$_B$
54$_H$	Timer control status register 1	TMCSR1	R/W	16-bit reload timer 1	00000000$_B$
55$_H$					____0000$_B$
56$_H$	Timer register 1/Reload register 1	TMR1/ TMRLR1	R/W		XXXXXXXX$_B$
57$_H$					XXXXXXXX$_B$
58$_H$	Output compare control status register 0	OCS0	R/W	Output compare 0/1	0000__00$_B$
59$_H$	Output compare control status register 1	OCS1	R/W		___00000$_B$
5A$_H$	Output compare control status register 2	OCS2	R/W	Output compare 2/3	0000__00$_B$
5B$_H$	Output compare control status register 3	OCS3	R/W		___00000$_B$
5C$_H$ to 6B$_H$	Reserved for CAN 2 Interface				
6C$_H$	Timer data register	TCDT	R/W	I/O timer	00000000$_B$
6D$_H$					00000000$_B$
6E$_H$	Timer control status register	TCCS	R/W		00000000$_B$
6F$_H$	ROM mirror function selection register	ROMM	R/W	ROM mirror function selec-tion module	_______1$_B$
70$_H$ to 7F$_H$	Reserved for CAN 0 Interface				
80$_H$ to 8F$_H$	Reserved for CAN 1 Interface				
90$_H$ to 9D$_H$	Prohibited area				
9E$_H$	Program address detection control status register	PACSR	R/W	Address match detection function	00000000$_B$
9F$_H$	Delayed interrupt/release register	DIRR	R/W	Delayed interrupt genera-tion module	_______0$_B$

(Continued)

Address	Register	Abbreviation	Read/ Write	Resource name	Initial value
A0$_H$	Low-power consumption mode control register	LPMCR	R/W	Low power consumption (stand-by) mode	00011000$_B$
A1$_H$	Clock selection register	CKSCR	R/W	Low power consumption (stand-by) mode	11111100$_B$
A2$_H$ to A4$_H$	Prohibited area				
A5$_H$	Automatic ready function select register	ARSR	W	External bus pin	0011__00$_B$
A6$_H$	External address output control register	HACR	W		00000000$_B$
A7$_H$	Bus control signal selection register	ECSR	W		0000000_$_B$
A8$_H$	Watchdog timer control register	WDTC	R/W	Watchdog timer	XXXXX111$_B$
A9$_H$	Time base timer control register	TBTC	R/W	Time base timer	1- -00100$_B$
AA$_H$	Watch timer control register	WTC	R/W	Watch timer	1X000000$_B$
AB$_H$ to AD$_H$	Prohibited area				
AE$_H$	Flash memory control status register (Flash only, otherwise reserved)	FMCS	R/W	Flash Memory	000X0000$_B$
AF$_H$	Prohibited area				
B0$_H$	Interrupt control register 00	ICR00	R/W	Interrupt controller	00000111$_B$
B1$_H$	Interrupt control register 01	ICR01	R/W		00000111$_B$
B2$_H$	Interrupt control register 02	ICR02	R/W		00000111$_B$
B3$_H$	Interrupt control register 03	ICR03	R/W		00000111$_B$
B4$_H$	Interrupt control register 04	ICR04	R/W		00000111$_B$
B5$_H$	Interrupt control register 05	ICR05	R/W		00000111$_B$
B6$_H$	Interrupt control register 06	ICR06	R/W		00000111$_B$
B7$_H$	Interrupt control register 07	ICR07	R/W		00000111$_B$
B8$_H$	Interrupt control register 08	ICR08	R/W		00000111$_B$
B9$_H$	Interrupt control register 09	ICR09	R/W		00000111$_B$
BA$_H$	Interrupt control register 10	ICR10	R/W		00000111$_B$
BB$_H$	Interrupt control register 11	ICR11	R/W		00000111$_B$
BC$_H$	Interrupt control register 12	ICR12	R/W		00000111$_B$
BD$_H$	Interrupt control register 13	ICR13	R/W		00000111$_B$
BE$_H$	Interrupt control register 14	ICR14	R/W		00000111$_B$
BF$_H$	Interrupt control register 15	ICR15	R/W		00000111$_B$
CO$_H$ to FF$_H$	External				

(Continued)

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Address	Register	Abbreviation	Read/ Write	Resource name	Initial value
1FF0$_H$	Program address detection register 0	PADR0	R/W	Address match detection function	XXXXXXXX$_B$
1FF1$_H$			R/W		XXXXXXXX$_B$
1FF2$_H$			R/W		XXXXXXXX$_B$
1FF3$_H$	Program address detection register 1	PADR1	R/W		XXXXXXXX$_B$
1FF4$_H$			R/W		XXXXXXXX$_B$
1FF5$_H$			R/W		XXXXXXXX$_B$

Address	Register	Abbreviation	Read/ Write	Resource name	Initial value
3900$_H$	Reload register L	PRLL0	R/W	16-bit programable pulse generator 0/1	XXXXXXXX$_B$
3901$_H$	Reload register H	PRLH0	R/W		XXXXXXXX$_B$
3902$_H$	Reload register L	PRLL1	R/W		XXXXXXXX$_B$
3903$_H$	Reload register H	PRLH1	R/W		XXXXXXXX$_B$
3904$_H$	Reload register L	PRLL2	R/W	16-bit programable pulse generator 2/3	XXXXXXXX$_B$
3905$_H$	Reload register H	PRLH2	R/W		XXXXXXXX$_B$
3906$_H$	Reload register L	PRLL3	R/W		XXXXXXXX$_B$
3907$_H$	Reload register H	PRLH3	R/W		XXXXXXXX$_B$
3908$_H$	Reload register L	PRLL4	R/W	16-bit programable pulse generator 4/5	XXXXXXXX$_B$
3909$_H$	Reload register H	PRLH4	R/W		XXXXXXXX$_B$
390A$_H$	Reload register L	PRLL5	R/W		XXXXXXXX$_B$
390B$_H$	Reload register H	PRLH5	R/W		XXXXXXXX$_B$
390C$_H$	Reload register L	PRLL6	R/W	16-bit programable pulse generator 6/7	XXXXXXXX$_B$
390D$_H$	Reload register H	PRLH6	R/W		XXXXXXXX$_B$
390E$_H$	Reload register L	PRLL7	R/W		XXXXXXXX$_B$
390F$_H$	Reload register H	PRLH7	R/W		XXXXXXXX$_B$
3910$_H$ to 3917$_H$	Reserved				
3918$_H$	Input capture register 0	IPCP0	R	Input captue 0/1	XXXXXXXX$_B$
3919$_H$	Input capture register 0	IPCP0	R		XXXXXXXX$_B$
391A$_H$	Input capture register 1	IPCP1	R		XXXXXXXX$_B$
391B$_H$	Input capture register 1	IPCP1	R		XXXXXXXX$_B$
391C$_H$	Input capture register 2	IPCP2	R	Input captue 2/3	XXXXXXXX$_B$
391D$_H$	Input capture register 2	IPCP2	R		XXXXXXXX$_B$
391E$_H$	Input capture register 3	IPCP3	R		XXXXXXXX$_B$
391F$_H$	Input capture register 3	IPCP3	R		XXXXXXXX$_B$

(Continued)

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Address	Register	Abbreviation	Read/ Write	Resource name	Initial value
3920H	Input capture register 4	IPCP4	R	Input captue 4/5	XXXXXXXXB
3921H	Input capture register 4	IPCP4	R		XXXXXXXXB
3922H	Input capture register 5	IPCP5	R		XXXXXXXXB
3923H	Input capture register 5	IPCP5	R		XXXXXXXXB
3924H	Input capture register 6	IPCP6	R	Input captue 6/7	XXXXXXXXB
3925H	Input capture register 6	IPCP6	R		XXXXXXXXB
3926H	Input capture register 7	IPCP7	R		XXXXXXXXB
3927H	Input capture register 7	IPCP7	R		XXXXXXXXB
3928H	Output compare register 0	OCCP0	R/W	Output compare 0/1	XXXXXXXXB
3929H	Output compare register 0	OCCP0	R/W		XXXXXXXXB
392AH	Output compare register 1	OCCP1	R/W		XXXXXXXXB
392BH	Output compare register 1	OCCP1	R/W		XXXXXXXXB
392CH	Output compare register 2	OCCP2	R/W	Output compare 2/3	XXXXXXXXB
392DH	Output compare register 2	OCCP2	R/W		XXXXXXXXB
392EH	Output compare register 3	OCCP3	R/W		XXXXXXXXB
392FH	Output compare register 3	OCCP3	R/W		XXXXXXXXB
3930H to 39FFH	Reserved				
3A00H to 3AFFH	Reserved for CAN 0 Interface				
3B00H to 3BFFH	Reserved for CAN 0 Interface				
3C00H to 3CFFH	Reserved for CAN 1 Interface				
3D00H to 3DFFH	Reserved for CAN 1 Interface				
3E00H to 3EFFH	Reserved for CAN 2 Interface				
3F00H to 3FFFH	Reserved for CAN 2 Interface				

- Meaning of abbreviations used for reading and writing
  - R/W : Read and Write enabled
  - R : Read only
  - W : Write only
- Explanation of initial values
  - 0 : The bit is initialized to 0.
  - 1 : The bit is initialized to 1.
  - X : The initial value of the bit is undefined.
  - _ : The bit is not used. Its initial value is undefined.

Note : Addresses in the range 0000H to 00FFH, which are not listed in the table, are reserved for the primary functions of the MCU. A read access to these reserved addresses results reading “X” and any write access should not be performed.

■ CAN CONTROLLER

The MB90440G series contains three generic CAN controllers (CAN0, CAN1, CAN2) .

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbps to 1 Mbps (when input clock is at 16 MHz)

List of Control Registers

Address			Register	Abbreviation	Read/ Write	Initial Value
CAN0	CAN1	CAN2				
000070$_H$	000080$_H$	00005C$_H$	Message buffer valid register	BVALR	R/W	00000000 00000000$_B$
000071$_H$	000081$_H$	00005D$_H$				
000072$_H$	000082$_H$	00005E$_H$	Transmit request register	TREQR	R/W	00000000 00000000$_B$
000073$_H$	000083$_H$	00005F$_H$				
000074$_H$	000084$_H$	000060$_H$	Transmit cancel register	TCANR	W	00000000 00000000$_B$
000075$_H$	000085$_H$	000061$_H$				
000076$_H$	000086$_H$	000062$_H$	Transmit complete register	TCR	R/W	00000000 00000000$_B$
000077$_H$	000087$_H$	000063$_H$				
000078$_H$	000088$_H$	000064$_H$	Receive complete register	RCR	R/W	00000000 00000000$_B$
000079$_H$	000089$_H$	000065$_H$				
00007A$_H$	00008A$_H$	000066$_H$	Remote request receiving register	RRTRR	R/W	00000000 00000000$_B$
00007B$_H$	00008B$_H$	000067$_H$				
00007C$_H$	00008C$_H$	000068$_H$	Receive overrun register	ROVRR	R/W	00000000 00000000$_B$
00007D$_H$	00008D$_H$	000069$_H$				
00007E$_H$	00008E$_H$	00006A$_H$	Receive interrupt enable register	RIER	R/W	00000000 00000000$_B$
00007F$_H$	00008F$_H$	00006B$_H$				
003B00$_H$	003D00$_H$	003F00$_H$	Control status register	CSR	R/W, R	00---000 0----0-1$_B$
003B01$_H$	003D01$_H$	003F01$_H$				
003B02$_H$	003D02$_H$	003F02$_H$	Last event indicator register	LEIR	R/W	-------- 000-0000$_B$
003B03$_H$	003D03$_H$	003F03$_H$				
003B04$_H$	003D04$_H$	003F04$_H$	Receive/transmit error counter	RTEC	R	00000000 00000000$_B$
003B05$_H$	003D05$_H$	003F05$_H$				

(Continued)

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Address			Register	Abbreviation	Read/ Write	Initial Value
CAN0	CAN1	CAN2				
003B06H	003D06H	003F06H	Bit timing register	BTR	R/W	-1111111 11111111B
003B07H	003D07H	003F07H				
003B08H	003D08H	003F08H	IDE register	IDER	R/W	XXXXXXXX XXXXXXXXB
003B09H	003D09H	003F09H				
003B0AH	003D0AH	003F0AH	Transmit RTR register	TRTRR	R/W	00000000 00000000B
003B0BH	003D0BH	003F0BH				
003B0CH	003D0CH	003F0CH	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX XXXXXXXXB
003B0DH	003D0DH	003F0DH				
003B0EH	003D0EH	003F0EH	Transmit interrupt enable register	TIER	R/W	00000000 00000000B
003B0FH	003D0FH	003F0FH				
003B10H	003D10H	003F10H	Acceptance mask select register	AMSR	R/W	XXXXXXXX XXXXXXXXB
003B11H	003D11H	003F11H				
003B12H	003D12H	003F12H				XXXXXXXX XXXXXXXXB
003B13H	003D13H	003F13H				
003B14H	003D14H	003F14H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX XXXXXXXXB
003B15H	003D15H	003F15H				
003B16H	003D16H	003F16H				XXXXX--- XXXXXXXXB
003B17H	003D17H	003F17H				
003B18H	003D18H	003F18H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX XXXXXXXXB
003B19H	003D19H	003F19H				
003B1AH	003D1AH	003F1AH				XXXXX--- XXXXXXXXB
003B1BH	003D1BH	003F1BH				

List of Message Buffers (ID Registers)

Address CAN0	Address CAN1	Address CAN2	Register	Abbreviation	Read/ Write	Initial Value
003A00$_H$ to 003A1F$_H$	003C00$_H$ to 003C1F$_H$	003E00$_H$ to 003E1F$_H$	RAM area	—	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$
003A20$_H$	003C20$_H$	003E20$_H$	ID register 0	IDR0	R/W	XXXXXXXX XXXXXXXX$_B$
003A21$_H$	003C21$_H$	003E21$_H$				
003A22$_H$	003C22$_H$	003E22$_H$				XXXXX--- XXXXXXXX$_B$
003A23$_H$	003C23$_H$	003E23$_H$				
003A24$_H$	003C24$_H$	003E24$_H$	ID register 1	IDR1	R/W	XXXXXXXX XXXXXXXX$_B$
003A25$_H$	003C25$_H$	003E25$_H$				
003A26$_H$	003C26$_H$	003E26$_H$				XXXXX--- XXXXXXXX$_B$
003A27$_H$	003C27$_H$	003E27$_H$				
003A28$_H$	003C28$_H$	003E28$_H$	ID register 2	IDR2	R/W	XXXXXXXX XXXXXXXX$_B$
003A29$_H$	003C29$_H$	003E29$_H$				
003A2A$_H$	003C2A$_H$	003E2A$_H$				XXXXX--- XXXXXXXX$_B$
003A2B$_H$	003C2B$_H$	003E2B$_H$				
003A2C$_H$	003C2C$_H$	003E2C$_H$	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXX$_B$
003A2D$_H$	003C2D$_H$	003E2D$_H$				
003A2E$_H$	003C2E$_H$	003E2E$_H$				XXXXX--- XXXXXXXX$_B$
003A2F$_H$	003C2F$_H$	003E2F$_H$				
003A30$_H$	003C30$_H$	003E30$_H$	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXX$_B$
003A31$_H$	003C31$_H$	003E31$_H$				
003A32$_H$	003C32$_H$	003E32$_H$				XXXXX--- XXXXXXXX$_B$
003A33$_H$	003C33$_H$	003E33$_H$				
003A34$_H$	003C34$_H$	003E34$_H$	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXX$_B$
003A35$_H$	003C35$_H$	003E35$_H$				
003A36$_H$	003C36$_H$	003E36$_H$				XXXXX--- XXXXXXXX$_B$
003A37$_H$	003C37$_H$	003E37$_H$				
003A38$_H$	003C38$_H$	003E38$_H$	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXX$_B$
003A39$_H$	003C39$_H$	003E39$_H$				
003A3A$_H$	003C3A$_H$	003E3A$_H$				XXXXX--- XXXXXXXX$_B$
003A3B$_H$	003C3B$_H$	003E3B$_H$				

(Continued)

Address			Register	Abbreviation	Read/ Write	Initial Value
CAN0	CAN1	CAN2				
003A3CH	003C3CH	003E3CH	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXXB
003A3DH	003C3DH	003E3DH				
003A3EH	003C3EH	003E3EH				XXXXX--- XXXXXXXXB
003A3FH	003C3FH	003E3FH				
003A40H	003C40H	003E40H	ID register 8	IDR8	R/W	XXXXXXXX XXXXXXXXB
003A41H	003C41H	003E41H				
003A42H	003C42H	003E42H				XXXXX--- XXXXXXXXB
003A43H	003C43H	003E43H				
003A44H	003C44H	003E44H	ID register 9	IDR9	R/W	XXXXXXXX XXXXXXXXB
003A45H	003C45H	003E45H				
003A46H	003C46H	003E46H				XXXXX--- XXXXXXXXB
003A47H	003C47H	003E47H				
003A48H	003C48H	003E48H	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXXB
003A49H	003C49H	003E49H				
003A4AH	003C4AH	003E4AH				XXXXX--- XXXXXXXXB
003A4BH	003C4BH	003E4BH				
003A4CH	003C4CH	003E4CH	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXXB
003A4DH	003C4DH	003E4DH				
003A4EH	003C4EH	003E4EH				XXXXX--- XXXXXXXXB
003A4FH	003C4FH	003E4FH				
003A50H	003C50H	003E50H	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXXB
003A51H	003C51H	003E51H				
003A52H	003C52H	003E52H				XXXXX--- XXXXXXXXB
003A53H	003C53H	003E53H				
003A54H	003C54H	003E54H	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXXB
003A55H	003C55H	003E55H				
003A56H	003C56H	003E56H				XXXXX--- XXXXXXXXB
003A57H	003C57H	003E57H				
003A58H	003C58H	003E58H	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXXB
003A59H	003C59H	003E59H				
003A5AH	003C5AH	003E5AH				XXXXX--- XXXXXXXXB
003A5BH	003C5BH	003E5BH				

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Address			Register	Abbreviation	Read/ Write	Initial Value
CAN0	CAN1	CAN2				
003A5CH	003C5CH	003E5CH	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXXB
003A5DH	003C5DH	003E5DH				
003A5EH	003C5EH	003E5EH				XXXXX--- XXXXXXXXB
003A5FH	003C5FH	003E5FH				

List of Message Buffers (**DLC Registers and Data Registers**)

Address			Register	Abbreviation	Read/ Write	Initial Value
CAN0	CAN1	CAN2				
003A60H	003C60H	003E60H	DLC register 0	DLCR0	R/W	----XXXXB
003A61H	003C61H	003E61H				
003A62H	003C62H	003E62H	DLC register 1	DLCR1	R/W	----XXXXB
003A63H	003C63H	003E63H				
003A64H	003C64H	003E64H	DLC register 2	DLCR2	R/W	----XXXXB
003A65H	003C65H	003E65H				
003A66H	003C66H	003E66H	DLC register 3	DLCR3	R/W	----XXXXB
003A67H	003C67H	003E67H				
003A68H	003C68H	003E68H	DLC register 4	DLCR4	R/W	----XXXXB
003A69H	003C69H	003E69H				
003A6AH	003C6AH	003E6AH	DLC register 5	DLCR5	R/W	----XXXXB
003A6BH	003C6BH	003E6BH				
003A6CH	003C6CH	003E6CH	DLC register 6	DLCR6	R/W	----XXXXB
003A6DH	003C6DH	003E6DH				
003A6EH	003C6EH	003E6EH	DLC register 7	DLCR7	R/W	----XXXXB
003A6FH	003C6FH	003E6FH				
003A70H	003C70H	003E70H	DLC register 8	DLCR8	R/W	----XXXXB
003A71H	003C71H	003E71H				
003A72H	003C72H	003E72H	DLC register 9	DLCR9	R/W	----XXXXB
003A73H	003C73H	003E73H				
003A74H	003C74H	003E74H	DLC register 10	DLCR10	R/W	----XXXXB
003A75H	003C75H	003E75H				
003A76H	003C76H	003E76H	DLC register 11	DLCR11	R/W	----XXXXB
003A77H	003C77H	003E77H				

(Continued)

Address			Register	Abbreviation	Read/ Write	Initial Value
CAN0	CAN1	CAN2				
003A78$_H$	003C78$_H$	003E78$_H$	DLC register 12	DLCR12	R/W	----XXXX$_B$
003A79$_H$	003C79$_H$	003E79$_H$				
003A7A$_H$	003C7A$_H$	003E7A$_H$	DLC register 13	DLCR13	R/W	----XXXX$_B$
003A7B$_H$	003C7B$_H$	003E7B$_H$				
003A7C$_H$	003C7C$_H$	003E7C$_H$	DLC register 14	DLCR14	R/W	----XXXX$_B$
003A7D$_H$	003C7D$_H$	003E7D$_H$				
003A7E$_H$	003C7E$_H$	003E7E$_H$	DLC register 15	DLCR15	R/W	----XXXX$_B$
003A7F$_H$	003C7F$_H$	003E7F$_H$				
003A80$_H$ to 003A87$_H$	003C80$_H$ to 003C87$_H$	003E80$_H$ to 003E87$_H$	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$
003A88$_H$ to 003A8F$_H$	003C88$_H$ to 003C8F$_H$	003E88$_H$ to 003E8F$_H$	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$
003A90$_H$ to 003A97$_H$	003C90$_H$ to 003C97$_H$	003E90$_H$ to 003E97$_H$	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$
003A98$_H$ to 003A9F$_H$	003C98$_H$ to 003C9F$_H$	003E98$_H$ to 003E9F$_H$	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$
003AA0$_H$ to 003AA7$_H$	003CA0$_H$ to 003CA7$_H$	003EA0$_H$ to 003EA7$_H$	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$
003AA8$_H$ to 003AAF$_H$	003CA8$_H$ to 003CAF$_H$	003EA8$_H$ to 003EAF$_H$	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$
003AB0$_H$ to 003AB7$_H$	003CB0$_H$ to 003CB7$_H$	003EB0$_H$ to 003EB7$_H$	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$

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Address			Register	Abbreviation	Read/ Write	Initial Value
CAN0	CAN1	CAN2				
003AB8H to 003ABFH	003CB8H to 003CBFH	003EB8H to 003EBFH	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXXB to XXXXXXXXB
003AC0H to 003AC7H	003CC0H to 003CC7H	003EC0H to 003EC7H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXXB to XXXXXXXXB
003AC8H to 003ACFH	003CC8H to 003CCFH	003EC8H to 003ECFH	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXXB to XXXXXXXXB
003AD0H to 003AD7H	003CD0H to 003CD7H	003ED0H to 003ED7H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXXB to XXXXXXXXB
003AD8H to 003ADFH	003CD8H to 003CDFH	003ED8H to 003EDFH	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXXB to XXXXXXXXB
003AE0H to 003AE7H	003CE0H to 003CE7H	003EE0H to 003EE7H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXXB to XXXXXXXXB
003AE8H to 003AEFH	003CE8H to 003CEFH	003EE8H to 003EEFH	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXXB to XXXXXXXXB
003AF0H to 003AF7H	003CF0H to 003CF7H	003EF0H to 003EF7H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXXB to XXXXXXXXB
003AF8H to 003AFFH	003CF8H to 003CFFH	003EF8H to 003EFFH	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXXB to XXXXXXXXB

■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt cause	EI^2OS support	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	#08	$FFFFDC_H$	—	—
INT9 instruction	N/A	#09	$FFFFD8_H$	—	—
Exception processing	N/A	#10	$FFFFD4_H$	—	—
CAN 0 Receive	N/A	#11	$FFFFD0_H$	ICR00	$0000B0_H$
CAN 0 Transmit/Node status	N/A	#12	$FFFFCC_H$		
CAN 1 Receive	N/A	#13	$FFFFC8_H$	ICR01	$0000B1_H$
CAN 1 Transmit/Node status	N/A	#14	$FFFFC4_H$		
External interrupt (INT0/INT1)	*1	#15	$FFFFC0_H$	ICR02	$0000B2_H$
Timebase timer	N/A	#16	$FFFFBC_H$		
16-bit reload timer 0	*1	#17	$FFFFB8_H$	ICR03	$0000B3_H$
8/10-bit A/D converter	*1	#18	$FFFFB4_H$		
Input/output timer	N/A	#19	$FFFFB0_H$	ICR04	$0000B4_H$
External interrupt (INT2/INT3)	*1	#20	$FFFFAC_H$		
Serial I/O	*1	#21	$FFFFA8_H$	ICR05	$0000B5_H$
8/16-bit PPG timer 0/1/2/3	N/A	#22	$FFFFA4_H$		
Input capture 0	*1	#23	$FFFFA0_H$	ICR06	$0000B6_H$
External interrupt (INT4/INT5)	*1	#24	$FFFF9C_H$		
CAN 2 Receive	N/A	#25	$FFFF98_H$	ICR07	$0000B7_H$
CAN 2 Transmit/Node status	N/A	#26	$FFFF94_H$		
External interrupt (INT6/INT7)	*1	#27	$FFFF90_H$	ICR08	$0000B8_H$
Monitoring timer	N/A	#28	$FFFF8C_H$		
Input capture 1	*1	#29	$FFFF88_H$	ICR09	$0000B9_H$
Input capture 2/3	*1	#30	$FFFF84_H$		
8/16-bit PPG timer 4/5/6/7	N/A	#31	$FFFF80_H$	ICR10	$0000BA_H$
Output compare 0	*1	#32	$FFFF7C_H$		
Output compare 1	*1	#33	$FFFF78_H$	ICR11	$0000BB_H$
Input capture 4/5	*1	#34	$FFFF74_H$		
Output compare 2/3-input capture 6/7	*1	#35	$FFFF70_H$	ICR12	$0000BC_H$
16-bit reload timer 1	*1	#36	$FFFF6C_H$		
UART 0 Receive	*2	#37	$FFFF68_H$	ICR13	$0000BD_H$
UART 0 Transmit	*1	#38	$FFFF64_H$		
UART 1 Receive	*2	#39	$FFFF60_H$	ICR14	$0000BE_H$
UART 1 Transmit	*1	#40	$FFFF5C_H$		

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Interrupt cause	EI^2OS support	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Flash memory	N/A	#41	$FFFF58_H$	ICR15	$0000BF_H$
Delayed interrupt generation module	N/A	#42	$FFFF54_H$H		

*1 : The interrupt request flag is cleared by the EI^2OS interrupt clear signal.

*2 : The interrupt request flag is cleared by the EI^2OS interrupt clear signal. A stop request is available.

Notes : • N/A : The interrupt request flag is not cleared by the EI^2OS interrupt clear signal.
- For a peripheral module with two interrupt causes for a single interrupt number, both interrupt request flags are cleared by the EI^2OS interrupt clear signal.
- At the end of EI^2OS, the EI^2OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI^2OS and in the meantime another interrupt flag is set by hardware event, the later event is lost because the flag is cleared by the EI^2OS clear signal caused by the first event. So it is recommended not to use the EI^2OS for this interrupt number.
- If EI^2OS is enabled, EI^2OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt causes share the same EI^2OS descriptor which should be unique for each interrupt cause. For this reason, when one interrupt cause uses the EI^2OS, the other interrupt should be disabled.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

($V_{SS} = AV_{SS} = 0.0$ V)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$ *1
	AVRH, AVRL	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq$ AVRH / AVRL, AVRH $\geq$ AVRL*1
Input voltage	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Output voltage	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Maximum clamp current	I_{CLAMP}	– 2.0	+ 2.0	mA	*6
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	*6
“L” level maximum output current	I_{OL}	—	15	mA	*3
“L” level average output current	I_{OLAV}	—	4	mA	*4
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	*5
“H” level maximum output current	I_{OH}	—	–15	mA	*3
“H” level average output current	I_{OHAV}	—	–4	mA	*4
“H” level total maximum output current	ΣI_{OH}	—	–100	mA	
“H” level total average output current	ΣI_{OHAV}	—	–50	mA	*5
Power consumption	P_D	—	500	mW	MB90F443G
		—	400	mW	MB90F443G (under development)
Operating temperature	T_A	–40	+ 105	°C	
Storage temperature	Tstg	–55	+ 150	°C	

*1 : AV_{CC}, AVRH, and AVRL shall never exceed V_{CC}. AVRH, AVRL shall never exceed AV_{CC}. Also, AVRL shall never exceed AVRH.

*2 : V_I and V_O shall never exceed V_{CC} + 0.3 V. V_I shall never exceed the specified ratings. However if the maximum current to/ from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*3 : Maximum output current specifies the peak value of the corresponding pin.

*4 : The average output current specifies the average current of corresponding pins within 100 ms. (operation current × operation rate = average value)

*5 : The total average output current specifies the average current of all corresponding pins within 100 ms. (operation current × operation rate = average value)

*6 : • Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0
• Use within recommended operating conditions.
• Use at DC voltage (current) .

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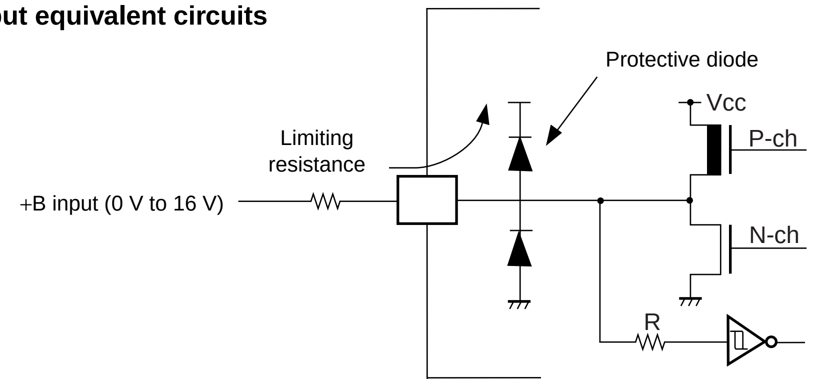
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits.

- **Input/Output equivalent circuits**



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.5	5.0	5.5	V	Under normal operation
		3.0	—	5.5	V	Retains status at the time of operation stop
Smoothing capacitor	C_S	0.022	0.1	1.0	µF	*
Operating temperature	T_A	–40	—	+105	°C	

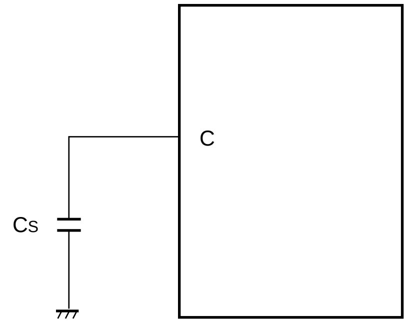
* : Use a ceramic capacitor or capacitor of better AC characteristics. Capacitor at the V_{CC} should be greater than this capacitor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

• **C pin connection circuit**



3. DC Characteristics

(V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IHS}	CMOS Hysteresis input pin	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHA}	AUTOMOTIVE input pin	—	0.8 V_{CC}	—	—	V	
	V_{IH}	TTL input pin	—	2.0	—	—	V	
	V_{IHM}	MD input pin	—	V_{CC} – 0.3	—	V_{CC} + 0.3	V	
Input L voltage	V_{ILS}	CMOS Hysteresis input pin	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
	V_{ILA}	AUTOMOTIVE input pin	—	—	—	0.5 V_{CC}	V	
	V_{IL}	TTL input pin	—	—	—	0.8	V	
	V_{ILM}	MD input pin	—	V_{SS} – 0.3	—	V_{SS} + 0.3	V	
Output H voltage	V_{OH}	All output pins	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
Output L voltage	V_{OL}	All output pins	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
Input leak current	I_{IL}	—	V_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	–5	—	+ 5	μA	

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(V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I_{CC}	V_{CC}	V_{CC} = 5.0 V Internal frequency : 16 MHz, At normal operating	—	45	60	mA	
			V_{CC} = 5.0 V Internal frequency : 16 MHz, At flash programming / erasing	—	50	70	mA	
	I_{CCS}		V_{CC} = 5.0 V Internal frequency : 16 MHz, At sleep	—	13	22	mA	
	I_{CCL}		V_{CC} = 5.0 V Internal frequency : 8 kHz, At sub operation T_A = + 25 °C	—	50	100	µA	MB90443G (under devel-opment)
				—	300	500	µA	MB90F443G
	I_{CCLS}		V_{CC} = 5.0 V Internal frequency : 8 kHz, At sub sleep T_A = + 25 °C	—	15	40	µA	
	I_{CCT}		V_{CC} = 5.0 V Internal frequency : 8 kHz, At watch mode T_A = + 25 °C	—	7	25	µA	
	I_{CTS}		V_{CC} = 5.0 V Internal frequency : 2 MHz, At timer base timer mode T_A = + 25 °C	—	600	1200	µA	
	I_{CCH}		At stop mode, T_A = + 25 °C	—	5	20	µA	
Input capacity	C_{IN}	Other than AV_{CC}, AV_{SS}, AVRH, AVRL, C, V_{CC}, V_{SS}	—	—	10	15	pF	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, $\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	

* : The power supply current is measured with an external clock.

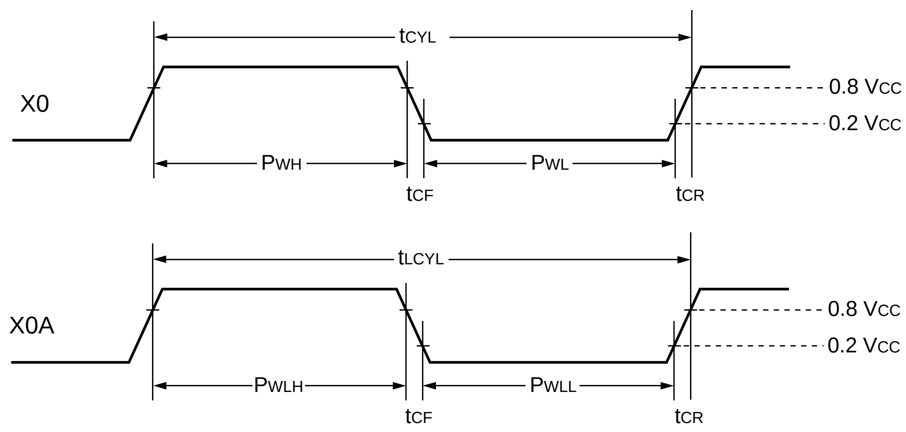
4. AC Characteristics

(1) Clock Timing

(V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

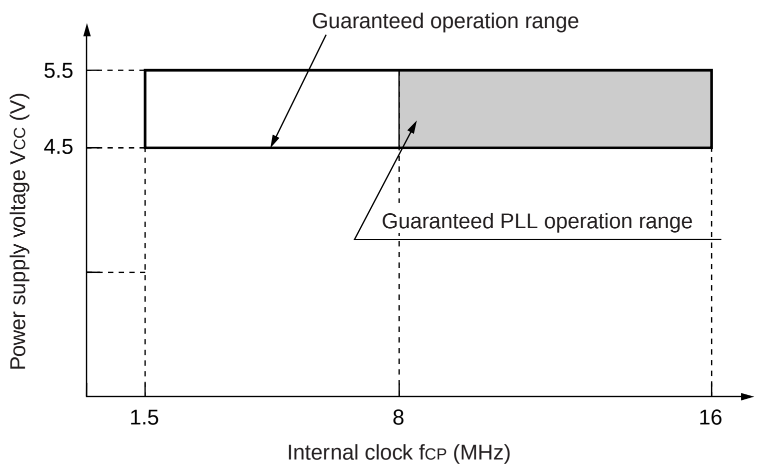
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	16	MHz	
	f_{CL}	X0A, X1A	—	32.768	—	kHz	
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	
	t_{LCYL}	X0A, X1A	—	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P_{WLH}, P_{WLL}	X0A	—	15.2	—	µs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Internal operating clock frequency	f_{CP}	—	1.5	—	16	MHz	When using main clock
	f_{LCP}	—	—	8.192	—	kHz	When using sub-clock
Internal operating clock cycle time	t_{CP}	—	62.5	—	666	ns	When using main clock
	t_{LCP}	—	—	122.1	—	µs	When using sub-clock

• **Clock Timing**

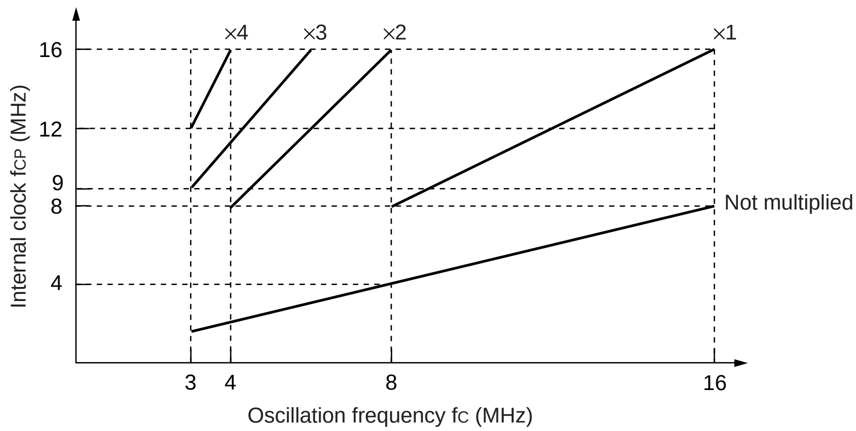


- **Guaranteed PLL operation range**

Relationship between internal operation clock frequency and power supply voltage



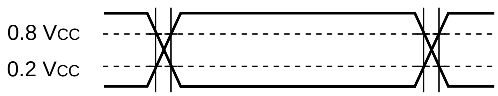
Relationship between oscillation frequency and internal operating clock frequency



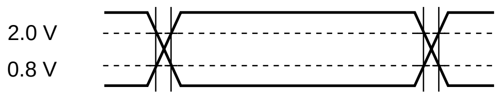
The AC ratings are measured for the following measurement reference voltages.

- Input signal waveform

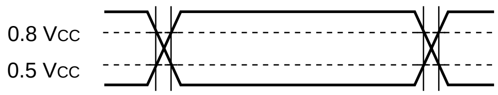
CMOS Hysteresis Input Pin



TTL Input Pin

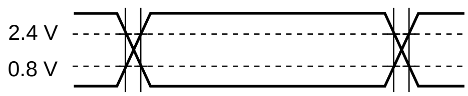


AUTOMOTIVE Input Pin



- Output signal waveform

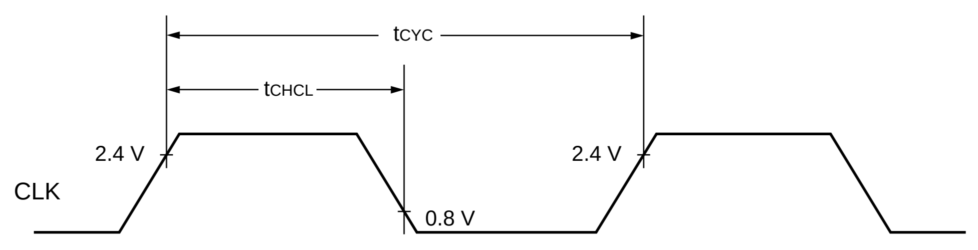
Output Pin



(2) Clock Output Timing

(V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	V_{CC} = 5 V ± 10%	62.5	—	ns	
CLK ↑ → CLK ↓	t_{CHCL}			20	—	ns	

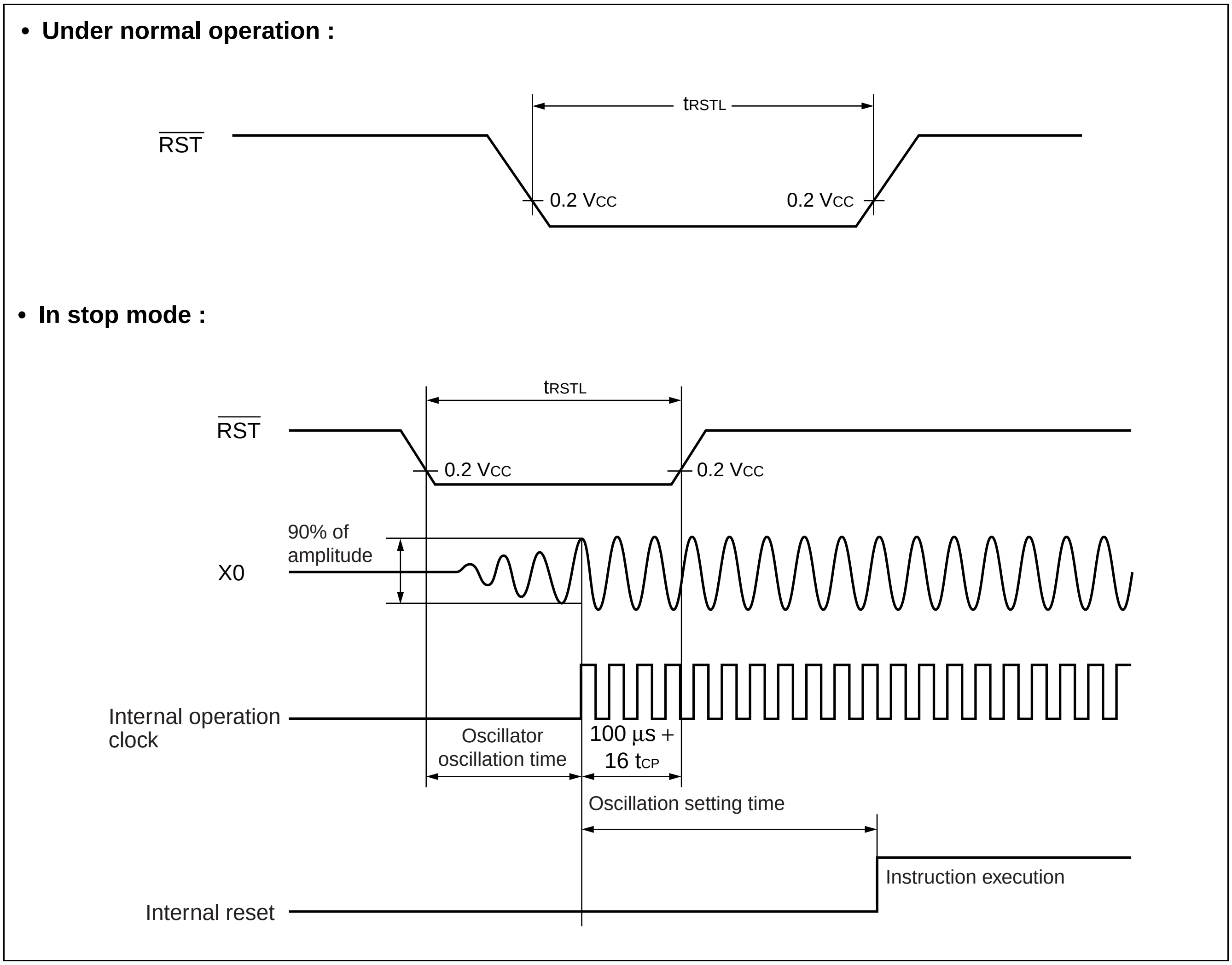


(3) Reset Input Timing and Hardware Stand-by Input Timing

(V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	16 t_{CP}	—	ns	Under normal operation
			Oscillation time of oscillator + 100 µs + 16 t_{CP}	—	—	In stop mode, watch mode, sub-clock mode, sub-sleep mode

Note: • Oscillator oscillation time is the time that amplitude reached 90%. For a crystal oscillator, the oscillation time is between several ms to tens of ms; for a FAR/ceramic oscillator, the oscillation time is between hundreds of µs to several ms, and for an external clock the oscillation time is 0 ms.
• Any reset can not fully initialize the Flash Memory if it is performing the automatic algorithm.



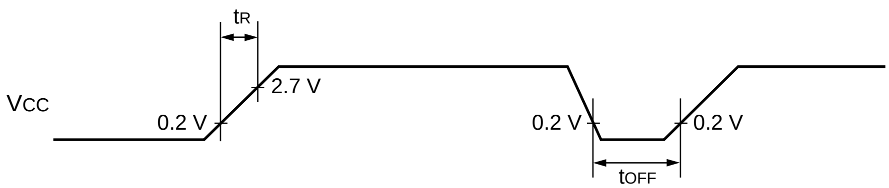
(4) Power-on Reset

(V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power supply rising time	t_R	V_{CC}	—	0.05	30	ms	*
Power supply cut-off time	t_{OFF}	V_{CC}		50	—	ms	Due to repeated operations

* : V_{CC} must be kept lower than 0.2 V before power-on.

Note : The above values are used for causing a power-on reset.
Some registers in the device are initialized only upon a power-on reset. To initialize these registers, turn the power supply on using the above values.



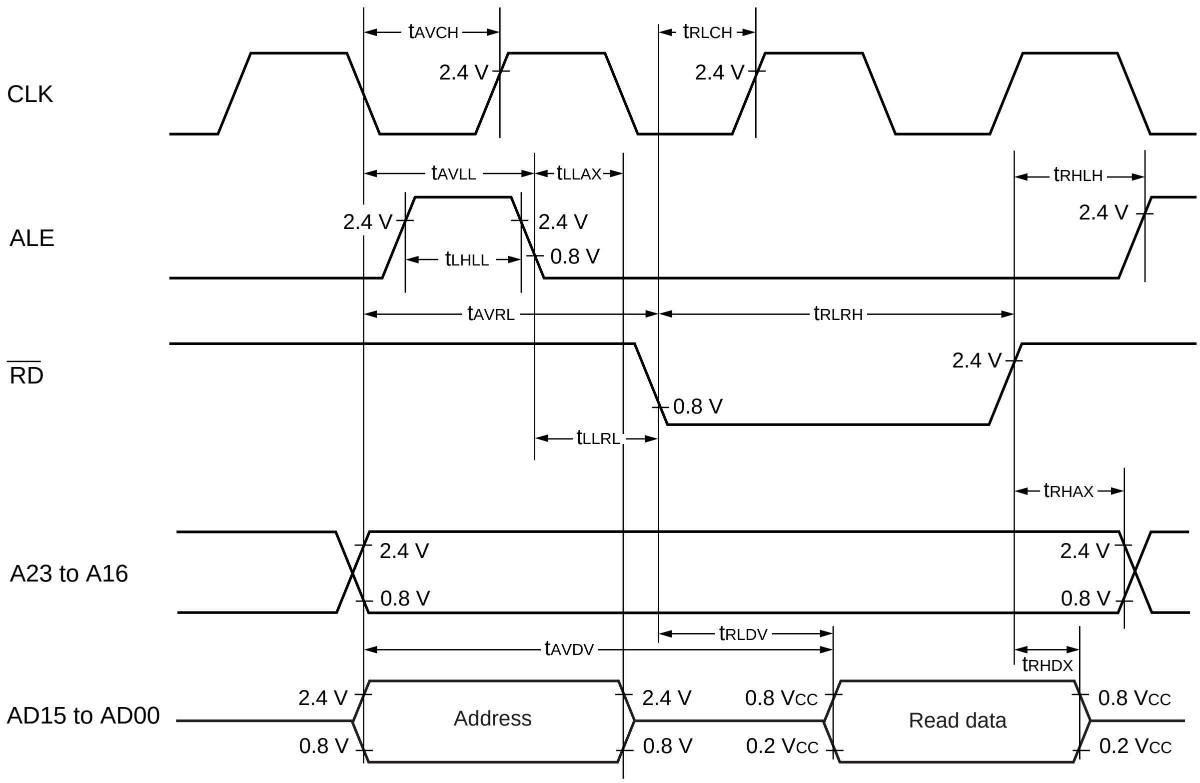
Sudden changes in the power supply voltage may cause a power on reset. We recommend to raise the voltage smoothly to suppress fluctuation during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.

(5) Bus Timing (Read)

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
ALE pulse width	t_{LHLL}	ALE	t_{CP} / 2 – 20	—	ns	
Valid address → ALE ↓ time	t_{AVLL}	ALE, A16 to A23, AD00 to AD15	t_{CP} / 2 – 20	—	ns	
ALE ↓ → Address valid time	t_{LLAX}	ALE, AD00 to AD15	t_{CP} / 2 – 15	—	ns	
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	A16 to A23, AD00 to AD15, $\overline{RD}$	t_{CP} – 15	—	ns	
Valid address → Valid data input	t_{AVDV}	A16 to A23, AD00 to AD15	—	5 t_{CP} / 2 – 60	ns	
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$	3 t_{CP} / 2 – 20	—	ns	
$\overline{RD}$ ↓ → Valid data input	t_{RLDV}	$\overline{RD}$, AD00 to AD15	—	3 t_{CP} / 2 – 60	ns	
$\overline{RD}$ ↑ → Data hold time	t_{RHDX}	$\overline{RD}$, AD00 to AD15	0	—	ns	
$\overline{RD}$ ↓ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE	t_{CP} / 2 – 15	—	ns	
$\overline{RD}$ ↑ → Address valid time	t_{RHAX}	$\overline{RD}$, A16 to A23	t_{CP} / 2 – 10	—	ns	
Valid address → CLK ↑ time	t_{AVCH}	A16 to A23, AD00 to AD15, CLK	t_{CP} / 2 – 20	—	ns	
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK	t_{CP} / 2 – 20	—	ns	
ALE ↓ → $\overline{RD}$ ↓ time	t_{LLRL}	ALE, $\overline{RD}$	t_{CP} / 2 – 15	—	ns	

- **Bus Timing** (**Read**)

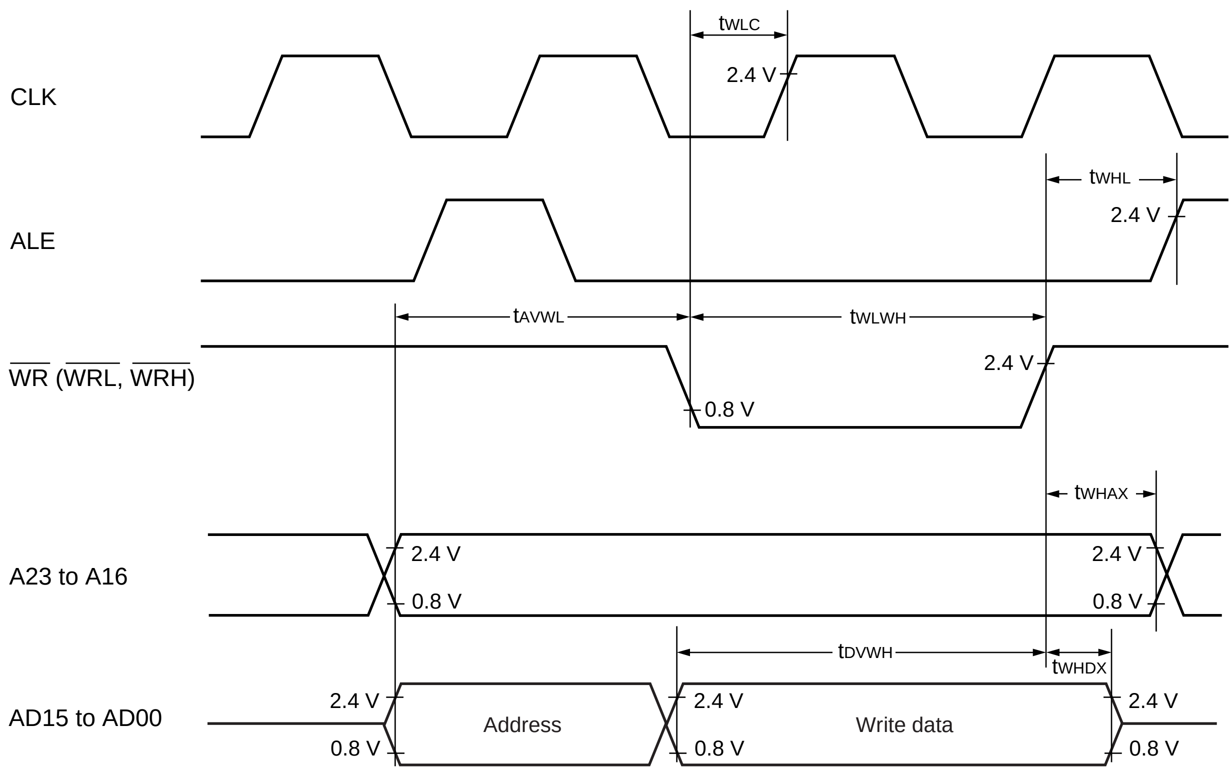


(6) Bus Timing (Write)

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	A16 to A23, AD00 to AD15, $\overline{WR}$	t_{CP} – 15	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$	3 t_{CP} / 2 – 20	—	ns	
Valid data output → $\overline{WR}$ ↑ time	t_{DVWH}	AD00 to AD15, $\overline{WR}$	3 t_{CP} / 2 – 20	—	ns	
$\overline{WR}$ ↑ → Data hold time	t_{WHDX}	AD00 to AD15, $\overline{WR}$	20	—	ns	
$\overline{WR}$ ↑ → Address valid time	t_{WHAX}	A16 to A23, $\overline{WR}$	t_{CP} / 2 – 10	—	ns	
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE	t_{CP} / 2 – 15	—	ns	
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK	t_{CP} / 2 – 20	—	ns	

- **Bus Timing (Write)**



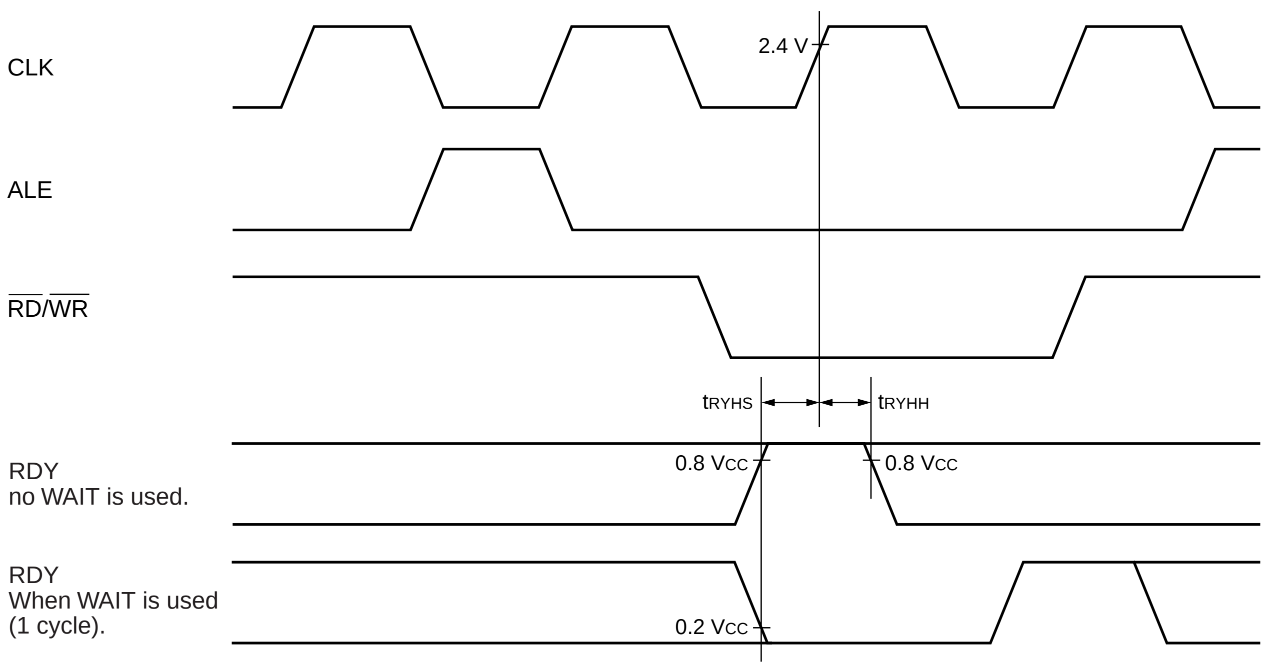
(7) Ready Input Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
RDY setup time	t_{RYHS}	RDY	45	—	ns	
RDY hold time	t_{RYHH}	RDY	0	—	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.

• **Ready Input Timing**



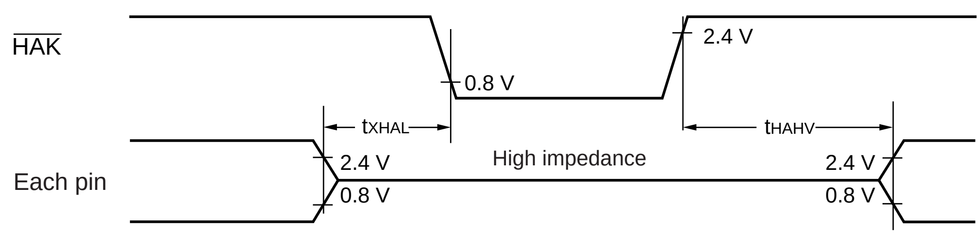
(8) Hold Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Pin floating → $\overline{HAK}$ ↓ time	t_{XHAL}	$\overline{HAK}$	30	t_{CP}	ns	
$\overline{HAK}$ ↑ → Pin valid time	t_{HAHV}	$\overline{HAK}$	t_{CP}	2 t_{CP}	ns	

Note : More than 1 machine cycle is needed before $\overline{HAK}$ changes after HRQ pin is fetched.

• **Hold Timing**



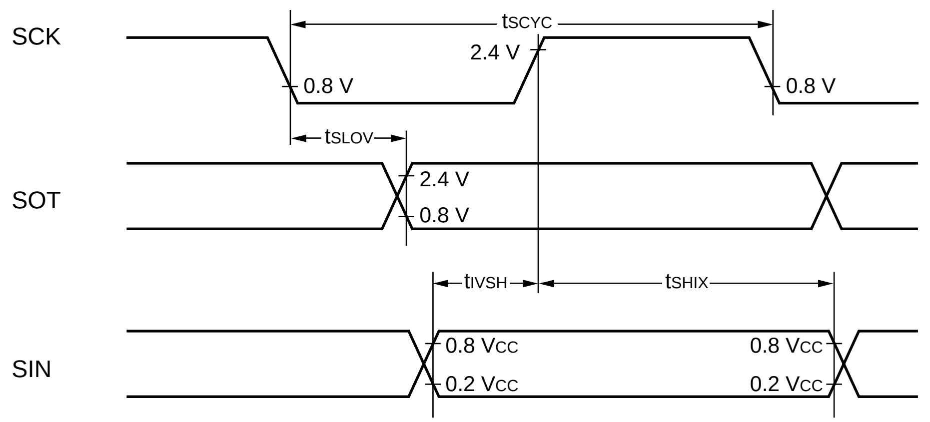
(9) UART0/1, Serial I/O Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

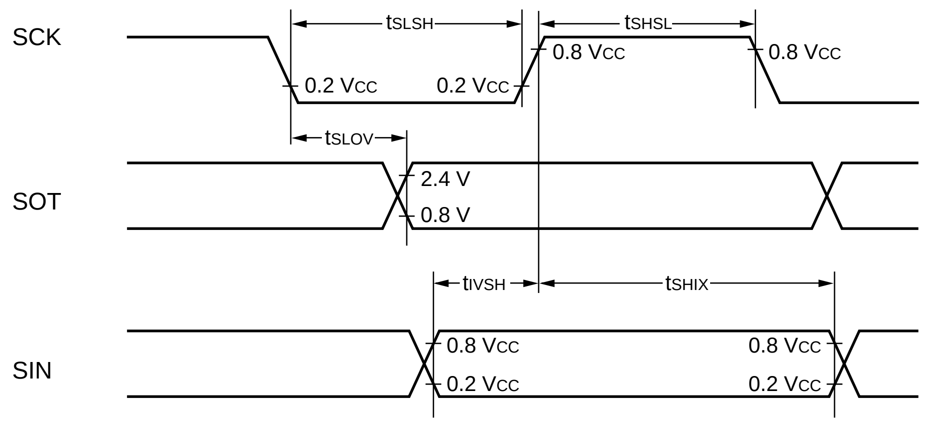
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2	An output pin of internal sift clock mode C_L = 80 pF + 1 TTL.	8 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		–80	+80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		100	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK2	An output pin of external sift clock mode C_L = 80 pF + 1 TTL.	4 t_{CP}	—	ns	
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK2		4 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		—	150	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	

Notes : • AC ratings in CLK synchronous mode.
• C_L is load capacitance value connected to pins when testing.

- **Internal Shift Clock Mode**



- **External Shift Clock Mode**

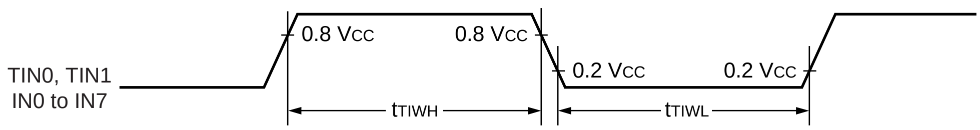


(10) Timer Related Resource Input Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	4 t_{CP}	—	ns	
	t_{TIWL}	IN0 to IN7					

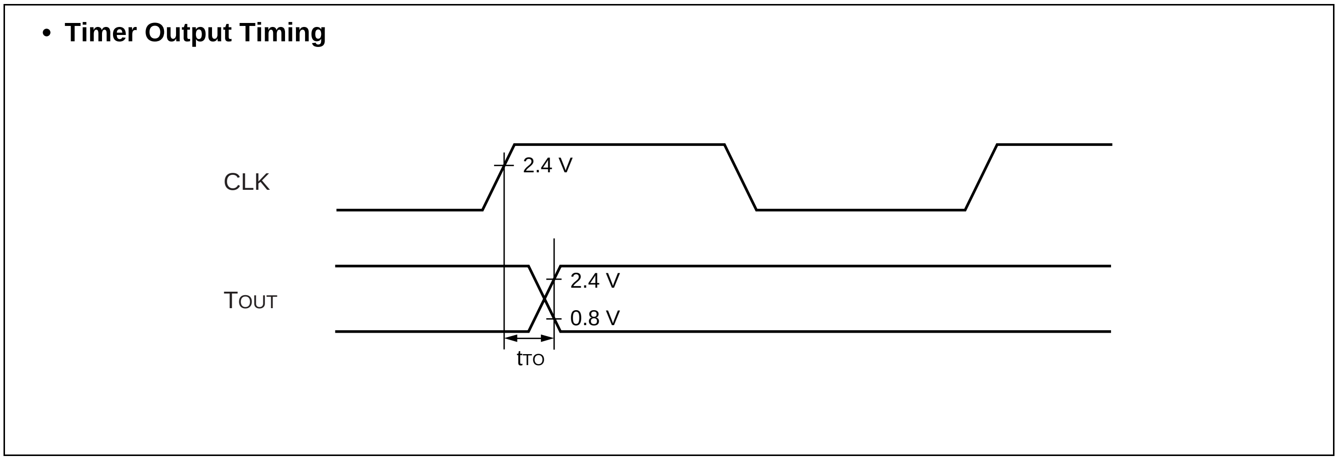
• **Timer Input Timing**



(11) Timer Related Resource Output Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

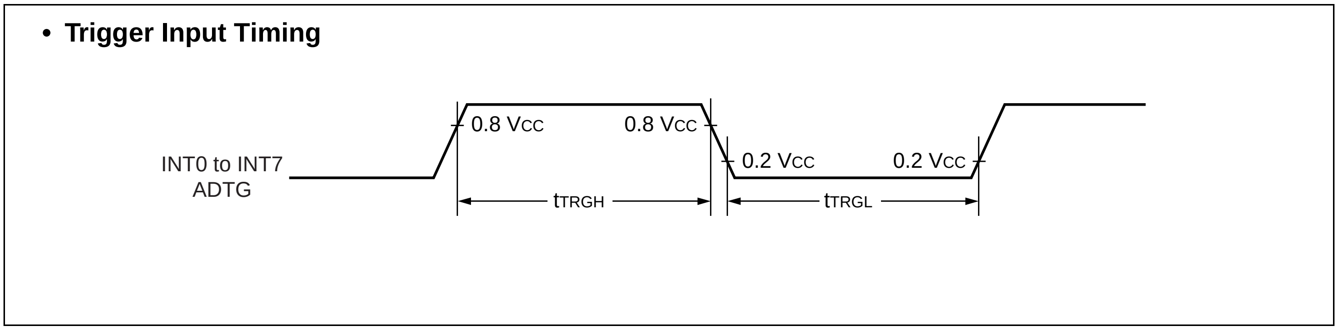
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
CLK ↑ → T_{OUT} transition time	t_{TO}	TOT0 to TOT1, PPG0 to PPG3	—	30	—	ns	



(12) Trigger Input Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	INT0 to INT7, ADTG	—	5 t_{CP}	—	ns	normal operation
				1	—	µs	stop mode



5. A/D Converter

- Electrical Characteristics

(V_{CC} = AV_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, 3.0 V ≤ AVRH − AVRL, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±5.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential linearity error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AVRL − 3.5 LSB	AVRL + 0.5 LSB	AVRL + 4.5 LSB	V	1 LSB = (AVRH − AVRL) / 1024 [V]
Full scale transition voltage	V_{FST}	AN0 to AN7	AVRH − 6.5 LSB	AVRH − 1.5 LSB	AVRH + 1.5 LSB	V	
Compare time	—	—	66 t_{CP}	—	—	ns	Machine clock of 16 MHz
Sampling time	—	—	32 t_{CP}	—	—	ns	
Analog port input current	I_{AIN}	AN0 to AN7	—	—	10	μA	
Analog input voltage	V_{AIN}	AN0 to AN7	AVRL	—	AVRH	V	
Reference voltage	—	AVRH	AVRL + 2.7 LSB	—	AV_{CC}	V	
	—	AVRL	0	—	AVRH − 2.7 LSB	V	
Power supply current	I_A	AV_{CC}	—	2	6	mA	
	I_{AH}	AV_{CC}	—	—	5	μA	*
Reference voltage supply current	I_R	AVRH	—	0.9	1.3	mA	
	I_{RH}	AVRH	—	—	5	μA	*
Offset between channels	—	AN0 to AN7	—	—	4	LSB	

* : Specifies the power supply current (V_{CC} = AV_{CC} = AVRH = 5.0 V) when the A/D converter is inactive and the CPU has been stopped.

- **A/D Converter Glossary**

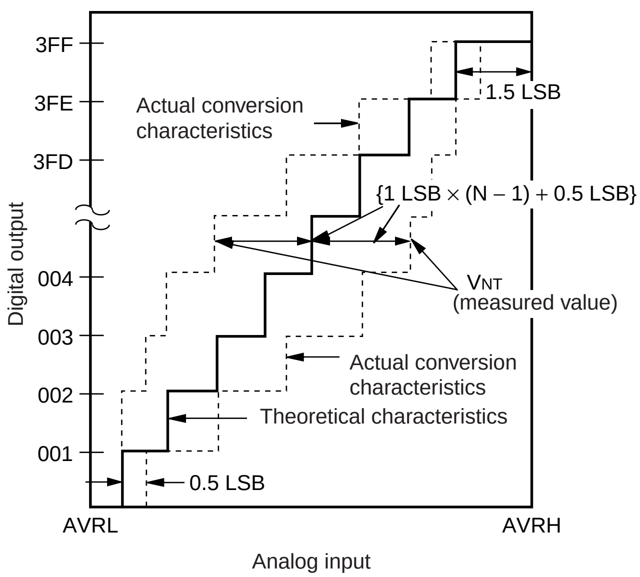
Resolution : Analog changes that are identifiable with the A/D converter

Linearity error : The deviation of the straight line connecting the zero transition point (“00 0000 0000” to “00 0000 0001”) with the full-scale transition point (“11 1111 1110” to “11 1111 1111”) from actual conversion characteristics.

Differential linearity error : The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value.

Total error : The difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error, and linearity error.

Total error



$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\text{ LSB} \times (N - 1) + 0.5\text{ LSB}\}}{1\text{ LSB}} \text{ [LSB]}$$

$$1\text{ LSB} = \text{(theoretical value) } \frac{AVRH - AVRL}{1024} \text{ [V]}$$

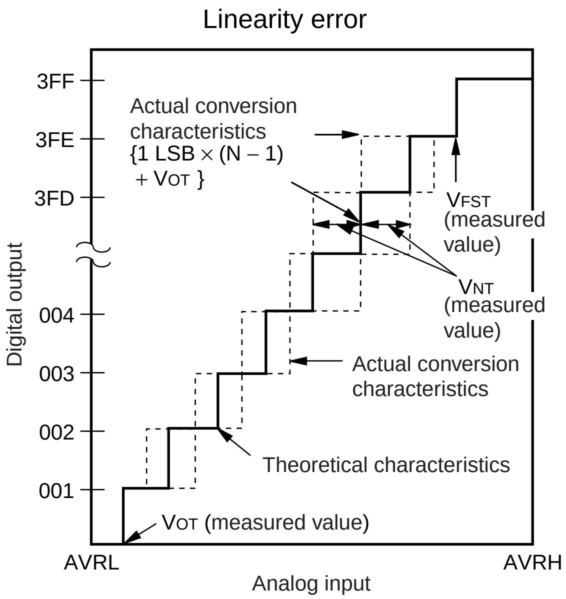
V_{OT} (theoretical value) $= AVRL + 0.5$ LSB [V]

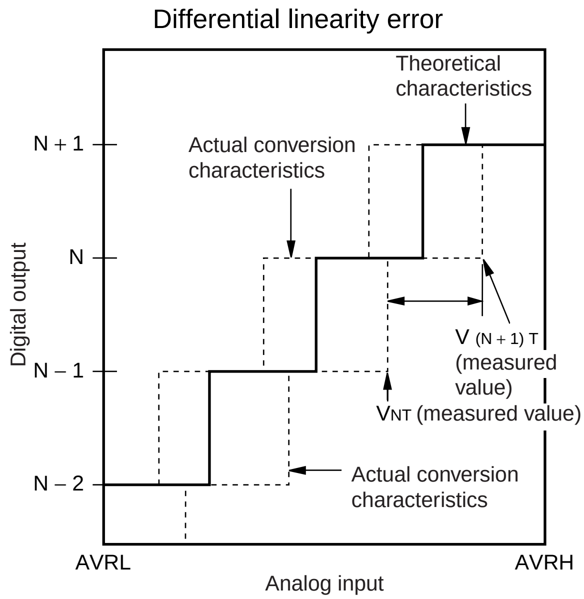
V_{FST} (theoretical value) $= AVRH - 1.5$ LSB [V]

V_{NT} : The voltage at a transition of digital output from (N – 1) to N.

(Continued)

(Continued)





$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + V_{OT}\}}{1\ \text{LSB}} \ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022} \ [\text{V}]$$

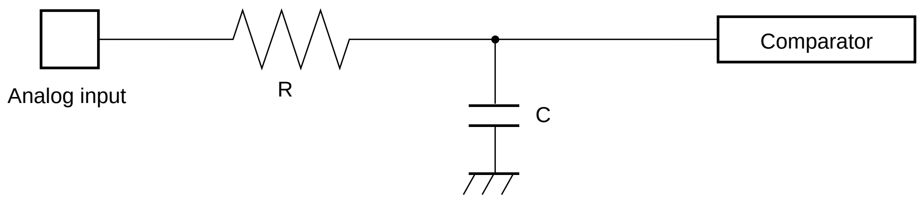
V_{OT} : Voltage at transition of digital output 000_H to 001_H.
V_{FST} : Voltage at transition of digital output $3FE_H$ to $3FF_H$.

• Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions :
Output impedance values of the external circuit of about 5 kΩ or lower are recommended.
If external capacitors are used, a capacitance of several thousand times the internal capacitor value is recommended in order to minimize the effect of voltage distribution between the external and internal capacitor.

Note: If the output impedance of the external circuit is too high, the sampling time for analog voltages may not be sufficient (sampling period = 2.00 µs @ machine clock of 16 MHz) . The output impedance of the external circuit can be set to approx. 15kΩ or lower , when the sampling period is set to 4.00 µs.

• Analog Input Circuit Model



MB90F443G, MB90V440G	R ≒ 3.2 kΩ, C ≒ 30 pF
MB90443G (Under development)	R ≒ 2.6 kΩ, C ≒ 28 pF

• **About Error**

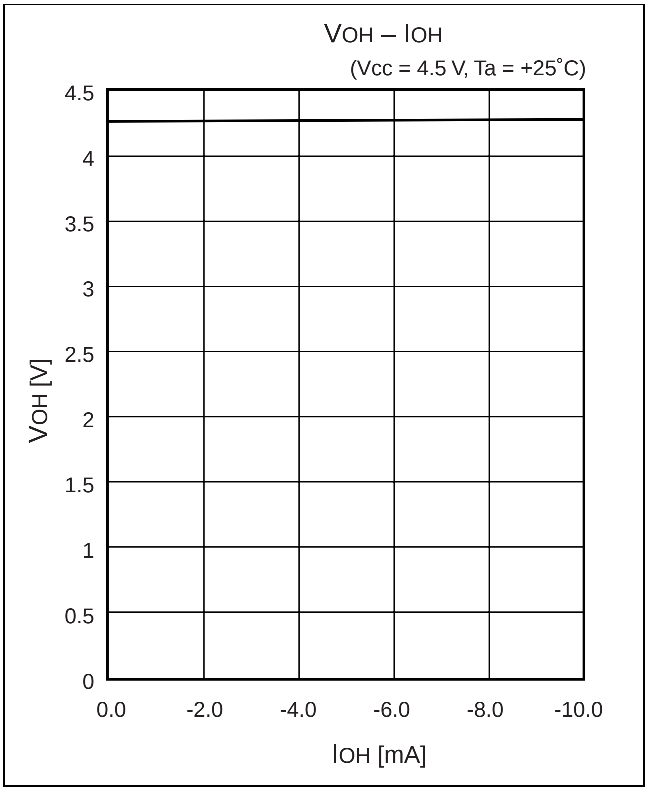
The smaller the absolute value of | AVRH – AVRL | is, the greater the relative error is.

6. Flash Memory Program/Erase Characteristics

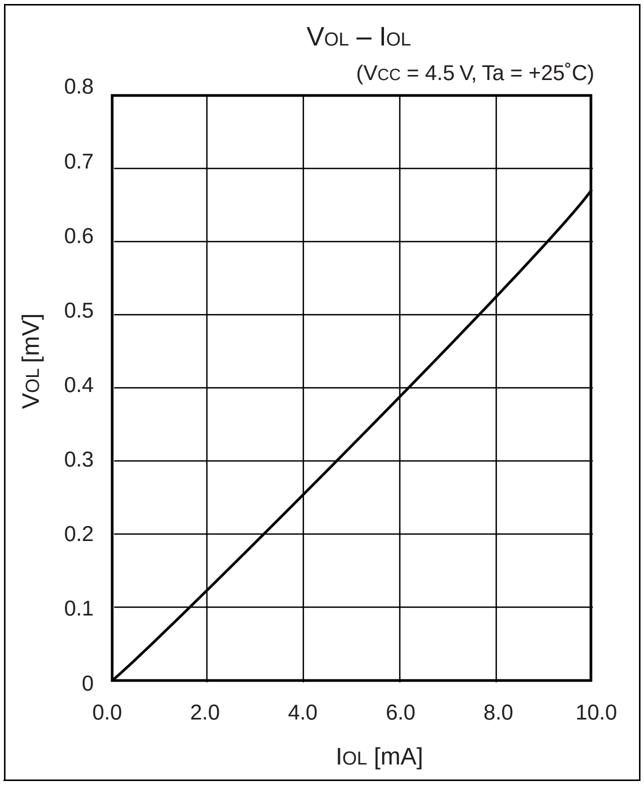
Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = + 25 °C V_{CC} = 5.0 V	—	1	15	s	Excludes 00H programming prior erasure
Chip erase time		—	5	—	s	Excludes 00H programming prior erasure
Word (16 bit width) programming time		—	16	3,600	µs	Excludes system-level overhead
Erase/Program cycle	—	10,000	—	—	cycle	

■ EXAMPLE CHARACTERISTICS

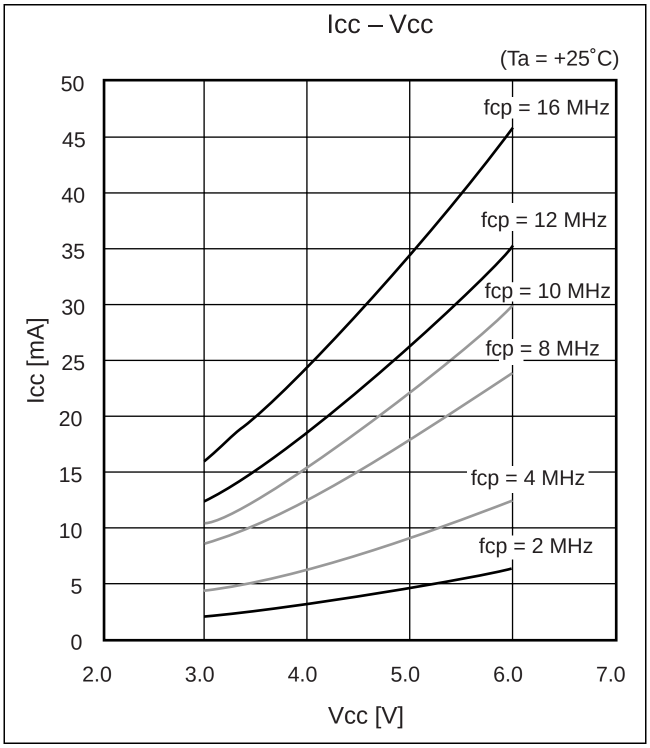
• "H" Level Output Voltage

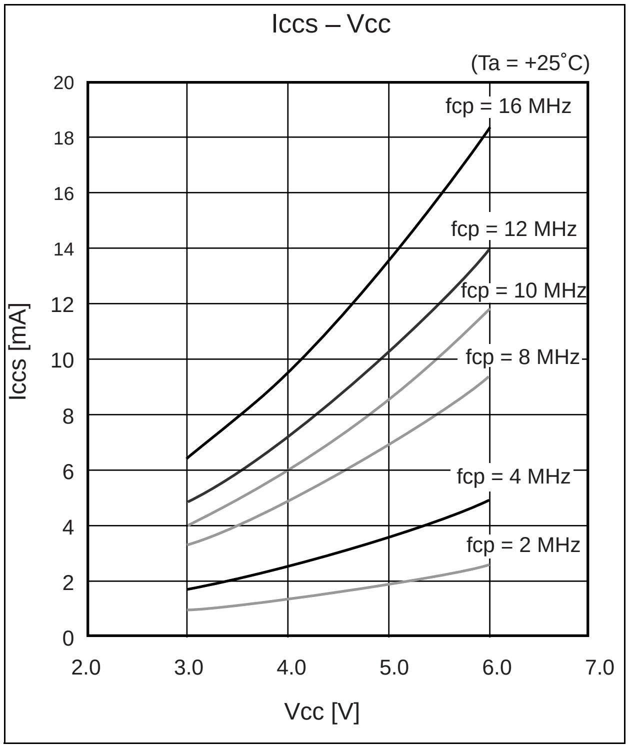


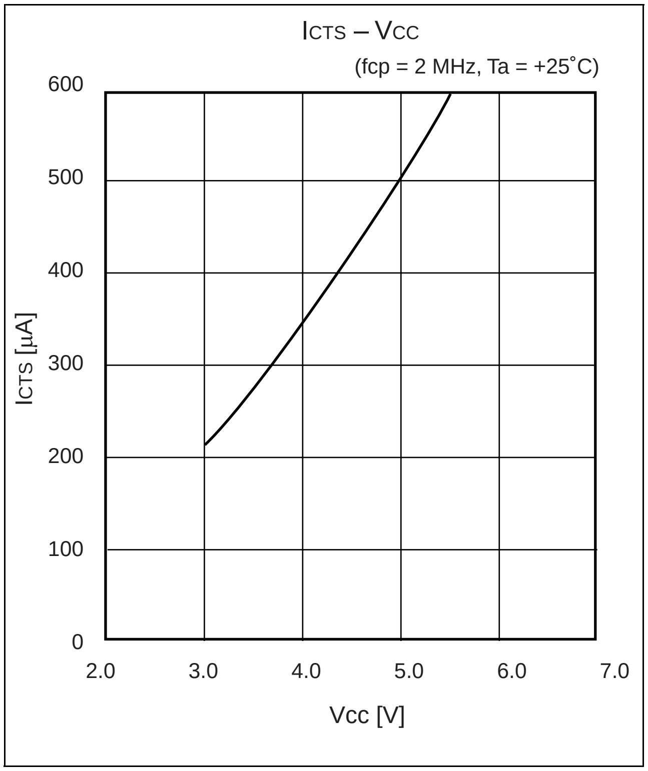
• "L" Level Output Voltage

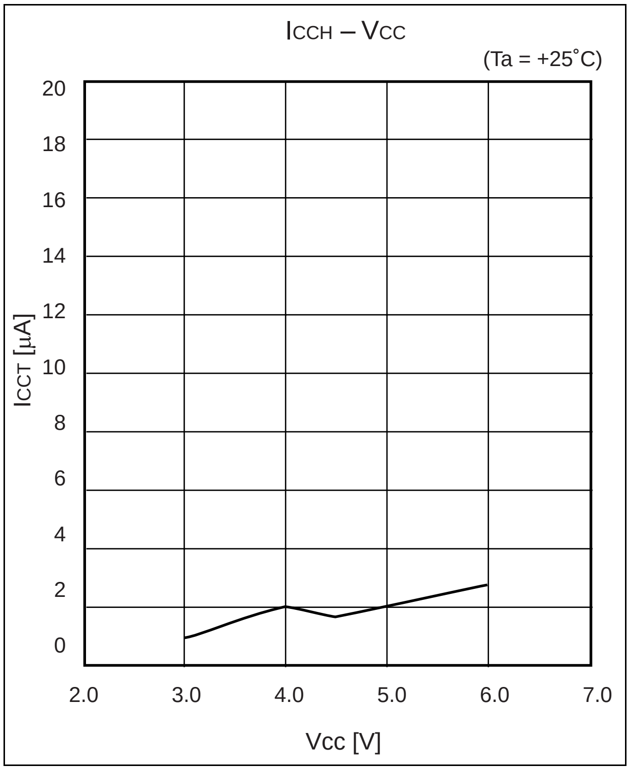


• Power Supply Current (FLASH)









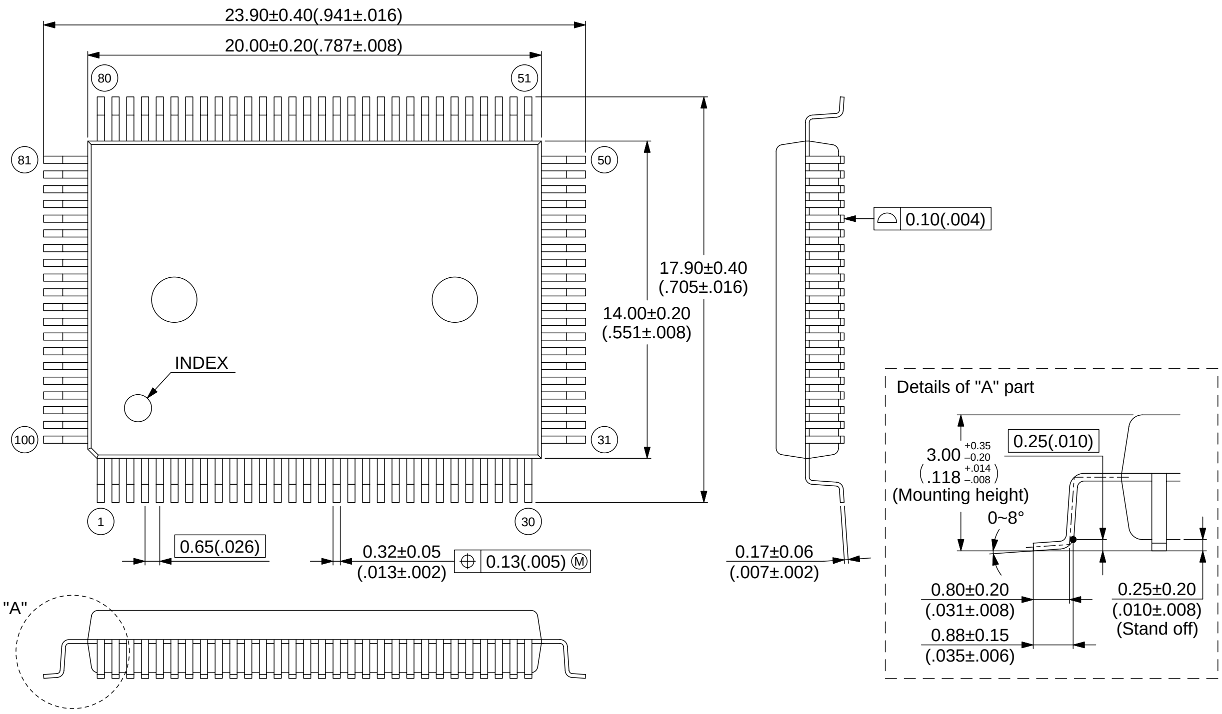
■ ORDERING INFORMATION

Part number	Package	Remarks
MB90443GPF (under development) MB90F443GPF	100-pin Plastic QFP (FPT-100P-M06)	
MB90V440GCR	256-pin Ceramic PGA (PGA-256C-A01)	For evaluation

■ PACKAGE DIMENSIONS

100-pin Plastic QFP
(FPT-100P-M06)

Note : Pins width and pins thickness include plating thickness.



Dimensions in mm (inches)

FUJITSU LIMITED

F0204