Revision: 0.03A
2001/10/12

# MX88L250EC-X
# MX88L250EC-S
# MX88L250EC-D
# Data Sheet

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## General Description

MX88L250EC Series is the Low Cost yet High Performance Solution for Flat Panel Display application. Applying Macronix's Smartscaling$^{TM}$–$2^{+}$ filter, it provides high quality scaled video image and format conversion capability.

## Applications

- XGA/SXGA LCD monitors

## Features

### General Features

- MX88L250EC-X and MX88L250EC-S are fully Pin to Pin Compatible.
- Convert PC video signal into flat panel display device timing and resolution.
- Built-in Line Buffer to provide Fame-Buffer-Less solution.
- Support Clock, Phase, Horizontal and Vertical position adjustments.
- Support Auto-Tracking and Auto-Position capabilities (SmartTracking$^{TM}$ Technology).
- Support Auto-Gain capability for input image
- Arbitrary scaling from 1 to 32 times with filters (SmartScaling$^{TM}$ – $2^{+}$ Technology).
- Support Edge Filter control.
- Built-in OSD generator with 64 ROM /128 programmable RAM fonts, mixer with Color Palette, Color Key and Alpha Blending.
- Provide 90-degree Rotation for internal OSD to support Portrait direction display.
- On-chip Digital Brightness and Contrast adjustments.
- On-chip Digital Gamma Correction for panel compensation.
- Support Temporal Dithering capability to make 18 bit video as good as 24 bit quality.
- Support "Test mode" function which internally generates some test patterns, including gray, saw, and cross talk, for output.

### Input

- MX88L250EC-X supports Single port 24bit, PC video up to XGA operation mode.
- MX88L250EC-S supports Single port 24bit, PC video up to SXGA operation mode.

- MX88L250EC-D supports Dual port 48bit, PC video up to SXGA operation mode
- Support Composite Sync. input.
- Support H/V Sync. Polarity and Pulse Width information for mode detection.
- Support H/V Sync. Interrupt for power management requirement.

**Output**

- Support TFT LCD panel in following resolution and frequency.

| Resolution | 800x600 | 1024x768 | 1280x1024 |
|---|---|---|---|
| Horizontal frequency (KHz) | 20 ~ 55 | 20 ~ 70 | 80 |
| Vertical frequency (Hz) | 50 ~ 75 | 50 ~ 75 | 75 |
| Dot clock (MHz) | 32.5 ~ 60 | 25 ~ 80 | 140 |

- Single (18/24) and Dual (36/48) bit RGB data output.
- Support Inverse, Delay and Frequency adjustments for LCD panel clock.
- Support programmable H/V sync. and LDTG timing for LCD panel.
- Support two PWM outputs

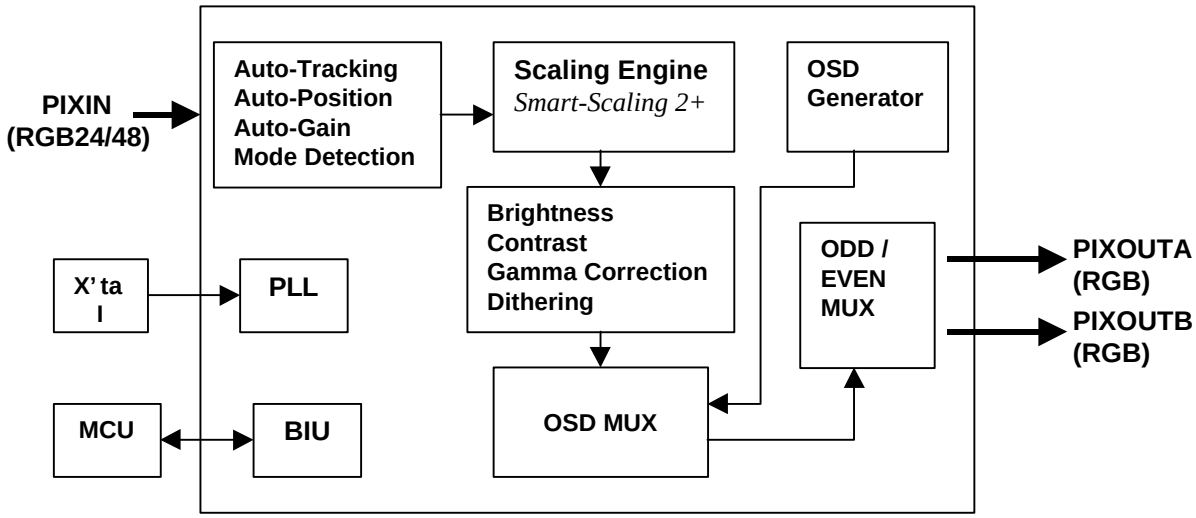
**CPU Interface**

- Support Direct Bus 8 bit interface (*MX88L250EC-D only)*
- Support Two/Three-Wire Serial Bus interface.
- Support Double Buffer Register capability.

**Power**

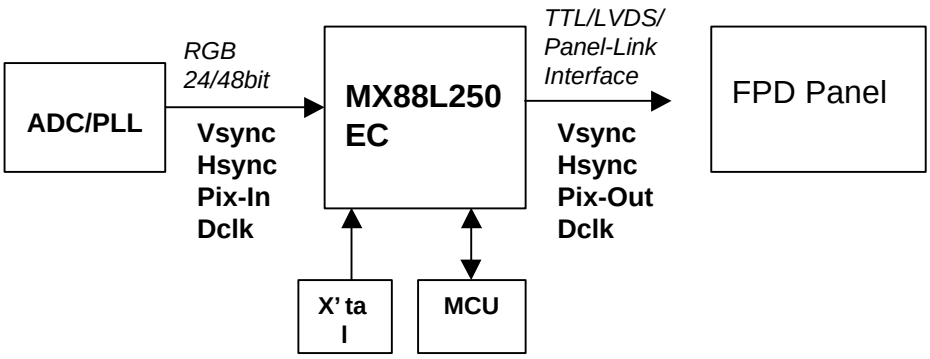
- Power Supplier: Dual Power 3.3/2.5 volts, 5V tolerant inputs.
- Power Consumption: less than 1W.

## Chip Block Diagram

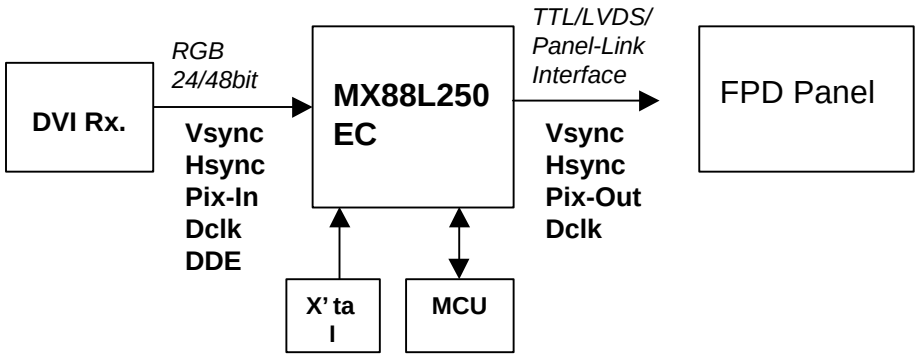


## System Block Diagram for LCD monitor ( TTL and PanelLink / LVDS Interfaced )

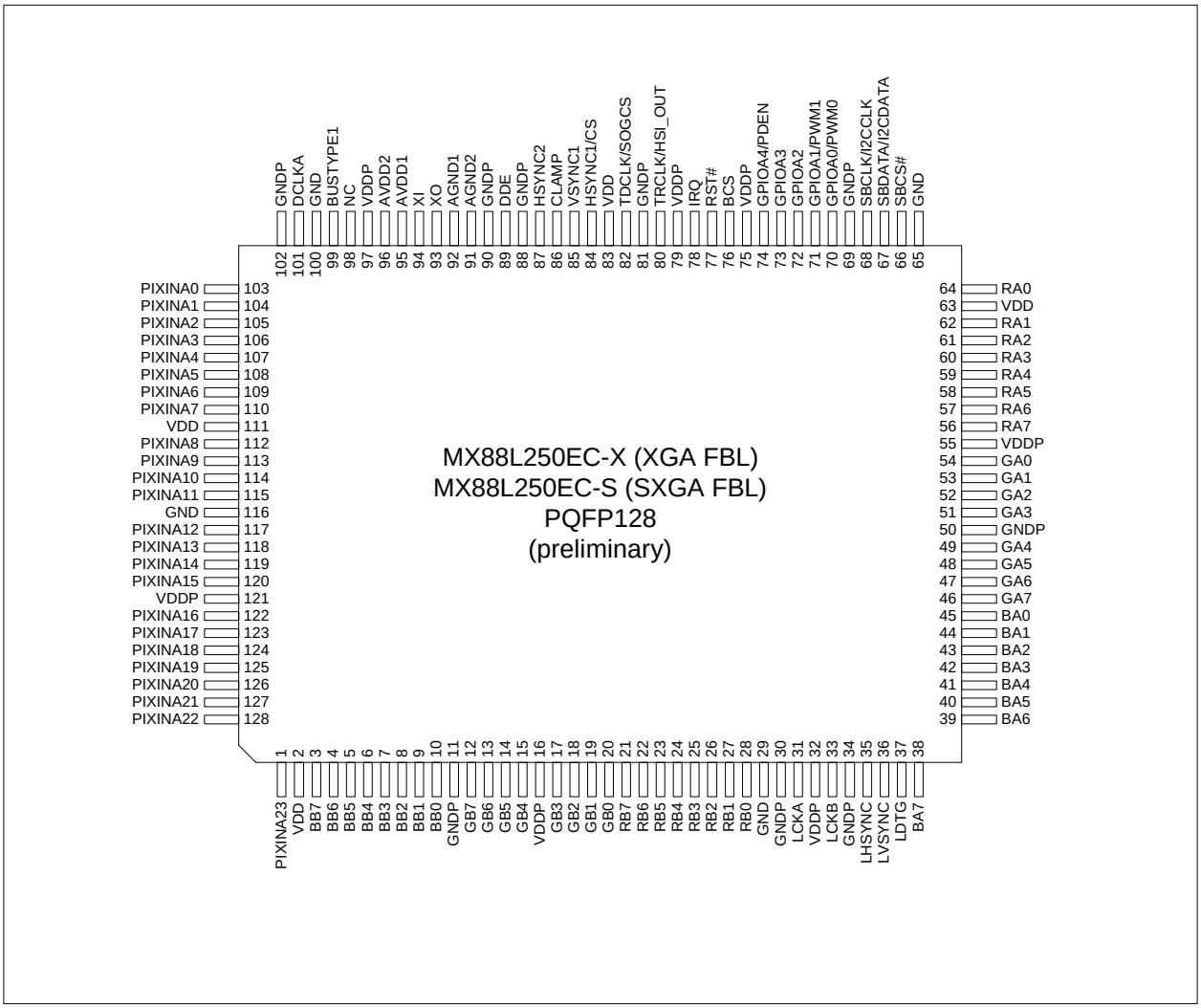
### Analog Interface LCD monitor



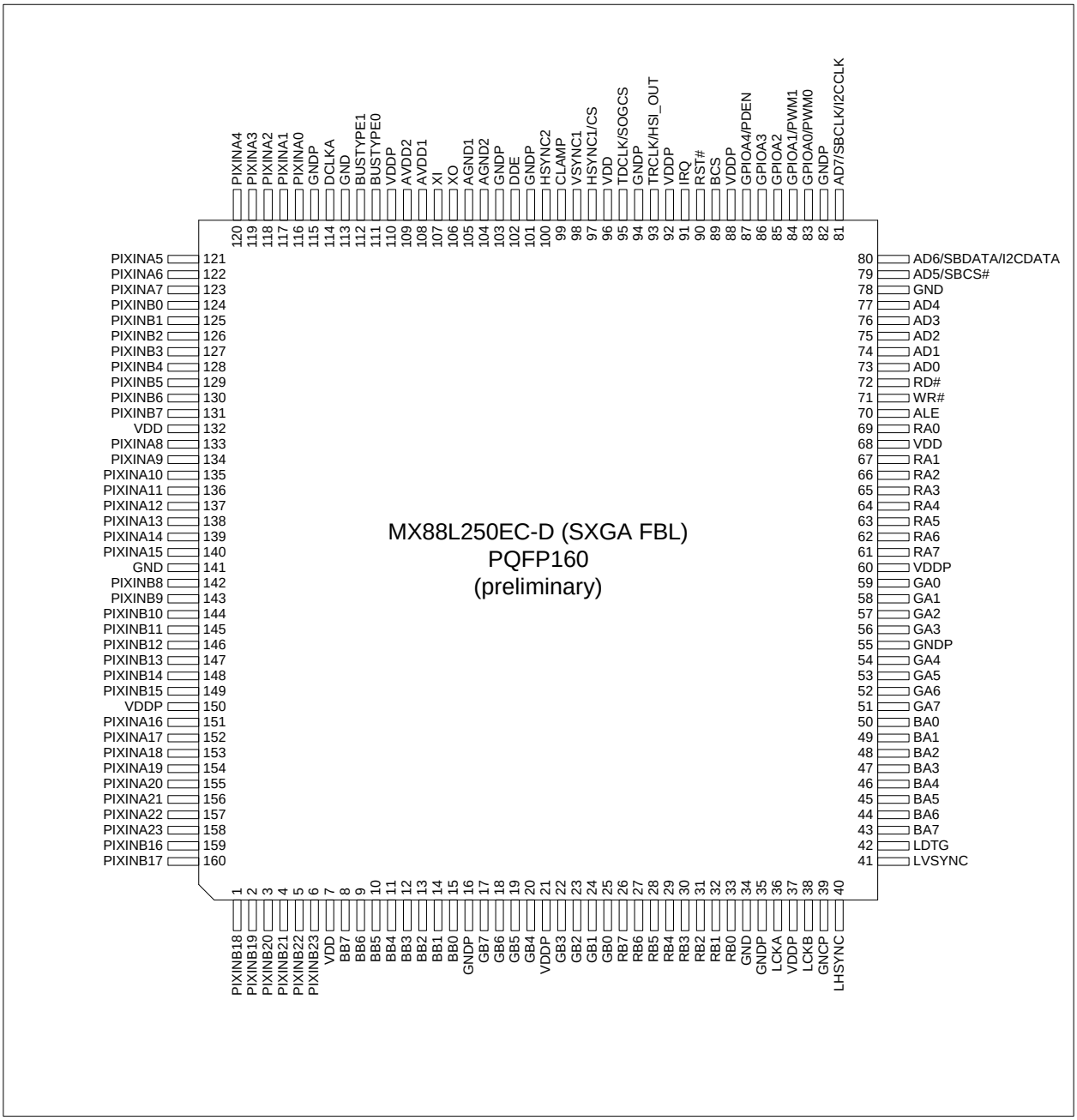

### Digital Interface LCD monitor



## MX88L250EC-X, MX88L250EC-S 128p Pin Configurations



## MX88L250EC-D 160p Pin Configurations



## General Description

There are three major portions in this chip which include VIP (Video Input Processor), VOP (Video Output Processor) and BIU (CPU Bus Interface Unit). Following is the block and description of these portions.

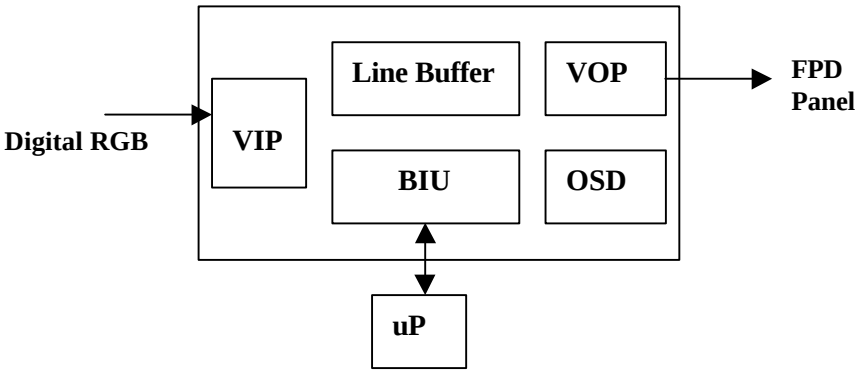



Fig. Chip Level Block Diagram

### VIP (Video Input Processor) Function Description

VIP is a video input process unit which receives digital data from ADC or digital input then process it to line buffer for VOP. It supports mode detection, auto-position, auto-gain, auto-tracking function for ADC modification.

### VOP (Video Output Processor) Function Description

VOP is a Video Output Process unit which reads data from line buffer and then process it to flat panel display.

With Line Buffers and Scale- up logic based on proprietary Smartscaling$^{TM}$ –$2^{+}$ algorithm, it can enlarge image smoothly. Furthermore, it provides many adjusting functions like programmable Brightness and Contrast control, programmable GAMMA table, programmable Dithering control, and OSD MUX to adjust the output quality. It also provides Single/Dual output to cope with different flat panels display device.

### BIU (Bus Interface Unit) Function Description

BIU is a bus interface unit between the host CPU and MX88L250 which supports two bus types: Direct and Serial Bus.

## Pin Description

**CPU Interface Pins: (8 / 16 pins)**

| Pin Name | Drive | I/O | Pin No. (L250EC-X) (L250EC-S) 128 pin | Pin No. (L250EC-D) 160 pin | DESCRIPTION |
|---|---|---|---|---|---|
| RST# | | I | 77 | 90 | System reset. |
| AD[7:0] | | IO | **X** | 81-79<br>77-73 | Multiplexed low order address and data bus |
| SBCLK / AD7 | | I | 68 | 81 | Two/Three-Wire Serial Bus Clock<br>*(share with AD7)* |
| SBDATA / AD6 | | IO | 67 | 80 | Two/Three-Wire Serial Bus Data<br>*(share with AD6)* |
| SBCS# / AD5 | | I | 66 | 79 | Three-Wire Serial Bus CS# (low active)<br>*(share with AD5)* |
| BCS | | I | 76 | 89 | Bus Select, Active high. |
| ALE | | I | **X** | 70 | Address Latch Enable for 8051 Bus. |
| WR# | | I | **X** | 71 | Memory Write Strobe for direct bus |
| RD# | | I | **X** | 72 | Memory Read Strobe for direct bus |
| BUSTYPE1 | | I | 99 | 112 | Bus type bit 1 |
| BUSTYPE0 | | I | 98 | 111 | Bus type bit 0 *(NC for MX88L250EC-S & -X)* |
| IRQ | | O | 78 | 91 | Interrupt request |

**Input Interface Pins: (29 / 53 pins)**

| Pin Name | Drive | I/O | Pin No. (L250EC-X) (L250EC-S) 128 pin | Pin No. (L250EC-D) 160 pin | DESCRIPTION |
|---|---|---|---|---|---|
| PIXINA 0-7 | | I | 103-110 | 116-123 | Input data R0-R7 |
| PIXINA 8-15 | | I | 112-115<br>117-120 | 133-140 | Input data G0-G7 |

| Pin Name | Drive | I/O | Pin No. (L250EC-X) (L250EC-S) 128 pin | Pin No. (L250EC-D) 160 pin | DESCRIPTION |
|---|---|---|---|---|---|
| PIXINA 16-23 | | I | 122-128<br>1 | 151-158 | Input data B0-B7 |
| PIXINB 0-7 | | I | **X** | 124-131 | Input data R0-R7 |
| PIXINB 8-15 | | I | **X** | 142-149 | Input data G0-G7 |
| PIXINB 16-23 | | I | **X** | 159-160<br>1-6 | Input data B0-B7 |
| HSYNC1/CS | | I | 84 | 97 | Hsync input1<br>*(for mode detection)* |
| HSYNC2 | | I | 87 | 100 | Hsync input2<br>*(for screen position & sampling use)* |
| VSYNC1 | | I | 85 | 98 | Vsync input |
| DDE | | I | 89 | 102 | Digital Data enable |
| DCLKA | | I | 101 | 114 | Input dot clock1 |

**LCD Interface Pins: (53 pins)**

| Pin Name | Drive | I/O | Pin No. (L250EC-X) (L250EC-S) 128 pin | Pin No. (L250EC-D) 160 pin | DESCRIPTION |
|---|---|---|---|---|---|
| RA[7:0] | 4 mA | O | 64<br>62-56 | 69<br>67-61 | RED DATA (Odd), |
| GA[7:0] | 4 mA | O | 54-51<br>49-46 | 59-56<br>54-51 | GREEN DATA (Odd), |
| BA[7:0] | 4 mA | O | 45-38 | 50-43 | BLUE DATA (Odd), |
| RB[7:0] | 4 mA | O | 28-21 | 33-26 | RED DATA (Even). |
| GB[7:0] | 4 mA | O | 20-17<br>15-12 | 25-22<br>20-17 | GREEN DATA (Even). |
| BB[7:0] | 4 mA | O | 10-3 | 15-8 | BLUE DATA (Even), |
| LVSYNC | 8 mA | O | 36 | 41 | VSYNC output for LCD display. |

| Pin Name | Drive | I/O | Pin No. (L250EC-X) (L250EC-S) 128 pin | Pin No. (L250EC-D) 160 pin | DESCRIPTION |
|---|---|---|---|---|---|
| LHSYNC | 8 mA | O | 35 | 40 | HSYNC output for LCD display. |
| LDTG | 8 mA | O | 37 | 42 | Data Enable output for LCD display. |
| LCKA | 16 mA | O | 31 | 36 | Odd data clock output for LCD display |
| LCKB | 16 mA | O | 33 | 38 | Even data clock output for LCD display. |

**Internal VCG Interface Pins: (2 pins)**

| Pin Name | Drive | I/O | Pin No. (L250EC-X) (L250EC-S) 128 pin | Pin No. (L250EC-D) 160 pin | DESCRIPTION |
|---|---|---|---|---|---|
| XI | | I | 94 | 107 | Analog pad for Reference Frequency Input for internal oscillator. (3.3 V) |
| XO | | O | 93 | 106 | Analog pad for Reference Frequency Output for internal oscillator. (3.3V) |

**Other Interface Pins: (6 pins)**

| Pin Name | Drive | I/O | Pin No. (L250EC-X) (L250EC-S) 128 pin | Pin No. (L250EC-D) 160 pin | DESCRIPTION |
|---|---|---|---|---|---|
| GPIOA0 / PWM0 | 2 mA | IO | 70 | 83 | Pulse width Modulation 0 Output, share with general IO 0 |
| GPIOA1 / PWM1 | 2 mA | IO | 71 | 84 | Pulse width Modulation 1 Output, share with general IO 1 |
| GPIOA2 | 2 mA | IO | 72 | 85 | General IO 2 |
| GPIOA3 | 2 mA | IO | 73 | 86 | General IO 3 |
| GPIOA4 / PDEN | 2 mA | IO | 74 | 87 | PDEN output for ADC Shared with general IO 4 |
| Clamp | | O | 86 | 99 | Clamp output for ADC |

**External Clock Input Interface Pins: (2 pin)**

| Pin Name | Drive | I/O | Pin No. (L250EC-X) (L250EC-S) 128 pin | Pin No. (L250EC-D) 160 pin | DESCRIPTION |
|---|---|---|---|---|---|
| TRCLK / HS1_OUT | | I O | 80 | 93 | External RCLK input (share with HS_OUT) |
| TDCLK / SOGCS | | I | 82 | 95 | External DCLK input. (share with SOGCS) |

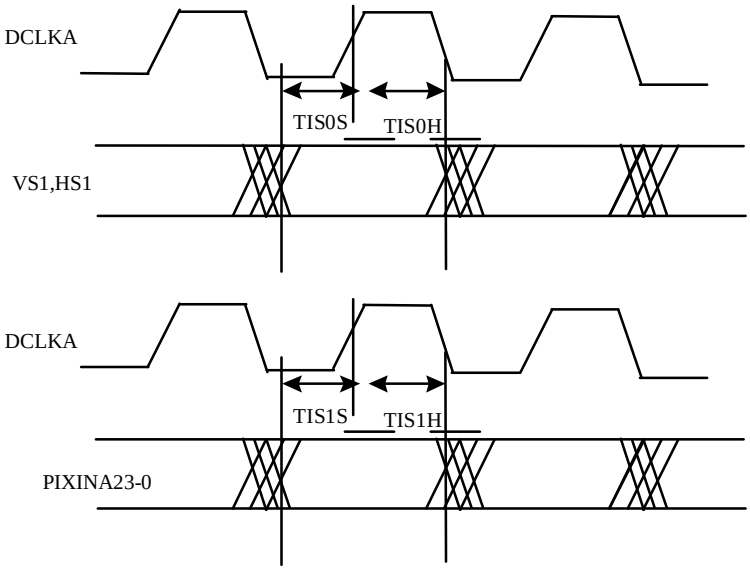
**Power Pins: (28 pins) dual power 3.3 / 2.5 Volts, 5 Volt tolerant inputs**

| Pin Name | Drive | I/O | Pin No. (L250EC-X) (L250EC-S) 128 pin | Pin No. (L250EC-D) 160 pin | DESCRIPTION |
|---|---|---|---|---|---|
| VDD | | | 2,63,83, 111, | 7,68,96, 132, | Core Power 2.5 V |
| GND | | | 29,65, 100,116 | 34,78,113, 141, | Core GND |
| VDDP | | | 16,32,55 ,75,79,9 7,121 | 21,37,60, 88,92,110, 150, | PAD Power 3.3 V |
| GNDP | | | 11,30,34 ,50,69,8 1,88,90, 102, | 16,35,39, 55,82,94, 101,103, 115, | PAD GND |
| AVDD1 / AVDD2 | | | 95,96 | 108,109 | Analog Power 2.5 V |
| AGND1 / AGND2 | | | 91,92 | 104,105 | Analog GND |

Remark:
1. All the input loading is 5pf
2. Driving capability is measured under 20pf loading
3. LCKA driving capability is measured under 30pf loading

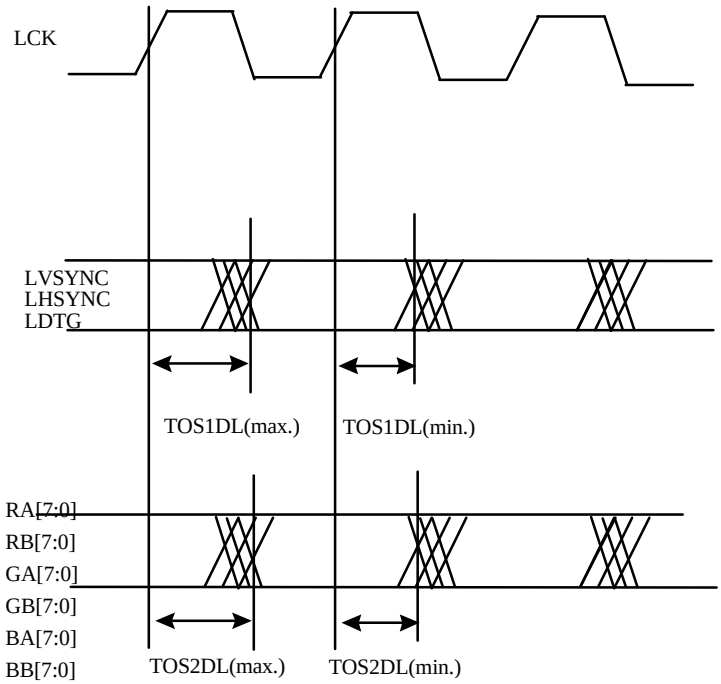
## AC Characteristics

### 1. Input signal



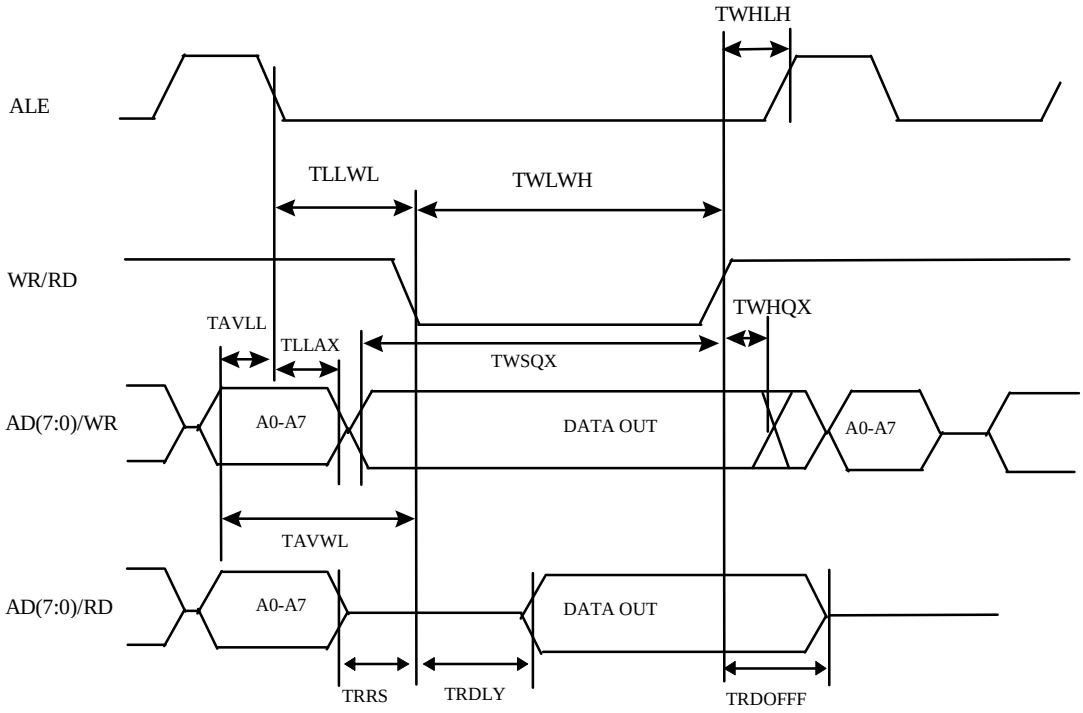

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| TIS0S, TIS0H | Setup time | 2 | | ns |
| TIS1S, TIS1H | Hold time | 2 | | ns |

## 2. Output signal




| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| TOS1DL | Output LHSYNC, LVSYNC, LDTG output delay | 1 | 5 | ns |
| TOS2DL | Output Pixel Signal output delay | 1 | 5 | ns |

### 3. Direct CPU Interface




| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| TAVLL | Address Valid to ALE Low | 2 | | ns |
| TLLAX | Address Hold After ALE Low | 1 | | ns |
| TWLWH | WR Pulse Width | 30 | | ns |
| TWSQX | Data Setup Before WR | 10 | | ns |
| TWHQX | Data Hold After WR | 0 | | ns |
| TWHLH | WR/RD High to ALE High | 0 | | ns |
| TRDLY | Data delay after RD Low | 10 | 35 | ns |
| TRDOFF | Data off delay after RD High | 0 | 7 | ns |

### 4. Serial Bus Interface

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| Tcsck | CS to CLK Start | 0 | | ns |
| Tckcs | CLK to CS high | 20 | | ns |
| Tds | Data setup time versus CLK | 10.1 | | ns |
| Tdh | Data hold time versus CLK | 20 | | ns |
| Tdd | Data delay time | 14 | 18 | ns |

### 5. External Clock Input Interface

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| Fclk | Maximum TDCLK input frequency | | 80 | MHz |
| Fpw | Minimum pulse width | 3 | | ns |

## DC characteristics

### 1. Environmental specification:

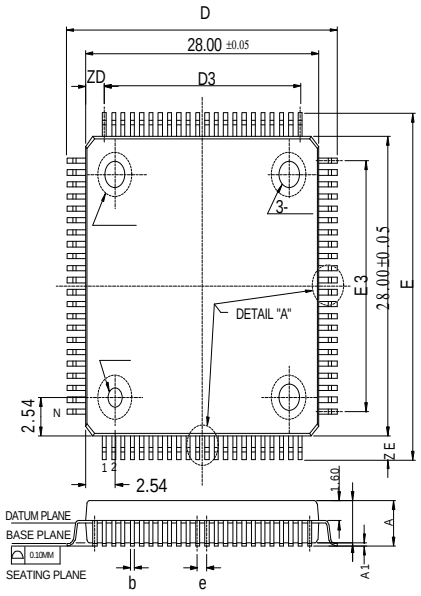
| Rating | Value | Unit |
|---|---|---|
| Ambient Operating Temperature | 0 to 70 | °C |
| Storage Temperature | -55 to 125 | °C |
| Maximum Junction Temperature | 125 | °C |
| Maximum Case Temperature | 100 | °C |

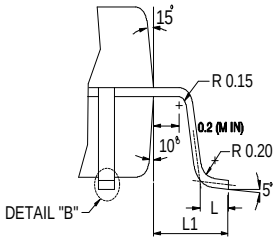
### 2. Standard DC Specification for 3.3 Volts Operation:

(Ta=0°C to 70°C, VCC=3V to 3.6V)

| Symbol | Parameter | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|
| VOH | Output High Voltage | 2.4 | | V | |
| VOL | Output Low Voltage | | 0.4 | V | |
| VIH | Input High Voltage | 2.0 | | V | |
| VIL | Input Low Voltage | | 0.8 | V | |
| RPU | I/O Pull-up Resistance | 100 | 300 | KOhm | |
| RPD | I/O Pull-down Resistance | 50 | 150 | KOhm | |
| ILI | Input Leakage Current | -10 | +10 | *u* A | |
| ILO | Output Leakage Current | -20 | +20 | *u* A | |

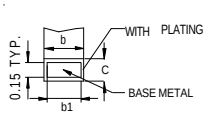
## Dimension



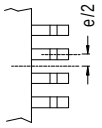




TERMINAL DETAILS

| DETAIL "A" | 144F2828-A | 160F2828-A | 208F2828-A | 256F2828-A |
|---|---|---|---|---|
| b | 0.32 | 0.32 | 0.22 | 0.18 |
| C | 0.10 | 0.10 | 0.10 | 0.10 |
| b1 | 0.30 | 0.30 | 0.20 | 0.16 |
| e | 0.65 | 0.65 | 0.50 | 0.40 |
| L1 | 1.60 | 1.60 | 1.30 | 1.30 |
| L | 0.80 | 0.80 | 0.50 | 0.50 |
| ZE (REF.) | 1.33 | 1.33 | 1.25 | 1.25 |
| E3 (REF.) | 25.35 | 25.35 | 25.50 | 25.50 |
| E | 31.2 | 31.2 | 30.6 | 30.6 |
| ZD (REF.) | 2.63 | 1.33 | 1.25 | 1.40 |
| D3 (REF.) | 25.35 | 25.35 | 25.50 | 25.20 |
| D | 31.2 | 31.2 | 30.6 | 30.6 |
| A1 | 0.35 | 0.35 | 0.35 | 0.35 |
| A (MAX.) | 3.80 | 3.80 | 3.80 | 3.80 |
| N | 144L | 160L | 208L | 256L |
| JEDEC | MO-108 DC-1 | MO-108 DD-1 | MO-143 FA-1 | MO-143 FB1 |




DETAIL "B"




DETAIL "A"

| | | | | DWG. NO. |
|---|---|---|---|---|
| Macronix International Co., Ltd. | | | | 6110-0212 |
| TITLE OUTLINE DIMENSIONS FOR QFP2828 MM PACKAGE | | | | TOLERANCE / ANGLE ° |
| DRAWN | APPROVED | SCALE | UNIT | REVISION |
| CH Lin | JW Lin | | mm | 2 |

# MX88L250EC

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