HD49351BP/HBP

CDS/PGA & 10-bit A/D TG Converter

REJ03F0110-0100Z
Rev.1.0
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Description

The HD49351BP/HBP is a CMOS IC that provides CDS-PGA analog processing (CDS/PGA) suitable for CCD camera digital signal processing systems together with a 10-bit A/D converter and timing generator in a single chip. HD49351 has deleted the stripe mode, pd_mix mode, and added the 5 – 6 pulse and H_msk2 - 4 as contrasted with HD49335.

There are address map and timing generator charts besides this specification. May be contacted to our sales department if examining the details.

Functions

- Correlated double sampling
- PGA
- 10-bit ADC
- Timing generator
- Operates using only the 3 V voltage
- Corresponds to switching mode of power consumption and operating frequency
  220 mW (Typ), maximum frequency: 36 MHz (HD49351HBP)
  150 mW (Typ), maximum frequency: 25 MHz (HD49351BP)
- ADC direct input mode
- FBGA 65-pin package

Features

- Suppresses low-frequency noise, which output from CCD by the correlated double sampling.
- The S/H response frequency characteristics for the reference level can be adjusted using values of external parts and registers.
- High sensitivity is achieved due to the high S/N ratio and a wide dynamic range provided by a PG amplifier.
- PGA, pulse timing, standby mode, etc., is achieved via a serial interface.
- High precision is provided by a 10-bit-resolution A/D converter.
- Difference encoded gray code can be selected as an A/D output code. It is effective in suppression of solarization (wave pattern). It is patented by Renesas.
- Timing generator generates the all of pulse which are needed for CCD driving.

Pin Arrangement

	10	9	8	7	6	5	4	3	2	1
A	32 XV3	31 XV2	30 XV1	29 DVdd3	26 H2	24 DVss4	22 H1	19 RG	17 VD_i/o	16 HD_i/o
B	33 XV4	34 CH1	28 DVdd4	27 1/4clk	25 DVss4	23 1/2clk	21 DVdd4	20 DVdd3	18 Reset	15 CLK_in
C	35 CH2	36 CH3						14 DVss3	14 DVss3	13 DVdd2
D	38 XSUB	37 CH4							12 D9	11 D8
E	40 SUB_PD	39 SUB_SW							10 D7	8 D5
F	42 DVss3	41 Strob							9 D6	6 D3
G	45 Bias	43 AVss							7 D4	4 D1
H	46 VRB	44 ADC_in							5 D2	3 D0
J	48 VRM	49 AVdd	52 AVdd	55 AVss	56 test2	57 test1	59 DVdd1	61 41cont	62 CDS_CS	2 DVss1,2
K	47 VRT	50 BLKC	51 CDS_in	53 BLKFB	54 BLKSH	58 DLLC	60 MON	63 Sdata	64 SCK	1 ID

(Top view)

Notes: 1. Pin 41 outputs the STROB, pin 39 outputs the SUB_SW when pin 61 is Low.
2. Pin 41 inputs the Vgate, pin 39 inputs the ADCK when pin 61 is High.
3. 1/2 and 4clk output terminal becomes 1/3 and 1/6clk output respectively, when operating TG in 3 divided mode.

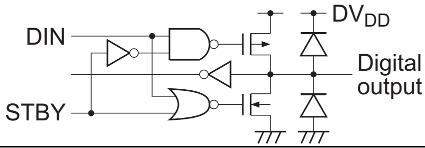
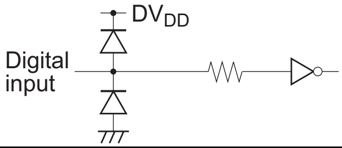
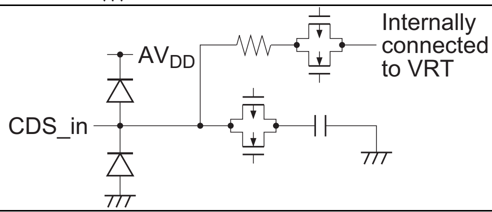
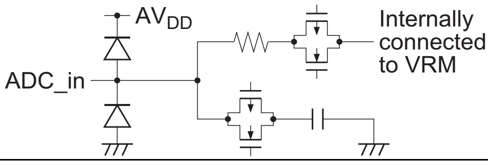
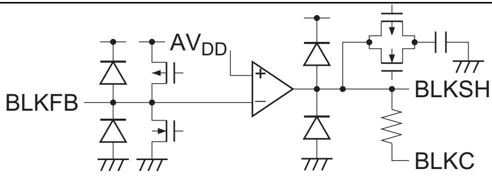
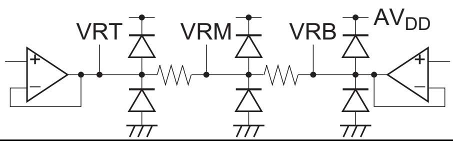
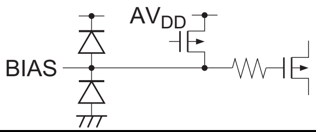
Pin Description

BGA Pin No.	PAD No.	Symbol	Description	I/O	Analog(A) or Digital(D)	Remarks
K1	1	ID	Odd/even number line detecting pulse output pin	O	D	2 mA/10 pF
J1	2	DVss1, 2	CDS Digital ground + ADC output buffer ground (0V)	—	D	
H1 to D2	3 to 12	D0 to D9	Digital output (D0; LSB, D9; MSB)	O	D	2 mA/10 pF
C1	13	DVdd2	ADC output buffer power supply (3 V)	—	D	
C2, C3	14	Dvss3	General ground for TG (0V)	—	D	
B1	15	CLK_in	CLK input (max 72 MHz)	I	D	
A1	16	HD_in	HD input	I	D	
A2	17	VD_in	VD input	I	D	
B2	18	Reset	Hardware reset (for DLL reset)	I	D	Schmitt trigger
A3	19	RG	Reset gate pulse output	O	D	3 mA/10 pF
B3	20	DVdd3	General power supply for TG (3V)	—	D	
B4	21	DVdd4	H1,2 buffer power supply (3 V)	—	D	
A4	22	H1	H.CCD transfer pulse output-1	O	D	30 mA/165 pF
B5	23	1/2clk_o	CLK_in 2 divided output. 3 divided output at 3 divided mode	O	D	2 mA/10 pF
A5	24	Dvss4	H1,2 buffer ground (0 V)	—	D	
B6	25	Dvss4	H1,2 buffer ground (0 V)	—	D	
A6	26	H2	H.CCD transfer pulse output-2	O	D	30 mA/165 pF
B7	27	1/4clk_o	CLK_in 4 divided output. 6 divided output at 3 divided mode	O	D	2 mA/10 pF
B8	28	DVdd4	H1,2 buffer power supply (3 V)	—	D	
A7	29	DVdd3	General power supply for TG (3 V)	—	D	

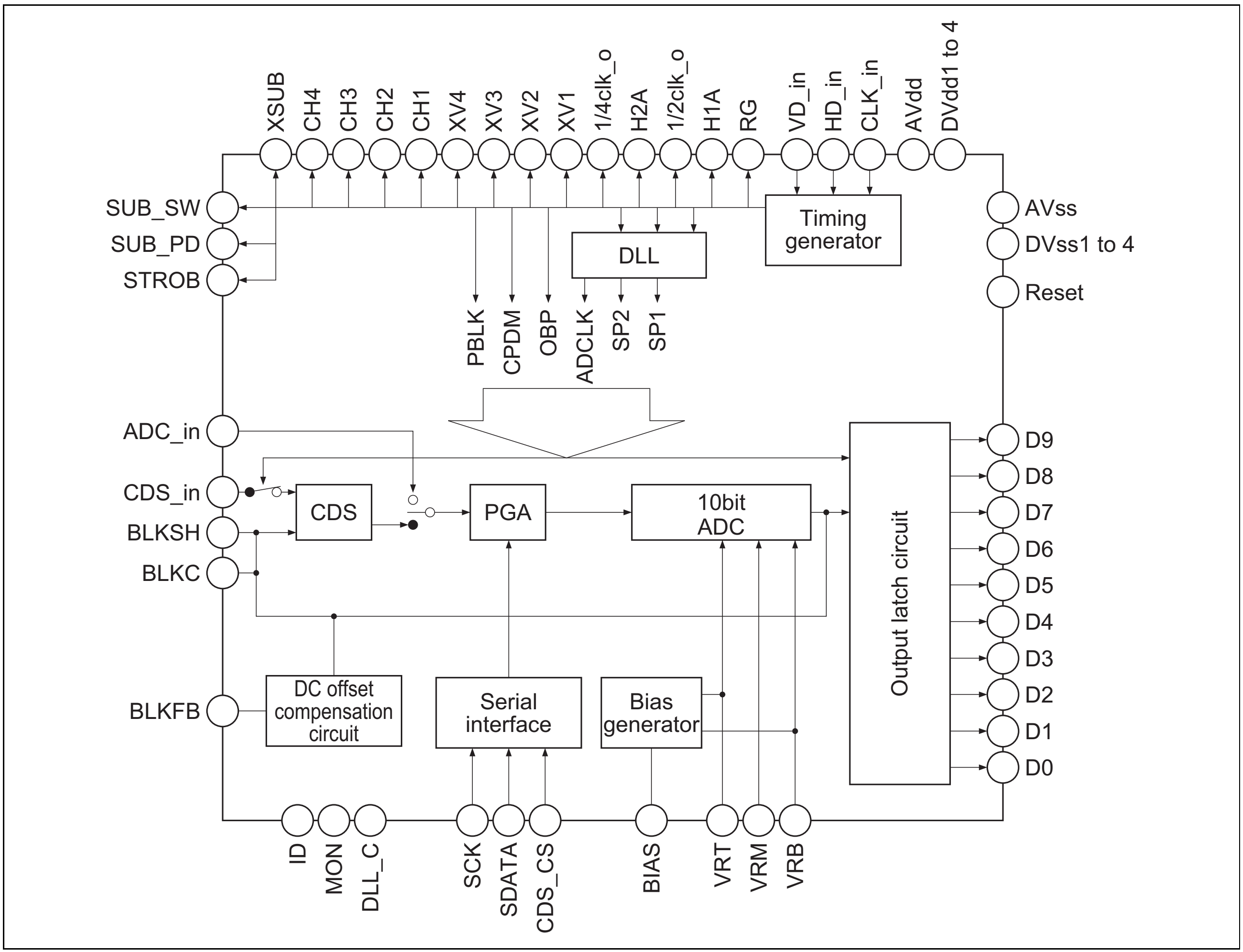
Pin Description (cont.)

BGA Pin No.	PAD No.	Symbol	Description	I/O	Analog(A) or Digital(D)	Remarks
A8	30	XV1	V.CCD transfer pulse output-1	O	D	2 mA/10 pF
A9	31	XV2	V.CCD transfer pulse output-2	O	D	2 mA/10 pF
A10	32	XV3	V.CCD transfer pulse output-3	O	D	2 mA/10 pF
B10	33	XV4	V.CCD transfer pulse output-4	O	D	2 mA/10 pF
B9	34	CH1	Read out pulse output-1	O	D	2 mA/10 pF
C10	35	CH2	Read out pulse output-2	O	D	2 mA/10 pF
C9	36	CH3	Read out pulse output-3	O	D	2 mA/10 pF
D9	37	CH4	Read out pulse output-4	O	D	2 mA/10 pF
D10	38	XSUB	Pulse output for electronic shutter	O	D	2 mA/10 pF
E9	39	SUB_SW	SUB voltage control output-1. Input the ADCK when 61 pin is Hi	I/O	D	2 mA/10 pF
E10	40	SUB_PD	SUB voltage control output-2	O	D	2 mA/10 pF
F9	41	STROB	Flash control output. Input Vgate at Hi of 61pin	I/O	D	2 mA/10 pF
F10	42	DVss3	General ground for TG (0 V)	—	D	
G9	43	AVss	Analog ground (0 V)	—	A	
H9	44	ADC_in	A/D converter input pin	I	A	
G10	45	BIAS	Bias standard resistance (33 kΩ for Gnd)	—	A	
H10	46	VRB	ADC bottom standard voltage (0.1 µF for Gnd)	—	A	
K10	47	VRT	ADC top standard voltage (0.1 µF for Gnd)	—	A	
J10	48	VRM	ADC middle standard voltage (0.1 µF for Gnd)	—	A	
J9	49	Avdd	Analog power supply (3 V)	—	A	
K9	50	BLK_C	Black level C pin (1000pF for Gnd)	—	A	
K8	51	CDS_in	CDS input pin	I	A	
J8	52	AVdd	Analog power supply (3 V)	—	A	
K7	53	BLKFB	Black level FB pin (1 µF between BLKFB and BLKSH)	I	A	
K6	54	BLKSH	Black level S/H pin	O	A	
J7	55	AVss	Analog ground (0 V)	—	A	
J6	56	Test2	H: Normal operation, L: CDS single operation mode Input 36; PBLK at testing, Input 37; OBP, Input 38; CPDM, Input 39; ADCLK, Input 40; SP2, Input 41; SP1	I	D	
J5	57	Test1	L: Slave mode, H: Master mode	I	D	
K5	58	DLL_C	Analog delay DLL external C pin (100 pF for Gnd)	O	A	
J4	59	Dvdd1	Digital power supply (3 V) CDS, PAG, ADC part	—	D	
K4	60	MON	Pulse monitor (SP1, SP2, ADCLK, OBP, CPDM, PBLK output)	O	D	2 mA/10 pF
J3	61	41cont	Input STROB = pin 41, Input SUB_SW = pin 39 at Low Input Vgate = pin 41, Input ADCK = pin 39 at Hi	I	D	
J2	62	CDS_CS	Serial data CS at CDS part	I	D	
K3	63	SDATA	Input serial data	I	D	
K2	64	SCK	Input serial clock	I	D	

Input/Output Equivalent Circuit

Pin Name		Equivalent Circuit
Digital output	D0 to D9, RG, H1A to H2B, XV1 to XV4, CH1 to CH4, XSUB, SUB_SW, SUB_PD, STROB, MON	
Digital input	ADCLK, OBP, CPDM, SP1,2, PBLK, CS, SCK, SDATA, CLK_in, HD_in, VD_in	
Analog	CDS_in	
	ADC_in	
	BLKSH, BLKFB, BLKC	
	VRT, VRM, VRB	
	BIAS	

Block Diagram



Internal Functions

Functional Description

- CDS input
  - — CCD low-frequency noise is suppressed by CDS (correlated double sampling).
  - — The signal level is clamped at 14 LSB to 76 LSB (set by resister: 5 bit 2 LSB step controls) during the OB period. *[1]
  - — Gain can be adjusted using 8 bits of register (0.132 dB steps) within the range from –2.36 dB to 31.40 dB. *[2]
- ADC input
  - — The center level of the input signal is clamped at 512 LSB (Typ).
  - — Gain can be adjusted using 8 bits of register (0.01784 times steps, register settings) within the range from 0.57 times (–4.86 dB) to 5.14 times (14.22 dB). *[2]
- Automatic offset calibration of PGA and ADC
- DC offset compensation feedback for CCD and CDS
- Pre-blanking
  - — Digital output is fixed at clamp level
- Digital outputs enable function

Note: 1. It is not covered by warranty when 14 LSB settings
2. Full-scale digital output is defined as 0 dB (one time) when 1 V is input.

Operating Description

Figure 1 shows CDS/PGA + ADC function block.

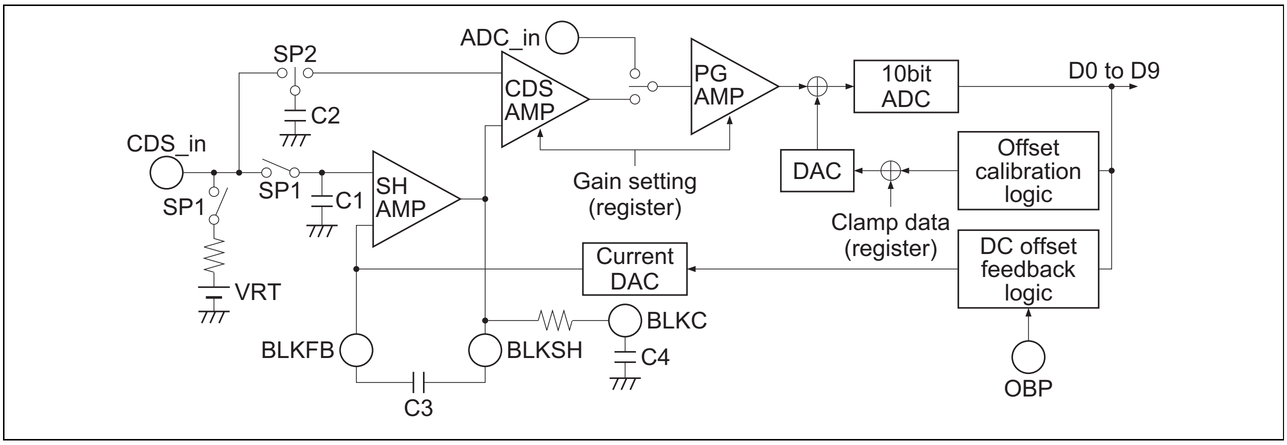


Figure 1 CDS/PGA Functional Block Diagram

1. CDS (Correlated Double Sampling) Circuit
   The CDS circuit extracts the voltage differential between the black level and a signal including the black level. The black level is directly sampled at C1 by using the SP1 pulse, buffered by the SHAMP, then provided to the CDSAMP.
   The signal level is directly sampled at C2 by using the SP2 pulse, and then provided to CDSAMP (see figure 1). The difference between these two signal levels is extracted by the CDSAMP, which also operates as a programmable gain amplifier at the previous stage. The CDS input is biased with VRT (2 V). During the PBLK period, the above sampling and bias operation are paused.
2. PGA Circuit
   The PGAMP is the programmable gain amplifier for the latter stage. The PGAMP and the CDSAMP set the gain using 8 bits of register.
   The equation below shows how the gain changes when register value N is from 0 to 255.
   In CDSIN mode: Gain = (–2.36 dB + 0.132 dB) × N (LOG linear).
   In ADCIN mode: Gain = (0.57 times + 0.001784 times) × N (linear).
   Full-scale digital output is defined as 0 dB (one time) when 1 V is input.

3. Automatic Offset Calibration Function and Black-Level Clamp Data Settings
   The DAC DC voltage added to the output of the PGA amplifier is adjusted by automatic offset calibration.
   The data, which cancels the output offset of the PGA amplifier and the input offset of the ADC, and the clamp data (14 LSB to 76 LSB) set by register are added and input to the DAC.
   The automatic offset calibration starts automatically after the RESET mode set by register is cancelled and terminates after 40,000 clock cycles (when fclk = 40.0 MHz, 1.0 ms, fclk = 20.0 MHz, 2.0 ms).
4. DC Offset Compensation Feedback Function
   Feedback is done to set the black signal level input during the OB period to the DC standard, and all offsets (including the CCD offset and the CDSAMP offset) are compensated for.
   The offset from the ADC output is calculated during the OB period, and SHAMP feedback capacitor C3 is charged by the current DAC (see figure 1).
   The open-loop differential gain (ΔGain/ΔH) per 1 H of the feedback loop is given by the following equation. 1H is the one cycle of the OBP.

   $\Delta Gain/\Delta H = 0.078/(fclk \times C3)$ (fclk: ADCLK frequency, C3: SHAMP external feedback capacitor)

   Example: When fclk = 20 MHz and C3 = 1.0 μF, ΔGain/ΔH = 0.0039

   DC offset compensation per 1 H (LSB) = 0.0039 × Offset error (LSB) [Note)]

   Note: There is a maximum value in the above-mentioned amount of offset errors.

   When the PGAMP gain setting is changed, the high-speed lead-in operation state is entered, and the feedback loop gain is increased by a multiple of N. Loop gain multiplication factor N can be selected from 4 times, 8 times, 16 times, or 32 times by changing the register settings (see table 1). Note that the open-loop differential gain (ΔGain/ΔH) must be one or lower. If it is two or more, oscillation occurs.
   The time from the termination of high-speed lead-in operation to the return of normal loop gain operation can be selected from 1 H, 2 H, 4 H, or 8 H. If the offset error is over 16 LSB, the high-speed lead-in operation continues, and when the offset error is 16 LSB or less, the operation returns to the normal loop-gain operation after 1 H, 2 H, 4 H, or 8 H depending on the register settings. (Refer to table 2.)

Table 1 Loop Gain Multiplication Factor during High-Speed Lead-In Operation

HGain-Nsel (register settings)		Multiplication Factor N
[0]	[1]	
L	L	× 4
H	L	× 8
L	H	× 16
H	H	× 32

Table 2 High-Speed Lead-In Operation Cancellation Time

HGstop-Hsel (register settings)		Cancellation Time
[0]	[1]	
L	L	1 H
H	L	2 H
L	H	4 H
H	H	8 H

5. Pre-Blanking Function
   During the PBLK input period, the CDS input operation is separated and protected from the large input signal. The ADC digital output is fixed to clamp data (14 to 76 LSB).

6. ADC Digital Output Control Function
   The ADC digital output includes the functions output enable, code conversion, and test mode. Tables 3, 4 and 5 show the output functions and the codes.

Table 3 ADC Digital Output Functions

STBY	TEST0	TEST1	LINV	MINV	PBLK	ADC Digital Output										Operating Mode
						D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
H	X	X	X	X	X	Hi-Z										Low-power wait state
L	X	X	X	X	X	Hi-Z										Output Hi-Z
	L	L	L	L	L	Same as in table 4.										Normal operation
			L	H	L	D9 is inverted in table 4.										
			H	L	L	D8 to D0 are inverted in table 4.										
			H	H	L	D9 to D0 are inverted in table 4.										
			X	X	H	Output code is set up to Clamp Level.										Pre-blanking
		H	L	L	L	Same as in table 5.										Normal operation
			L	H	L	D9 is inverted in table 5.										
			H	L	L	D8 to D0 are inverted in table 5.										
			H	H	L	D9 to D0 are inverted in table 5.										
			X	X	H	Output code is set up to Clamp Level.										Pre-blanking
	H	X	L	L	X	H	L	H	L	H	L	H	L	H	L	Test mode
			L	H	X	L	L	H	L	H	L	H	L	H	L	
			H	L	X	H	H	L	H	L	H	L	H	L	H	
			H	H	X	L	H	L	H	L	H	L	H	L	H	

Note: 1. STBY, TEST, LINV, and MINV are set by register.

Table 4 ADC Output Code (Binary)

Output Pin				D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Output codes	Steps	0		L	L	L	L	L	L	L	L	L	L
		1		L	L	L	L	L	L	L	L	L	H
		2		L	L	L	L	L	L	L	L	H	L
		3		L	L	L	L	L	L	L	L	H	H
		4		L	L	L	L	L	L	L	H	L	L
		5		L	L	L	L	L	L	L	H	L	H
		6		L	L	L	L	L	L	L	H	H	L
		⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
		511		L	H	H	H	H	H	H	H	H	H
		512		H	L	L	L	L	L	L	L	L	L
		⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
		1020		H	H	H	H	H	H	H	H	L	L
		1021		H	H	H	H	H	H	H	H	L	H
		1022		H	H	H	H	H	H	H	H	H	L
		1023		H	H	H	H	H	H	H	H	H	H

Table 5 ADC Output Code (Gray)

Output Pin				D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Output codes	Steps	0		L	L	L	L	L	L	L	L	L	L
		1		L	L	L	L	L	L	L	L	L	H
		2		L	L	L	L	L	L	L	L	H	H
		3		L	L	L	L	L	L	L	L	H	L
		4		L	L	L	L	L	L	L	H	H	L
		5		L	L	L	L	L	L	L	H	H	H
		6		L	L	L	L	L	L	L	H	L	H
		⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
		511		L	H	L	L	L	L	L	L	L	L
		512		H	H	L	L	L	L	L	L	L	L
		⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
		1020		H	L	L	L	L	L	L	L	H	L
		1021		H	L	L	L	L	L	L	L	H	H
		1022		H	L	L	L	L	L	L	L	L	H
		1023		H	L	L	L	L	L	L	L	L	L

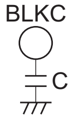
7. Adjustment of Black-Level S/H Response Frequency Characteristics
   The CR time constant that is used for sampling/hold (S/H) at the black level can be adjusted by changing the register settings, as shown in table 6.

Table 6 SHSW CR Time Constant Setting

<table>
<tr><td></td><td colspan="32">SHSW-fsel (Register setting)</td></tr>
<tr><td></td><td>[0]</td><td>[1]</td><td>[2]</td><td>[3]</td><td>[0]</td><td>[1]</td><td>[2]</td><td>[3]</td><td>[0]</td><td>[1]</td><td>[2]</td><td>[3]</td><td>[0]</td><td>[1]</td><td>[2]</td><td>[3]</td><td>[0]</td><td>[1]</td><td>[2]</td><td>[3]</td><td>[0]</td><td>[1]</td><td>[2]</td><td>[3]</td><td>[0]</td><td>[1]</td><td>[2]</td><td>[3]</td><td>[0]</td><td>[1]</td><td>[2]</td><td>[3]</td></tr>
<tr><td></td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>L</td><td>L</td><td>H</td><td>H</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>L</td><td>H</td><td>H</td><td>L</td><td>H</td><td>H</td><td>H</td><td>L</td></tr>
<tr><td>CR Time Constant (Typ)
(cutoff frequency conversion)</td><td colspan="4">2.20 nsec
(72 MHz)</td><td colspan="4">2.30 nsec
(69 MHz)</td><td colspan="4">2.51 nsec
(63 MHz)</td><td colspan="4">2.64 nsec
(60 MHz)</td><td colspan="4">2.93 nsec
(54 MHz)</td><td colspan="4">3.11 nsec
(51 MHz)</td><td colspan="4">3.52 nsec
(45 MHz)</td><td colspan="4">3.77 nsec
(42 MHz)</td></tr>
</table>

<table>
<tr><td></td><td colspan="32">SHSW-fsel (Register setting)</td></tr>
<tr><td></td><td>[0]</td><td>[1]</td><td>[2]</td><td>[3]</td><td>[0]</td><td>[1]</td><td>[2]</td><td>[3]</td><td>[0]</td><td>[1]</td><td>[2]</td><td>[3]</td><td>[0]</td><td>[1]</td><td>[2]</td><td>[3]</td><td>[0]</td><td>[1]</td><td>[2]</td><td>[3]</td><td>[0]</td><td>[1]</td><td>[2]</td><td>[3]</td><td>[0]</td><td>[1]</td><td>[2]</td><td>[3]</td><td>[0]</td><td>[1]</td><td>[2]</td><td>[3]</td></tr>
<tr><td></td><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td><td>L</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>H</td><td>H</td><td>L</td><td>H</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>L</td><td>H</td><td>H</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td></tr>
<tr><td>CR Time Constant (Typ)
(cutoff frequency conversion)</td><td colspan="4">4.40 nsec
(36 MHz)</td><td colspan="4">4.80 nsec
(33 MHz)</td><td colspan="4">5.87 nsec
(27 MHz)</td><td colspan="4">6.60 nsec
(24 MHz)</td><td colspan="4">8.80 nsec
(18 MHz)</td><td colspan="4">10.6 nsec
(15 MHz)</td><td colspan="4">17.6 nsec
(9 MHz)</td><td colspan="4">26.4 nsec
(6 MHz)</td></tr>
</table>

8. The SHAMP frequency characteristics can be adjusted by changing the register settings and the C4 value of the external pin.
   The settings are shown in table 7.
   Values other than those shown in the table 7 cannot be used.



Recommendation value of C is 1000 pF

Table 7 SHAMP Frequency Characteristics Setting

<table>
<tr><td rowspan="3">LoPwr
(Register setting)</td><td colspan="8">SHA-fsel (Register setting)</td></tr>
<tr><td>[0]</td><td>[1]</td><td>[0]</td><td>[1]</td><td>[0]</td><td>[1]</td><td>[0]</td><td>[1]</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td></tr>
<tr><td>"Lo"</td><td colspan="2">230 MHz
6800 pF
(240 pF)</td><td colspan="2">116 MHz
10000 pF
(270 pF)</td><td colspan="2">75 MHz
13000 pF
(300 pF)</td><td colspan="2">56 MHz
18000 pF
(360 pF)</td></tr>
<tr><td>"Hi"</td><td colspan="2">100 MHz
10000 pF
(560 pF)</td><td colspan="2">49 MHz
15000 pF
(620 pF)</td><td colspan="2">32 MHz
22000 pF
(750 pF)</td><td colspan="2">24 MHz
27000 pF
(820 pF)</td></tr>
</table>

Note: Upper line : SHAMP cutoff frequency (Typ)
Middle line : Standard value of C4 (maximum value is not defined)
Lower line : Minimum value of C4 (do not set below this value)

Timing Chart

Figure 2 shows the timing chart when CDS_in and ADC_in input modes are used.

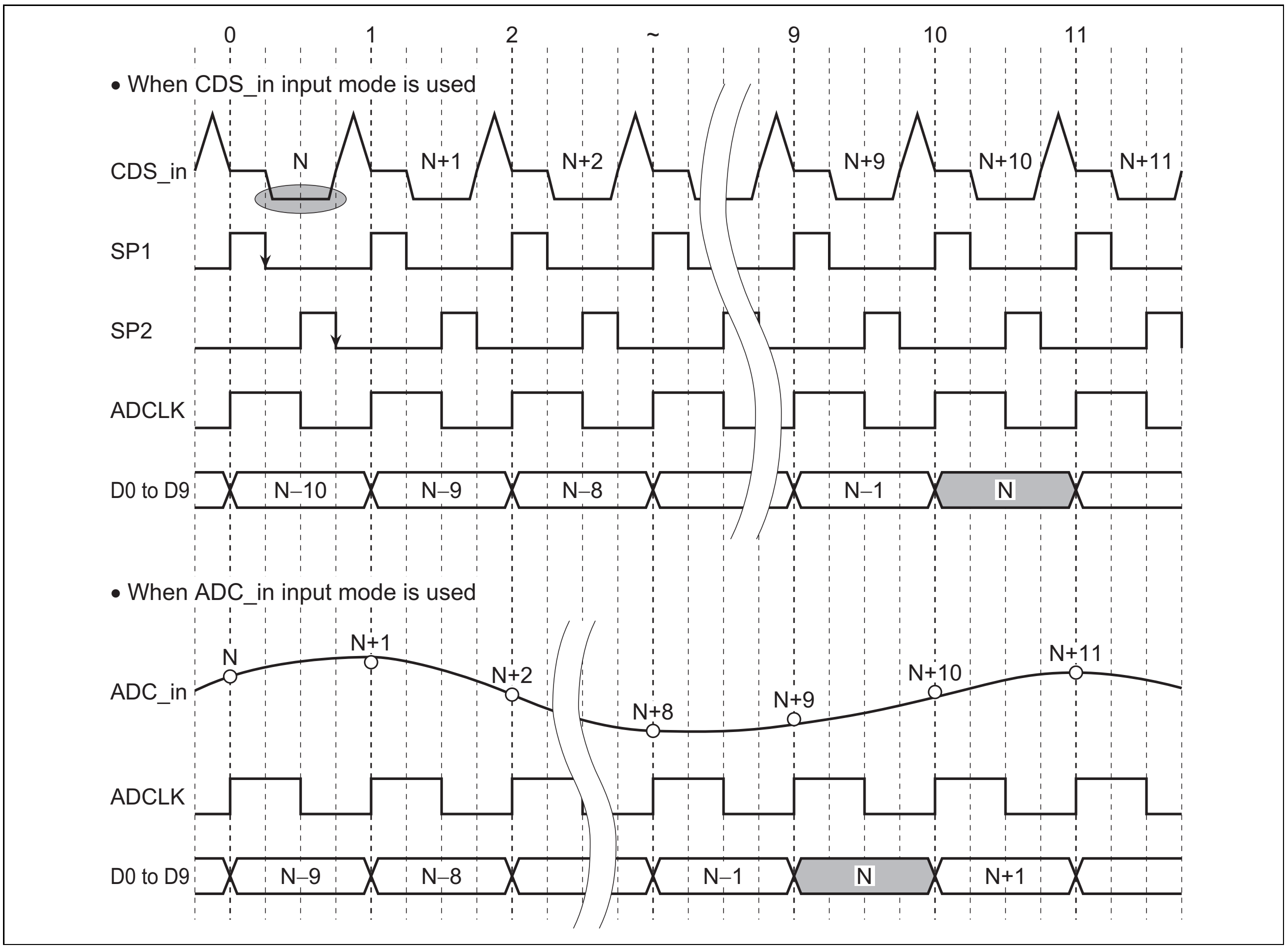


Figure 2 Output Timing Chart when CDS_in and ADC_in Input Modes are Used

- The ADC output (D0 to D9) is output at the rising edge of the ADCLK in both modes.
- Pipe-line delay is ten clock cycles when CDS_in is used and nine when ADC_in is used.
- In ADC_in input mode, the input signal is sampled at the rising edge of the ADCLK.

RENESAS

Detailed Timing Specifications

Detailed Timing Specifications when CDS_in Input Mode is Used

Figure 3 shows the detailed timing specifications when the CDS_in input mode is used, and table 8 shows each timing specification.

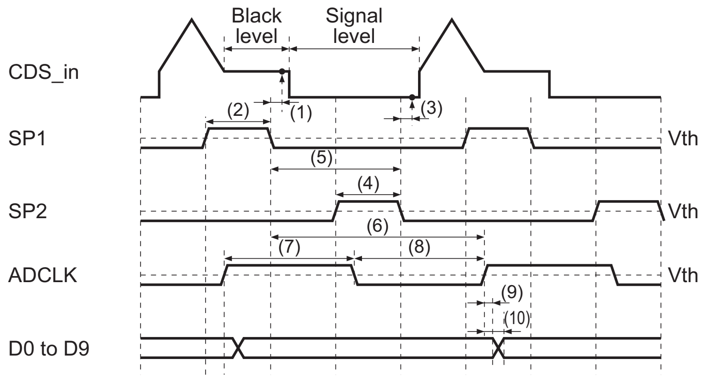


Figure 3 Detailed Timing Chart when CDS_in Input Mode is Used

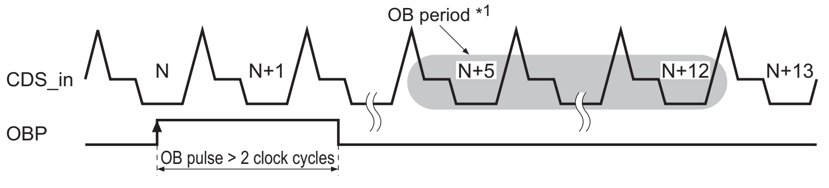
Table 8 Timing Specifications when the CDS_in Input Mode is Used

No.	Timing	Symbol	Min	Typ	Max	Unit
(1)	Black-level signal fetch time	t_{CDS1}	—	(1.5)	—	ns
(2)	SP1 'Hi' period	t_{CDS2}	Typ × 0.8	$1/4f_{CLK}$	Typ × 1.2	ns
(3)	Signal-level fetch time	t_{CDS3}	—	(1.5)	—	ns
(4)	SP2 'Hi' period	t_{CDS4}	Typ × 0.8	$1/4f_{CLK}$	Typ × 1.2	ns
(5)	SP1 falling to SP2 falling time	t_{CDS5}	Typ × 0.85	$1/2f_{CLK}$	Typ × 1.15	ns
(6)	SP1 falling to ADCLK rising inhibit time	t_{CDS6}	—	(5)	—	ns
(7), (8)	ADCLK t_{WH} min./t_{WL} min	$t_{CDS7,\,8}$	11	—	—	ns
(9)	ADCLK rising to digital output holding time	t_{CHLD9}	—	(7)	—	ns
(10)	ADCLK rising to digital output delay time	t_{COD10}	—	(16)	—	ns

OBP Detailed Timing Specifications

Figure 4 shows the OBP detailed timing specifications.

The OB period is from the fifth to the twelfth clock cycle after the OB pulse is inputted. The average of the black signal level is taken for eight input cycles during the OB period and it becomes the clamp level (DC standard).



Note: 1. Shifts ±1 clock cycle depending on the OBP input timing.

Figure 4 OBP Detailed Timing Specifications

Detailed Timing Specifications at Pre-Blanking

Figure 5 shows the pre-blanking detailed timing specifications.

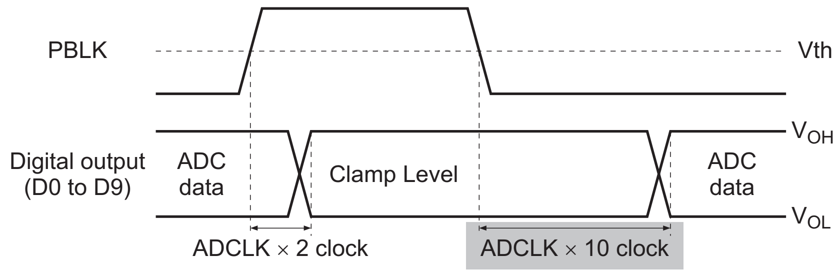


Figure 5 Detailed Timing Specifications at Pre-Blanking

Detailed Timing Specifications when ADC_in Input Mode is Used

Figure 6 shows the detailed timing chart when ADC_in input mode is used, and table 9 shows each timing specification.

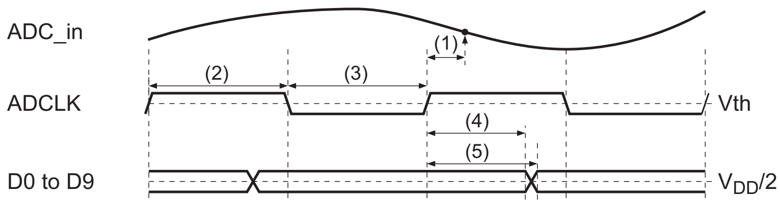


Figure 6 Detailed Timing Chart when ADC_in Input Mode is Used

Table 9 Timing Specifications when ADC_in Input Mode is Used

No.	Timing	Symbol	Min	Typ	Max	Unit
(1)	Signal fetch time	t_{ADC1}	—	(6)	—	ns
(2), (3)	ADCLK t_{WH} min./t_{WL} min.	$t_{ADC2, 3}$	Typ × 0.85	$1/2f_{ADCLK}$	Typ × 1.15	ns
(4)	ADCLK rising to digital output hold time	t_{AHLD4}	—	(14.5)	—	ns
(5)	ADCLK rising to digital output delay time	t_{AOD5}	—	(23.5)	—	ns

Dummy Clamp

It adjusts the mis-clamp which occurs when taking the photo under the highlight conditions. (Like a sun) Normally it woks with the OB clamp, however when black level is out of the range caused by hightlight enter to OB part, it changes to clamp processing by dummy bit level. Resister settings are follows.

D12, D11, D10 (Dummy CP) of address H'F7
0, 0, 0 ; OFF
0, 0, 1 ; +32
0, 1, 0 ; +64
0, 1, 1 ; +96
:
:
1, 1, 1 ; +224
The amount of offset are changes automatically depends on PGA gain in the LSI.

D8, D9 (DMCG) of address H'F7
The amount of feed back current can be reduced with only dummy clamp.
Data = 0:1/4
1:1/8
2:1/16
3:1/32

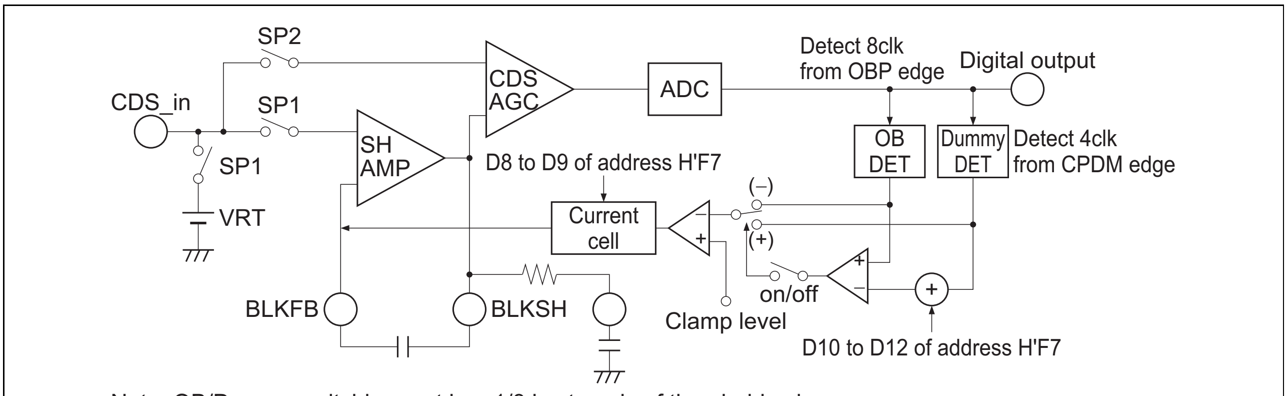


Figure 7 Internal Bias Circuitry

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Power supply voltage	Vdd(max)	4.1	V
Power dissipation	Pt(max)	500	mW
Operating power supply voltage	Vopr	2.70 to 3.45	V
Analog input voltage	V_{IN}(max)	–0.3 to AVdd +0.3	V
Digital input voltage	V_I(max)	–0.3 to DVdd +0.3	V
Operating temperature	Topr	–10 to +75	°C
Storage temperature	Tstg	–55 to +125	°C

Note: AVdd, AVss are analog power source systems of CDS, PGA, and ADC.
DVdd1, DVss1 are digital power source systems of CDS, PGA and ADC.
DVdd2, DVss2 are buffer power source systems of ADC output.
DVdd3, DVss3 are general digital power source systems of TG.
DVdd4, DVss4 are buffer power source systems of H1 and H2.

- Pin 2 multi bonds the DVss1 and DVss2
- When pin 64 is set to Low, pin 41 = STROB output, pin 39 = SUB_SW output
  When Hi, pin 41 = Vgate input, pin 39 = ADCLK input

Electrical Characteristics

(Unless specified, Ta = 25°C, AVdd = 3.0 V, DVdd = 3.0 V, and R_{BIAS} = 33 kΩ)

- Items Common to CDS_in and ADC_in Input Modes

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Remarks
Power supply voltage range	Vdd	2.70	3.00	3.45	V		
Conversion frequency	f_{CLK} hi	20	—	36	MHz	LoPwr = low *1	HD49351HBP
	f_{CLK} low	5.5	—	25	MHz	LoPwr = high	HD49351BP
Digital input voltage	V_{IH2}	$2.25 \times \frac{DVdd}{3.0}$	—	DVdd	V		All of digital input pin
	V_{IL2}	0	—	$0.6 \times \frac{DVdd}{3.0}$	V		
Digital output voltage	V_{OH}	DVdd –0.5	—	—	V	I_{OH} = –1 mA	
	V_{OL}	—	—	0.5	V	I_{OL} = +1 mA	
Digital input current	I_{IH}	—	—	50	μA	DVdd = V_{IH} = 3.0 V	
	I_{IL}	–50	—	—	μA	V_{IL} = 0 V	
Digital output current	I_{OZH}	—	—	50	μA	V_{OH} = Vdd	
	I_{OZL}	–50	—	—	μA	V_{OL} = 0 V	
ADC resolution	RES	—	10	—	bit		
ADC integral linearity	INL	—	(2)	—	LSBp-p	f_{CLK} = 20 MHz	
ADC differential linearity	DNL	—	(±0.3)	—	LSB	f_{CLK} = 20 MHz	*2
Sleep current	I_{SLP}	–100	0	100	μA	Fix digital input pin to 0 V, output pin should open	
Standby current	I_{STBY}	—	3	5	mA	Fix digital I/O pin to 0 V	
Digital output Hi-Z delay time	t_{HZ}	—	—	100	ns	R_L = 2 kΩ, C_L = 10 pF	Refer to figure 7
	t_{LZ}	—	—	100	ns		
	t_{ZH}	—	—	100	ns		
	t_{ZL}	—	—	100	ns		

Notes: 1. It is expressing on the frequency in an analog circuit part. Please keep in your mind that TG part has 2 divided, 3 divided mode.
2. Differential linearity is the calculated difference in linearity errors between adjacent codes.
3. Values within parentheses ( ) are for reference.

Electrical Characteristics (cont.)

(Unless specified, Ta = 25°C, AVdd = 3.0 V, DVdd = 3.0 V, and R_{BIAS} = 33 kΩ)

- Items for CDS_in Input Mode

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Remarks
Consumption current (1)	I_{DD1}	—	(65)	—	mA	f_{CLK} = 36 MHz	CDS_in mode LoPwr = low
Consumption current (2)	I_{DD2}	—	(50)	—	mA	f_{CLK} = 20 MHz	CDS_in mode LoPwr = high
CCD offset tolerance range	V_{CCD}	(–150)	—	(150)	mV		
Timing specifications (1)	t_{CDS1}	—	(1.5)	—	ns		Refer to table 8
Timing specifications (2)	t_{CDS2}	Typ × 0.8	$1/4f_{CLK}$	Typ × 1.2	ns		
Timing specifications (3)	t_{CDS3}	—	(1.5)	—	ns		
Timing specifications (4)	t_{CDS4}	Typ × 0.8	$1/4f_{CLK}$	Typ × 1.2	ns		
Timing specifications (5)	t_{CDS5}	Typ × 0.85	$1/2f_{CLK}$	Typ × 1.15	ns		
Timing specifications (6)	t_{CDS6}	—	(5)	—	ns		
Timing specifications (7)	t_{CDS7}	11	—	—	ns		
Timing specifications (8)	t_{CDS8}	11	—	—	ns		
Timing specifications (9)	t_{CHLD9}	—	(7)	—	ns	C_L = 10 pF	
Timing specifications (10)	t_{COD10}	—	(16)	—	ns	C_L = 10 pF	
Clamp level	CLP(00)	—	(14)	—	LSB		
	CLP(09)	—	(32)	—	LSB		
	CLP(31)	—	(76)	—	LSB		
PGA gain at CDS input	PGA(0)	–4.4	–2.4	–0.4	dB		
	PGA(63)	4.1	6.1	8.1	dB		
	PGA(127)	12.5	14.5	16.5	dB		
	PGA(191)	21.0	23.0	25.0	dB		
	PGA(255)	29.4	31.4	33.4	dB		

Note: Values within parentheses ( ) are for reference.

- Items for ADC_in Input Mode

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Remarks
Consumption current (3)	I_{DD3}	—	(35)	—	mA	f_{CLK} = 36 MHz	ADC_in mode LoPwr = low
Consumption current (4)	I_{DD4}	—	(20)	—	mA	f_{CLK} = 25 MHz	ADC_in mode LoPwr = high
Timing specifications (11)	t_{ADC1}	—	(6)	—	ns		Refer to table 9
Timing specifications (12)	t_{ADC2}	Typ × 0.85	$1/2f_{ADCLK}$	Typ × 1.15	ns		
Timing specifications (13)	t_{ADC3}	Typ × 0.85	$1/2f_{ADCLK}$	Typ × 1.15	ns		
Timing specifications (14)	t_{AHLD4}	—	(14.5)	—	ns	C_L = 10 pF	
Timing specifications (15)	t_{AOD5}	—	(23.5)	—	ns	C_L = 10 pF	
Input current at ADC input	IIN_{CIN}	–110	—	110	μA	V_{IN} = 1.0 to 2.0 V	
Clamp level at ADC input	OF2	462	512	562	LSB		
PGA gain at ADC input	GSL(0)	0.45	0.57	0.72	Times		
	GSL(63)	1.36	1.71	2.16	Times		
	GSL(127)	2.27	2.86	3.60	Times		
	GSL(191)	3.18	4.00	5.04	Times		
	GSL(255)	4.08	5.14	6.47	Times		

Note : Values within parentheses ( ) are for reference.

Serial Interface Specifications

Timing Specifications

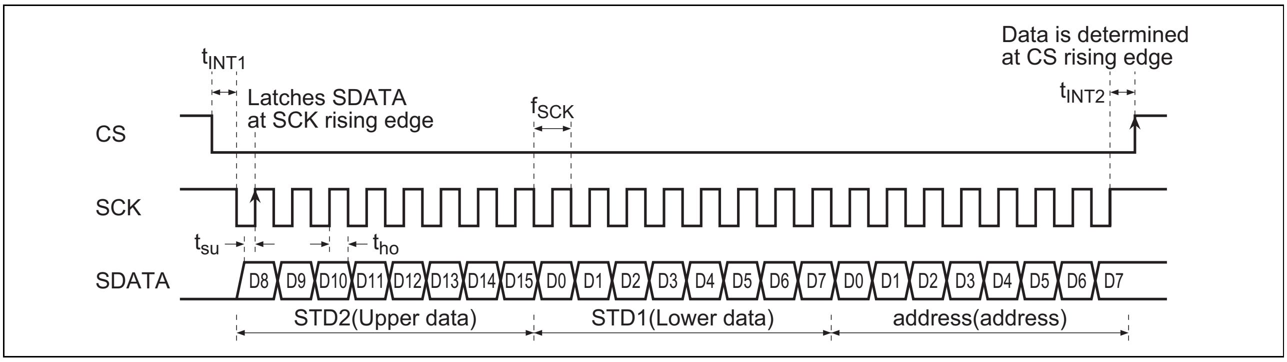


Figure 8 Serial Interface Timing Specifications

Item	Min	Max
f_{SCK}	—	5 MHz
$t_{INT1,2}$	50 ns	—
t_{su}	50 ns	—
t_{ho}	50 ns	—

Notes:
1. 3 byte continuous communications.
2. Input SCK with 24 clock when CS is Low.
3. It becomes invalid when data communications are stopped on the way.
4. Data becomes a default with hardware reset.
5. Input more than double frequency of SCK to the CLK_in when transfer the serial data.

The Kind of Data

Data address has 256 type. H’00 to H’FF

H’00
:
:
H’EF — Data at timing generator part

H’F0
:
:
H’FF — Data at CDS part

Address map of each data referred to other sheet.
Details of timing generator refer to the timing chart on the other sheet together with this specification.
This specification only explains about the data of CDS part.

Explanation of Serial Data of CDS Part

Serial data of CDS part are assigned to address H'F0 to H'F8. Functions are follows.

Address								STD1[7:0] (L)								STD2[15:8] (H)							
1	1	1	1	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13					
								PGA gain								test_I1							

- PGA gain (D0 to D7 of address H'F0)
  Details are referred to page 6 block diagram.
  At CDS_in mode: –2.36 dB + 0.132 dB × N (Log linear)
  At ADC_in mode: 0.57 times + 0.01784 times × N (Times linear)
  ∗: Full-scale digital output is defined as 0 dB when 1 V is input.

  Above PGA gain definition means input signal 1 Vp-p to CDS_in, and set N = 18 (correspond 2.36 dB), and then PGA outputs the 2 V full-range, and also ADC outputs the full code (1023).
  This mean offset gain of PGA has 6 dB – 2.36 dB = 3.64 dB, therefore it should be decided that how much dB add on.

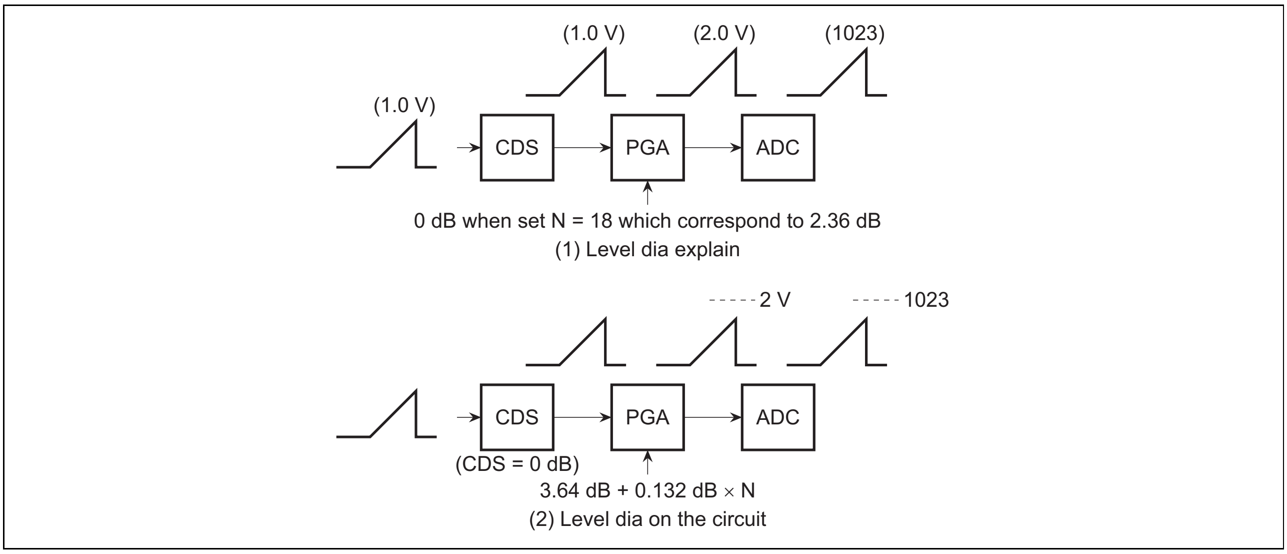


Figure 9 Level Dia of PGA

- Test_I1 (D13 to D15 of address H'F0)
  It controls the standard current of analog amplifier systems of CDS, PGA. Use data = 4 (D15 = 1) normally.
  When data = 0, 50% current value with default
  When data = 4, default
  When data = 7, 150% current value with default

Address								STD1[7:0] (L)								STD2[15:8] (H)							
1	1	1	1	0	0	0	1				D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8
											test0	MINV	LINV	STBY	SLP	test_I2		SHSW_fsel				SHA_fsel	

- SLP and STBY (D0, D1 of address H'F1)
  SLP: Stop the all circuit. Consumption current of CDS part is less than 10 µA.
  Start up from offset calibration when recover is needed.
  STBY: Only the standard voltage generating circuit is operated. Consumption current of CDS part is about 3 mA.
  Allow 50 H time for feedback clamp is stabilized until recover.

- Output mode (D2 to D4 of address H'F1 and address H'F4 of D6)
  It is a test mode. Combination details are page 8. Normally set to all 0.
- SHA-fsel (D8 to D9 of address H'F1)
  It is a LPF switching of SH amplifier. Frequency characteristics are referred to page 9. To get rough idea, set the double cut off frequency point with using.
- SHSW-fsel (D10 to D13 of address H'F1)
  It is a time constant which sampling the black level of SH amplifier. Frequency characteristics are referred to page 9. To get rough idea, set the double cut off frequency point with using. S/N changes by this data, so find the appropriate point with set data to up/down.
- Test_I2 (D14 to D15 of address H'F1)
  Current of ADC analog part can be set minutely. Normally use data = 0.
  0: Default (100%)
  1: 150%
  2: 50%
  3: 80%

Address								STD1[7:0] (L)								STD2[15:8] (H)							
1	1	1	1	0	0	1	0				D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8
											Clamp level					Reset	AD_sel	CDS_buff	Low_pwr	HGain-Nsel		HGstop-Hsel	

- Clamp (D0 to D4 of address H'F2)
  Determine the OB part level with digital code of ADC output.
  Clamp level = setting data × 2 + 14
  Default data is 9 = 32 LSB.
- HGstop-Hsel, HGain-Nsel (D8 to D11 of address H'F2)
  Determine the lead-in speed of OB clamp. Details are referred to page 7. PGA gain need to be changed for switch the high speed leading mode. Transfer the gain +1/–1 to previous field, its switch to high speed leading mode.
- Low_PWR (D12 of address H'F2)
  Switch circuit current and frequency characteristic.
  Data = 0: 40 MHz guarantee
  Data = 1: 25 MHz guarantee
- ADSEL (D14 of address H'F2)
  Data = 0: Select CDS_in
  Data = 1: Select ADC_in
- Reset (D15 of address H'F2)
  Software reset.
  Data = 1: Normal
  Data = 0: Reset

  Offset calibration should be done when starting up with using this bit. Details are referred to page 23.

Address								STD1[7:0] (L)								STD2[15:8] (H)							
1	1	1	1	0	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8

- Address H'F3 are all testing data.
  Normally set to all 0., or do not transfer the data.

Address								STD1[7:0] (L)								STD2[15:8] (H)							
1	1	1	1	0	1	0	0	D7	D6	D5	D4	D3	D2	D1	D0				D12	D11	D10	D9	D8
								VD latch	H12_Buff				MON						Gray_test			Gray code	

- MON (D0 to D2 of address H'F4)
  Select the pulse which output to pin MON (pin 60).
  When D0 to D2: 0, Fix to Low   When 1, ADCLK
  When 2, SP1   When 3, SP2
  When 4, OBP   When 5, PBLK
  When 6, CPDM   When 7, DLL_test
- H12Baff (D3 to D6 of address H'F4)
  Select the buffer size which output to pin H1A, H2A (pin 22, 26).
  D3: 2 mA buffer
  D4: 4 mA buffer
  D5: 10 mA buffer
  D6: 14 mA buffer

  Above data can be on/off individually. Default is D6 can be on only. (18 mA buffer)
- VD latch (D7 of address H'F4)
  Data = 0: Gain data is determined when CS rising
  Data = 1: Gain data is determined when VD rising
- Gray (D8 to D9 of address H'F4)
  ADC output code can be change to following types. Differential code is mentioned to next page.

Gray Code [1]	**Gray Code [0]**	**Output Code**
0	0	Binary code
0	1	Gray code
1	0	Differential encoded binary
1	1	Differential encoded gray

- Gray_test (D10 to D12 of address H'F4)
  Data which determine the differential code and standard phase of gray code.

- Gray code (D8 to D12 of address H’F4)

  ADC output code can be change to following type by differential code gray SW (D9, D8).

  Binary code at D8: 0, Gray code at D8: 1

  Normal at D9: 0, differential code at D9: 1

  Differential code and gray code are recommended for this countermeasure. Figure 10 indicates circuit block. When luminance signal changes are smoothly, the number of bit of switching digital output bit can be reduced and easily to reduce the ripple using this function. This function is especially effective for longer the settings of sensor more than clk = 30 MHz, and ADC output.

  Figure 12 indicates the timing specifications.

Standard Phase (D10)	Standard Phase (D11)	Standard Data Output timing at Selecting the Differential Code
0	0	Third and fourth
1	0	Fourth and fifth
0	1	Fifth and sixth
1	1	Sixth and seventh

Note: Color filter is different1 in the number of pixels with odd number and even number therefore first 2 pixcels should be standard.

- adck phase (D12): ADCK polar to OBP

  When 0: Select positive edge

  When 1: Select negative edge

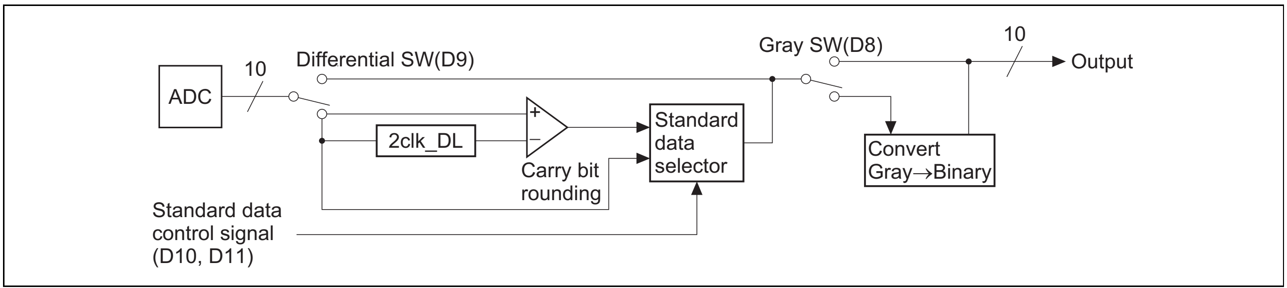


Figure 10 Differential Code and Gray Code Circuit

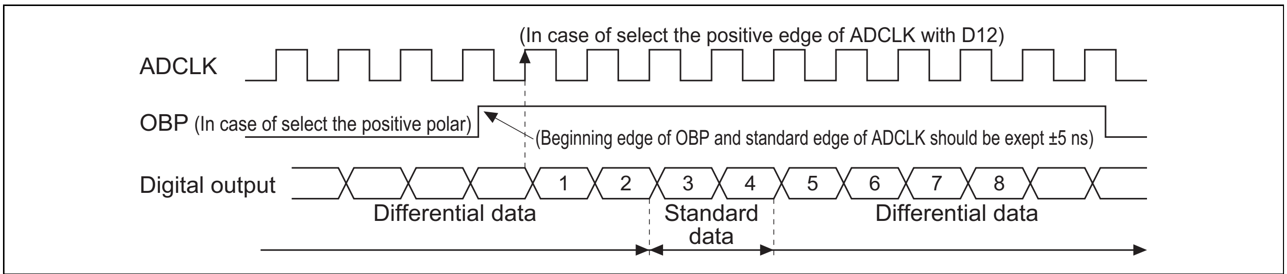


Figure 11 Timing Specification of Differential Code

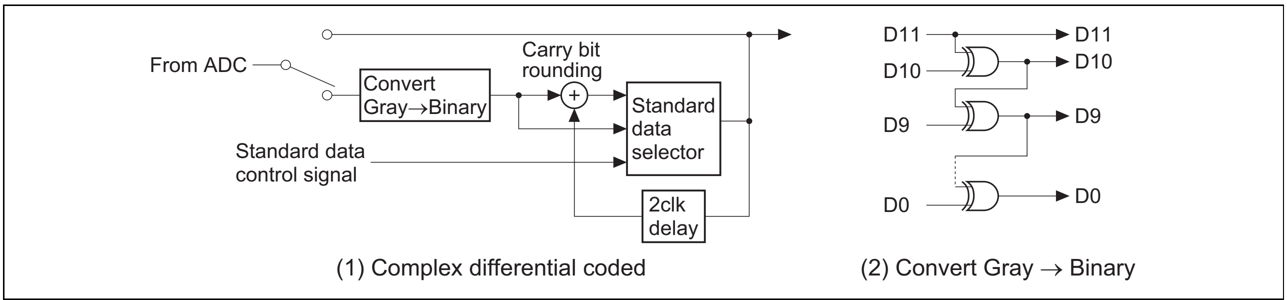


Figure 12 Complex Circuit Example at the DSP Side

Address								STD1[7:0] (L)								STD2[15:8] (H)							
1	1	1	1	0	1	0	1	D7	D6	D5	D4	D3	D2	D1	D0				D12	D11	D10	D9	D8
								P_RG		P_ADCLK		P_SP2		P_SP1					DLL current	DLL steps			

Address								STD1[7:0] (L)								STD2[15:8] (H)							
1	1	1	1	1	0	0	0		D6	D5	D4		D2	D1	D0	D15	D14	D13	D12		D10	D9	D8
									P_SP2				P_SP1			2,3 divided select	P_RG				P_ADCLK		

- Address H'F5 sets the DLL delay time and selects the 1/4 phase. Details are on the next page. And D15 of address H'F8 can switch 2/3 divided mode but ensure that this address data relative to valid/invalid.

	D15 of address H'F8 = 0	**D15 of address H'F8 = 1**
Divided mode	Select the 2 divided, 1/4 phase	Select the 3 divided, 1/6 phase
D0 to D7 of address H'F5	Valid	Invalid
D0 to D14 of address H'F8	Invalid	Valid

- Phase settings of high speed pulse (address H'F5 to H'F8)
  (1) Select the 1/4 phase from figure 13 at 2 divided mode (D15 = 0 of address H'F8).
  Select the 1/6 phase from figure 14 at 3 divided mode (D15 = 1 of address H'F8).
  ·····P_SP1, P_SP2, P_ADCLK, P_RG
  (2) Then select the necessary delay time from figure 15.
  ·····DL_SP1, DL_SP2, DL_RG, DL_ADCLK
  RG can be set both of rising / falling edge optionally.

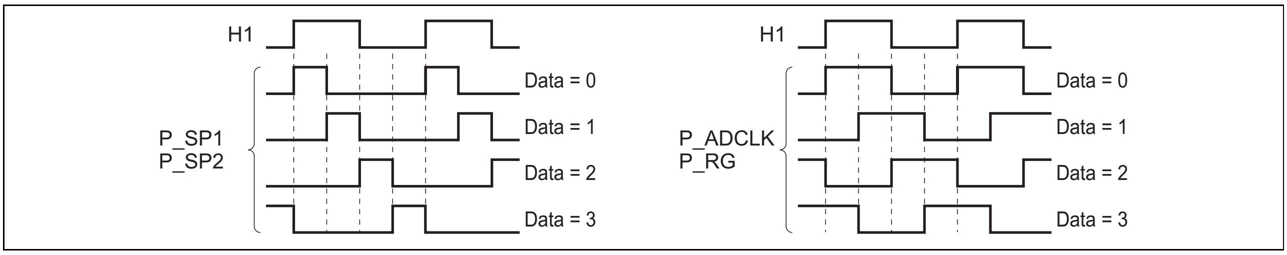


Figure 13 2 Divided Mode, 1/4 Phase Select (Valid at D15 = 0 of address H'F8)

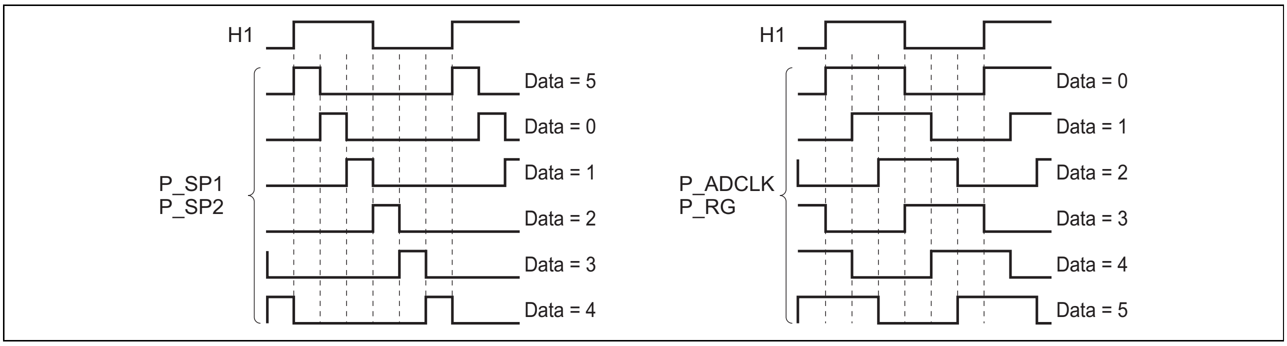


Figure 14 3 Divided Mode, 1/6 Phase Select (Valid at D15 = 1 of address H'F8)

Default Value of Each Phases

	P_SP1	**P_SP2**	**P_ADCLK**	**P_RG**
2 divided mode	1	2	1	0
3 divided mode	0	3	1	5

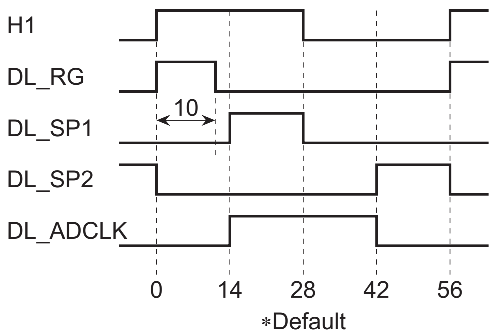
Note: 50% of duty pulse makes tr, tf of RG by DLL.

Address								STD1[7:0] (L)								STD2[15:8] (H)							
1	1	1	1	0	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0				D12	D11	D10	D9	D8
								DL_SP2				DL_SP1							CDS_test	DL_ADCLK			

Address								STD1[7:0] (L)								STD2[15:8] (H)							
1	1	1	1	0	1	1	1	D7	D6	D5	D4	D3	D2	D1	D0				D12	D11	D10	D9	D8
								DL_RG_f				DL_RG_r							Dummy clamp th			Dummy clamp current	

(3) Setting method of DLL

1. DLL step decides the how many divide the 1 cycle of sensor CLK. For reference, set 1 ns(when 2 ns DLL_current bit = 0, when 1 set to 1 ns)
   Can be set 16 to 64 steps by 4 steps.
   Steps = 4 + (4 × N); possible to set N = 3 to 15
   Recommended steps is clk_in = when 11 to 14 MHz: H'0E(60 steps)
   when 14 to 22MHz: H'09(40 steps)
   when 22 to 50MHz: H'1E(60 steps)
   when 50 to 72MHz: H'19(40 steps)
2. Can be change each 4 type of pulse 0 to 15 steps with 1 step. (1 ns or 2 ns divide)
3. Select the 2 ns divide when sensor CLK is less than 15 MHz.



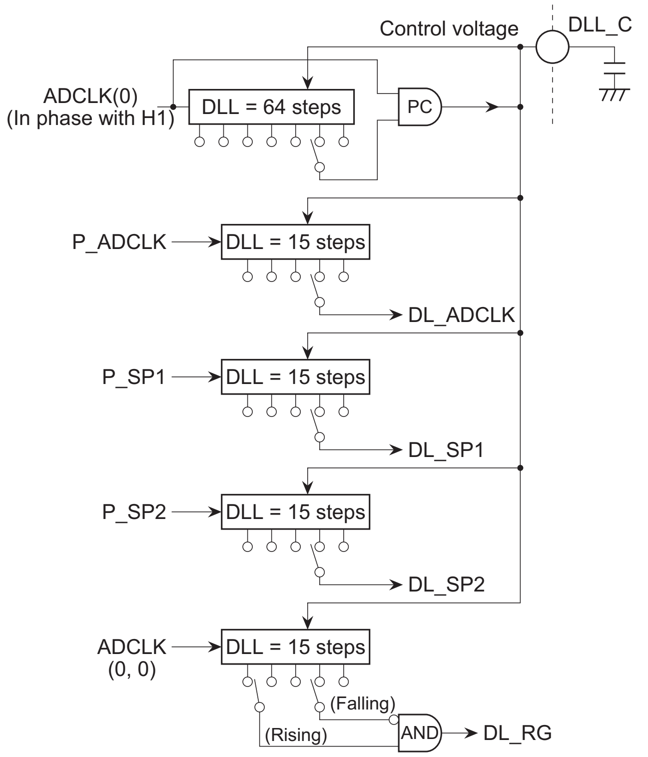


Figure 15 Analog Delay (DLL) Circuit Block.

- CDS_test (D12 of address H'F6)
  It is testing data. Normally set to 0.
- Dummy clamp current (D9 to 8 of address H'F7)

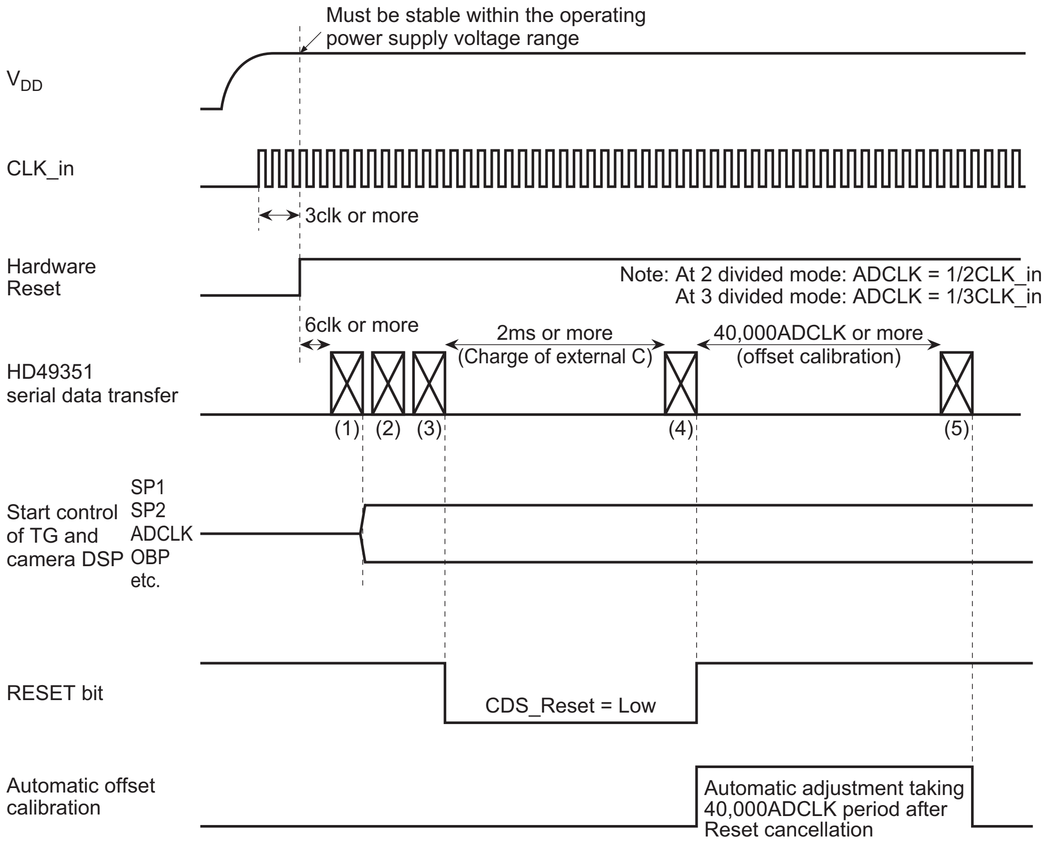
Data =	When 0, 1/4	When 1, 1/8
	When 2, 1/16	When 3, 1/32

  Details are refer to page 13.
- Dummy clamp threshold (D12 to 10 of address H'F7)

Data =	When 0, off	When 1, +32
	When 2, +64	When 3, +96
	When 4, +128	When 5, +160
	When 6, +192	When 7, +224

  Details are refer to page 13.

Operation Sequence at Power On



The following describes the above serial data transfer. For details of resistor settings are referred to serial data function table.

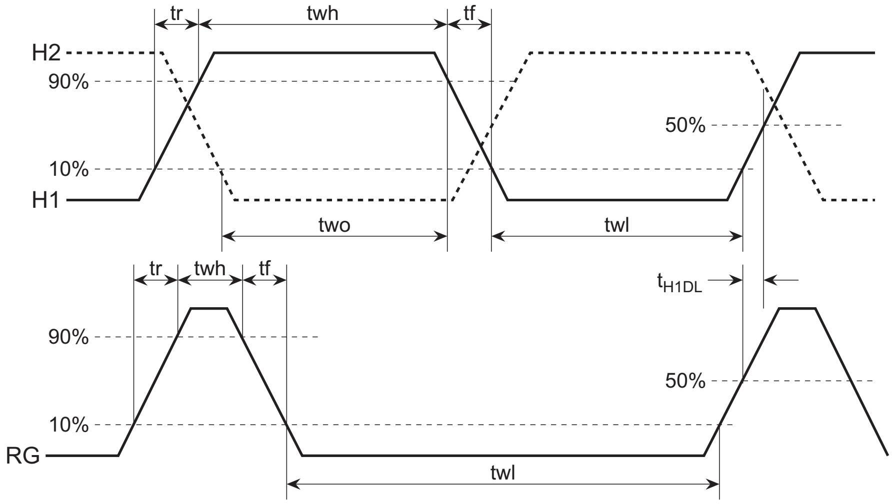
(1) Resistor transfer of TG part : Wait more than 6clk after release the hardware Reset and then transfer the necessary data to TG part.
(2) DLL data transfer of CDS part : Transfer the phase data of RG, SP1, SP2, ADCLK of CDS part.
(3) Reset=L of CDS part : Transfer Reset bit = 0 of address H'F2.
(4) Reset=H of CDS part : Transfer Reset bit = 1 of address H'F2. (Reset release)
(5) Other data of CDS part : Transfer the SH_SW_fsel and other PGA.

* Before transfer the Reset bit = 0, TG series pulse need to be settled, so address H'00 to H'EF of TG part and H'F4 to H7F7 of CDS part should transfer in advance.

Figure 16 Operation Sequence at Power On

Timing Specifications of High Speed Pulse

• H1, H2, RG waveform



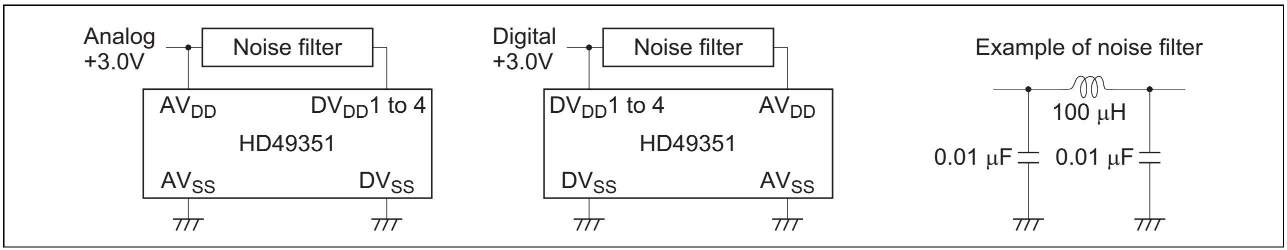
Item	twh			twl			tr			tf			Unit	Load capacitance
	min	typ	max	min	typ	max	min	typ	max	min	typ	max		
H1/H2	14	20	—	14	20	—	—	8.0	14	—	8.0	14	ns	165 pF
RG	7	10	—	—	37	—	—	4.0	—	—	4.0	—	ns	15 pF
XV1 to 4	—	—	—	—	—	—	—	20	—	—	20	—	ns	15 pF
CH1 to 4	—	—	—	—	—	—	—	20	—	—	20	—	ns	15 pF
XSUB/SUB_SW	—	—	—	—	—	—	—	20	—	—	20	—	ns	15 pF

Item	two			Unit
	min	typ	max	
H1/H2 overlap	12	20	—	ns

Power supply specification of H1, H2, RG are 3.0 V to 3.3 V.
Values are sensor CLK = when 18 MHz.

Notice for Use

1. Careful handling is necessary to prevent damage due to static electricity.
2. This product has been developed for consumer applications, and should not be used in non-consumer applications.
3. As this IC is sensitive to power line noise, the ground impedance should be kept as small as possible. Also, to prevent latchup, a ceramic capacitor of 0.1 µF or more and an electrolytic capacitor of 10 µF or more should be inserted between the ground and power supply.
4. Common connection of AV_{DD} and DV_{DD} should be made off-chip. If AV_{DD} and DV_{DD} are isolated by a noise filter, the phase difference should be 0.3 V or less at power-on and 0.1 V or less during operation.
5. If a noise filter is necessary, make a common connection after passage through the filter, as shown in the figure below.



6. Connect AV_{SS} and DV_{SS} off-chip using a common ground. If there are separate analog system and digital system set grounds, connect to the analog system.
7. When V_{DD} is specified in the data sheet, this indicates AV_{DD} and DV_{DD}.
8. No Connection (NC) pins are not connected inside the IC, but it is recommended that they be connected to power supply or ground pins or left open to prevent crosstalk in adjacent analog pins.
9. To ensure low thermal resistance of the package, a Cu-type lead material is used. As this material is less tolerant of bending than Fe-type lead material, careful handling is necessary.
10. The infrared reflow soldering method should be used to mount the chip. Note that general heating methods such as solder dipping cannot be used.
11. Serial communication should not be performed during the effective video period, since this will result in degraded picture quality. Also, use of dedicated ports is recommended for the SCK and SDATA signals used in the HD49330AF. If ports are to be shared with another IC, picture quality should first be thoroughly checked.
12. At power-on, automatic adjustment of the offset voltage generated from PGA, ADC, etc., must be implemented in accordance with the power-on operating sequence (see page 23).
13. Ripple noise of DC/DC converter which generates the voltage of analog part should set under –50 dB with power supply voltage.

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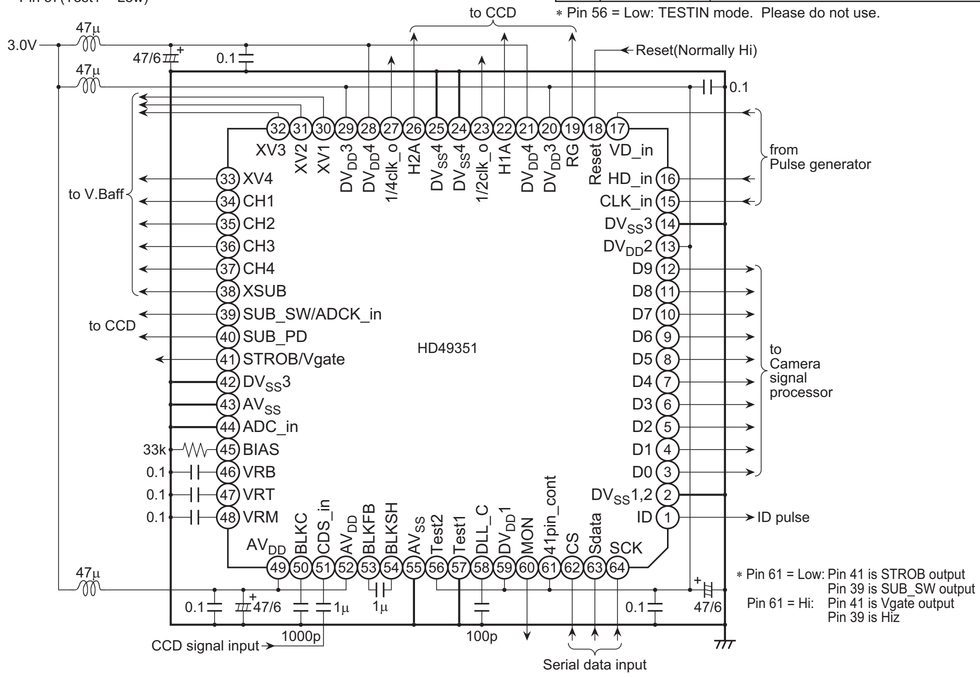
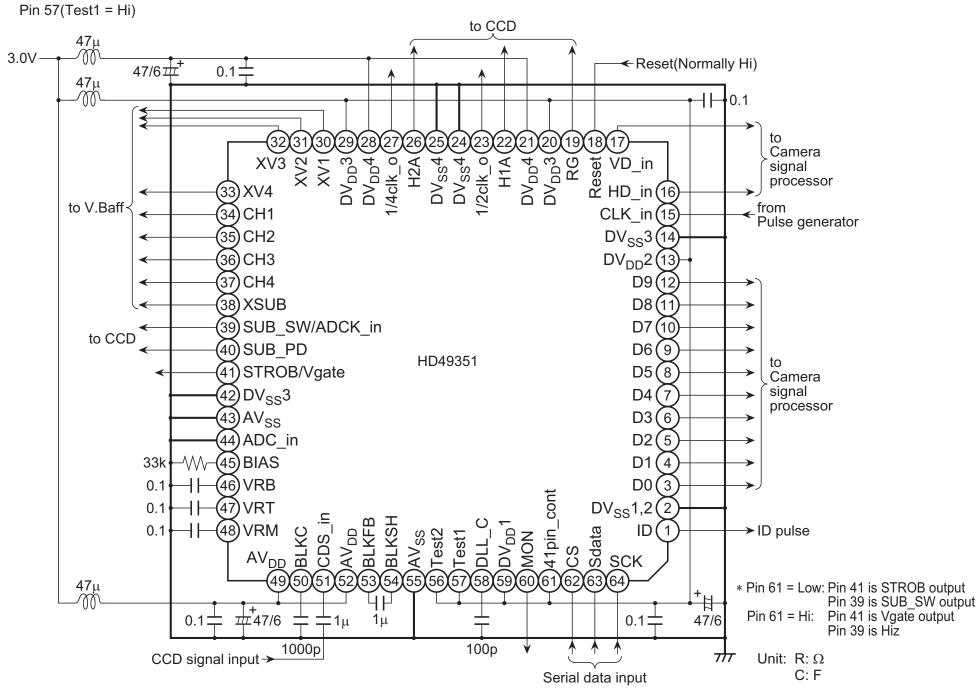
Example of Recommended External Circuit

Pin 57	Mode	Specification
Low	Slave mode	CLK, HD, VD input from SSG.
Hi	Master mode	HD, VD output

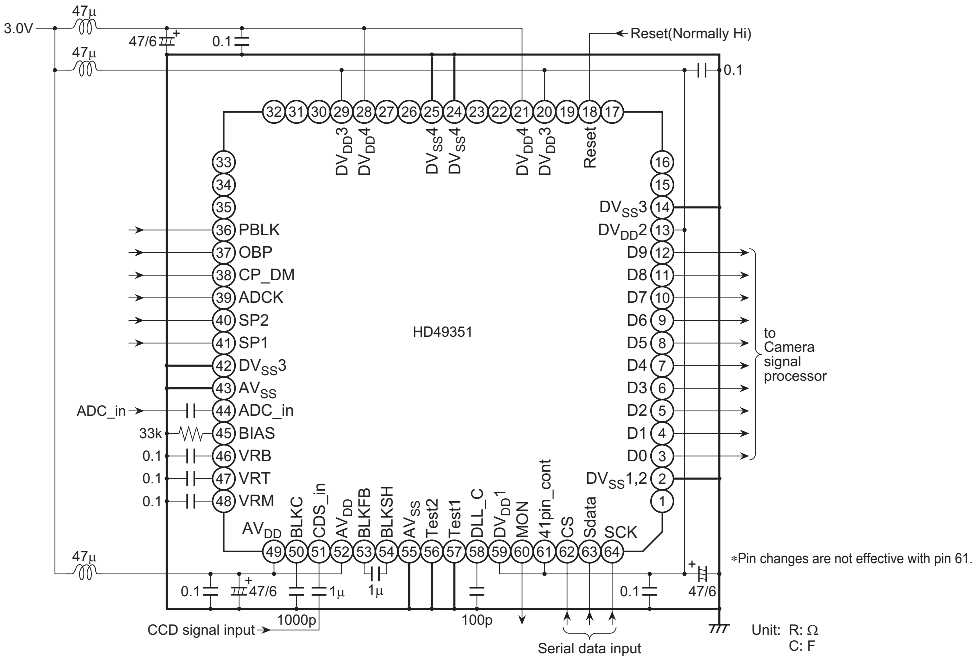
• Slave mode
Pin 57(Test1 = Low)



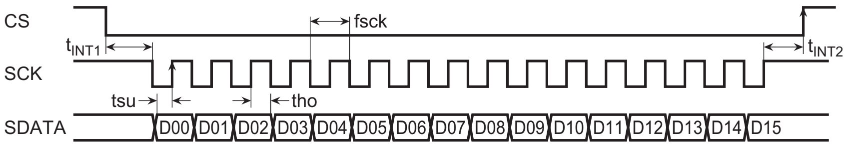
• Master mode
Pin 57(Test1 = Hi)



- CDS single operating mode
  Pin 56(Test2 = Low) *Pin 57 is "Don't care" in this mode.



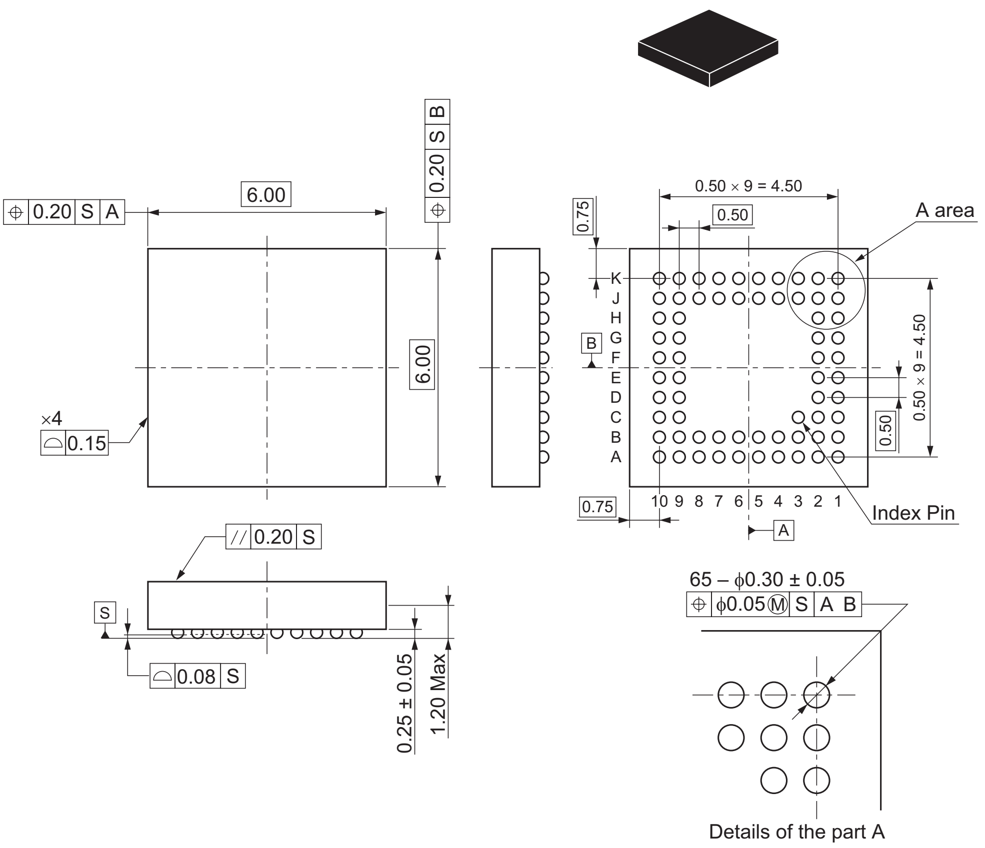
Serial data when CDS single operation mode are following resister specifications.
(Latch timing specification is same as normal mode)



	Resister 0		Resister 1		Resister 2		Resister 3		Resister 4		Resister 5		Resister 6		Resister 7	
D00	Low	0	High	1	Low	0	High	1	Low	0	High	1	Low	0	High	1
D01	Low	0	Low	0	High	1	High	1	Low	0	Low	0	High	1	High	1
D02	Low	0	Low	0	Low	0	Low	0	High	1	High	1	High	1	High	1
D03	X	0	SLP Low: Normal High: Sleep	0	Clamp(0)	1		0	MON(0)	0	P_SP1(0)	1	DL_SP1(0)	0	DL_RG_r(0)	0
D04	X	0	STBY Low: Normal High: Standby	0	Clamp(1)	0		0	MON(1)	0	P_SP1(1)	0	DL_SP1(1)	0	DL_RG_r(1)	0
D05	PGA(0) LSB	0	Output mode(LINV)	0	Clamp(2)	0		0	MON(2)	0	P_SP2(0)	1	DL_SP1(2)	0	DL_RG_r(2)	0
D06	PGA(1)	0	Output mode(MINV)	0	Clamp(3)	1		0	H12Baff(0)	0	P_SP2(1)	1	DL_SP1(3)	0	DL_RG_r(3)	0
D07	PGA(2)	0	Output mode(Test0)	0	Clamp(4)	0		0	H12Baff(1)	0	P_ADCLK(0)	1	DL_SP2(0)	0	DL_RG_f(0)	0
D08	PGA(3)	0	SHA-fsel(0)	0	HGstop-Hsel(0)	0		0	H12Baff(2)	0	P_ADCLK(1)	0	DL_SP2(1)	0	DL_RG_f(1)	1
D09	PGA(4)	0	SHA-fsel(1)	0	HGstop-Hsel(1)	0	test	0	H12Baff(3)	1	P_RG(0)	0	DL_SP2(2)	0	DL_RG_f(2)	0
D10	PGA(5)	0	SHSW-fsel(0)	0	HGain-Nsel(0)	0		0	VD latch	0	P_RG(1)	0	DL_SP2(3)	0	DL_RG_f(3)	1
D11	PGA(6)	0	SHSW-fsel(1)	0	HGain-Nsel(1)	0		0	Gray1	0	DLL_CK(0)	1	DL_ADCLK(0)	0	DMCG(0)	0
D12	PGA(7) MSB	0	SHSW-fsel(2)	0	LoPwr Low: Normal High: Low power	1		0	Gray2	0	DLL_CK(1)	0	DL_ADCLK(1)	0	DMCG(1)	0
D13	Test_I1 (0)	0	SHSW-fsel(3)	0	X	0		0	Gray_ts(0)	0	DLL_CK(2)	1	DL_ADCLK(2)	0	Dummy CP(0)	0
D14	Test_I1 (1)	0	Test_I2 (0)	0	ADSEL Low:CDSin High:ADin	0		0	Gray_ts(1)	0	DLL_CK(3)	1	DL_ADCLK(3)	0	Dummy CP(1)	0
D15	Test_I1 (2)	1	Test_I2 (1)	0	Reset Low: Reset High: Normal	1		0	Gray_ts(2)	0	DLL_current	1	CDS_test	0	Dummy CP(2)	0

Package Dimensions

Unit: mm



Package Code	TFBGA0606-65
JEDEC	—
JEITA	—
Mass (reference value)	0.056 g

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