Am27S65

4096-Bit (1024 x 4) Bipolar Registered PROM
with SSR ™ Diagnostics Capability

DISTINCTIVE CHARACTERISTICS

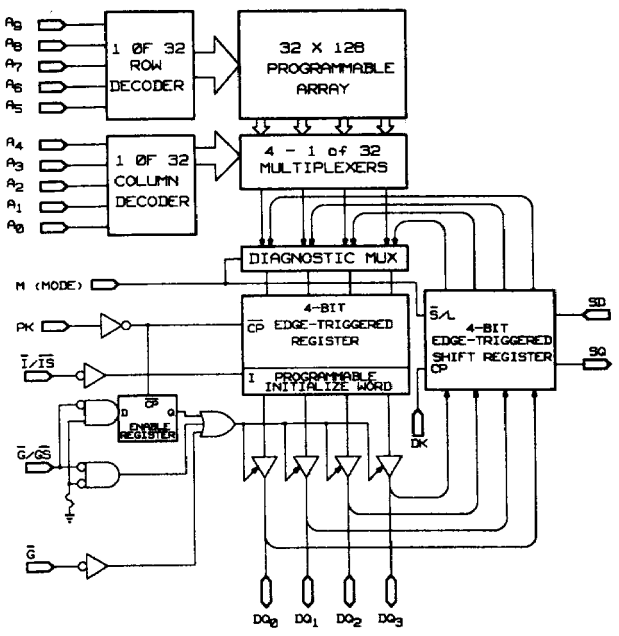
- On-chip diagnostic shift register for serial observability and controllability of the output register
- User-programmable Enable Pin for Asynchronous or Synchronous Enable operation
- User-programmable Initialization Pin for Asynchronous or Synchronous Initialize operation
- Slim, 24-pin, 300-mil lateral center package permits a reduction in board space over standard discrete PROM and registers
- Consumes approximately ½ the power of separate PROM/register combination for improved system reliability
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ. > 98%)
- Increased drive capability, 24 mA I_{OL}

GENERAL DESCRIPTION

This device contains a 4-bit parallel data register in the array-to-output path intended for normal registered data operations. In parallel with the output data registers is another 4-bit register with shifting capability, called a shadow register. As the name implies, the shadow register is intended to operate in the background of the normal output data register. This shadow register can be used in a systematic way to control and observe the output data register to exercise desired system functions during a diagnostic test mode.

To offer the system designer maximum flexibility, this device contains user-programmable architecture for Enable and Initialize. The unprogrammed state of these pins operates as Asynchronous inputs ($\overline{G}$) and ($\overline{I}$), respectively. An architecture word permits the programming of the functionality of these pins to Synchronous Enable ($\overline{GS}$) and Synchronous Initialize ($\overline{IS}$). A non-programmable Asynchronous Enable ($\overline{G}$) is also provided.

BLOCK DIAGRAM



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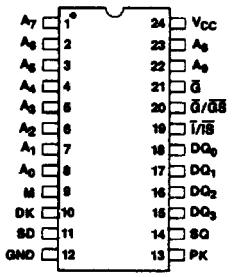
PRODUCT SELECTOR GUIDE

Part Number	27S65A	27S65	27S65A	27S65
Address Set-up Time	23 ns	30 ns	27 ns	35 ns
Clock-to-Output Delay	10 ns	15 ns	13 ns	20 ns
Operating Range	C	C	M	M

CONNECTION DIAGRAMS

Top View



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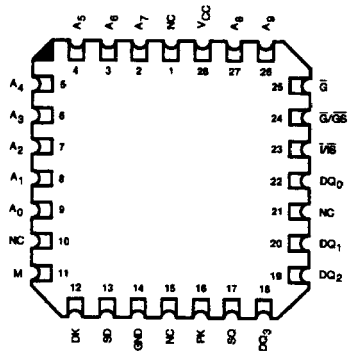

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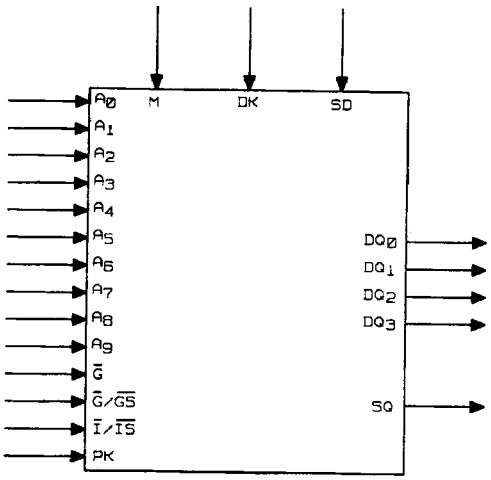
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



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