Ordering number : EN4128B

CMOS LSI

# LC8900KQ

## Digital Audio Interface Receiver

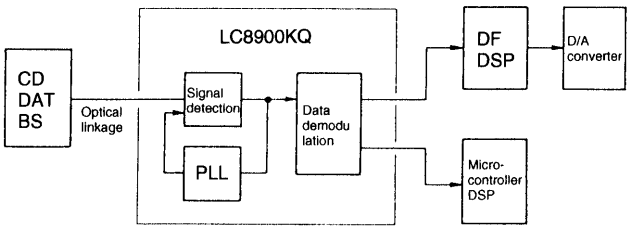
## Overview

The LC8900KQ is a CMOS LSI circuit chip that can be used to enable the EIAJ CP-1201 formatted data transmission between digital audio equipment. It is used by the receiving end and operates synchronously with input signals. This chip demodulates input signals into normally-formatted signals.

## Features

- On-chip PLL circuit: enables the LSI operation to be synchronous to the transmitted EIAJ format input signals.
- Four input pins and one output pin: The output pin enables the input data to be sent as they are.
- Two data output function modes: 20-bit data LSB first mode and 16-bit data MSB first mode.
- Four output clocks: Bit clock, LRCK, 384Fs and 256Fs. All these clocks are synchronized to the data.
- Various signal outputs: copy inhibit, emphasis on:off control, user's bit, validity flag and sampling frequency.
- LPF time constant select mode: This function can be used in the PLL lock-up state.
- Error detect signal output: If an input data error is detected, this LSI circuit chip outputs the error signal. In this case, the previous data will be output by the chip.
- Lock-up signal output: This signal is output when the internal PLL (Phase Locked Loop) block of the LSI circuit chip is locked.
- The chip has the pin to receive a signal for stopping the PLL operation.
- Control and processing mode via microcontroller interface: input pin select, copy information and sampling frequency output.
- Each input pin has an internal amplifier circuit.
- Si gate, CMOS process technology and single 5V power supply applicational and functional concept.

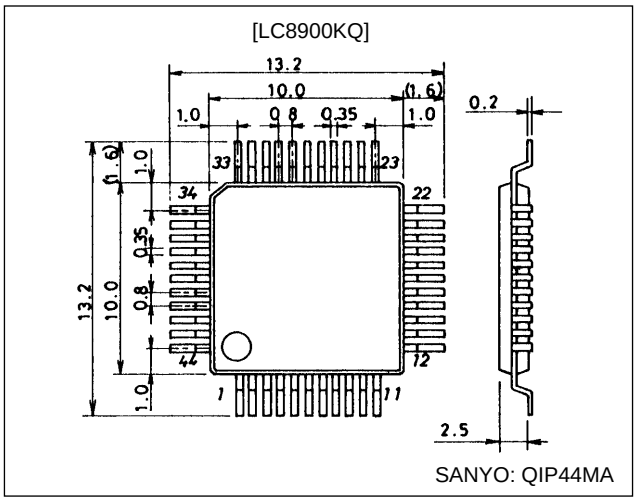
## Applicational and Functional Concept



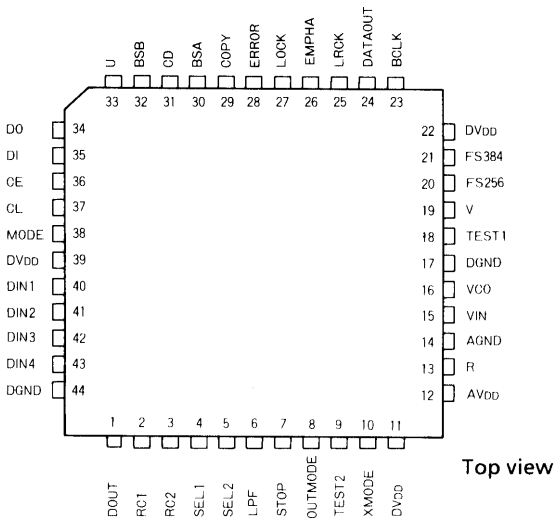

## Package Dimensions

unit:mm

**3148-QFP44MA**

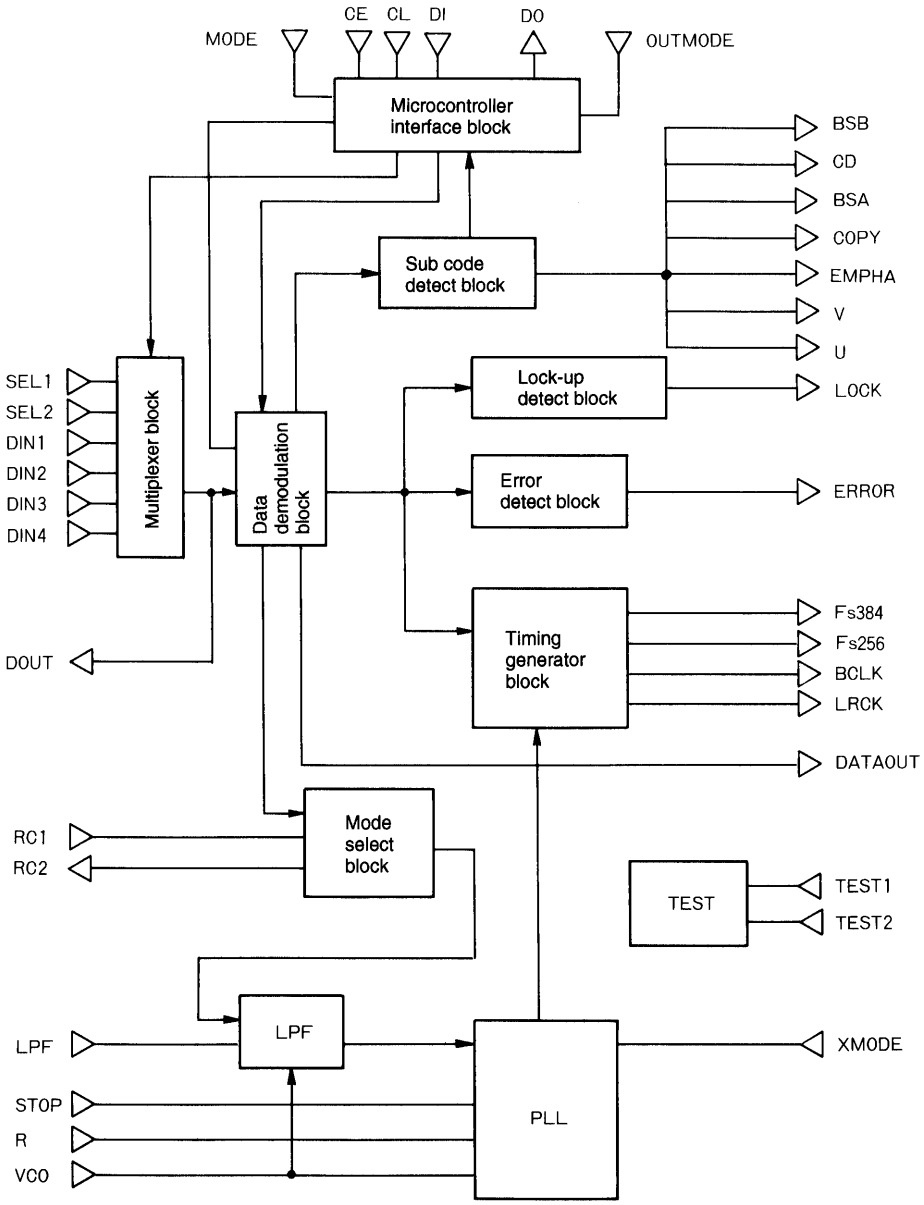


## Pin Assignment




Top view

## Block Diagram



## Pin Functions

| Pin No. | Pin Name | I/O Type | Functional Description |
|---|---|---|---|
| 1 | DOUT | O | Input data output pin. However, its output is fixed at the low level if the DIN4 input pin is selected. |
| 2 | RC1 | I | RC oscillation pin |
| 3 | RC2 | O | RC oscillation pin |
| 4 | SEL1 | I | Input pin select pin |
| 5 | SEL2 | I | Input pin select pin |
| 6 | LPF | I | High level = LPF time constant select mode. low level = LPF time constant fixed mode. Fixed to high in most cases. |
| 7 | STOP | I | High = level:Forces the VCO operation to stop. Fixed to low in most cases. |
| 8 | OUTMODE | I | Output data format select pin.<br>High = 20-bit LSB first data format.<br>Low = 16-bit MSB first data format |
| 9 | TEST2 | I | Test pin:Connected to the DGND in most cases. |
| 10 | XMODE | I | Input pin to start the PLL operation immediately after the LSI chip is powered on. |
| 11 | $DV_{DD}$ | | Digital power supply |
| 12 | $AV_{DD}$ | | Analog power supply |
| 13 | R | I | VCO oscillation bandwidth adjust pin |
| 14 | AGND | | Analog ground |
| 15 | Vin | I | VCO self oscillation frequency setting pin |
| 16 | VCO | O | PLL LPF pin |
| 17 | DGND | | Digital Ground |
| 18 | TEST1 | I | Test pin:Connected to the DGND in most cases. |
| 19 | V | O | Validity flag output pin |
| 20 | FS256 | O | 256 Fs clock output pin |
| 21 | FS384 | O | 384 Fs clock output pin |
| 22 | $DV_{DD}$ | | Digital Power Supply |
| 23 | BCLK | O | Bit clock output pin |
| 24 | DATAOUT | O | Audio data output pin |
| 25 | LRCK | O | L/R clock output pin, Lch = high, Rch = low |
| 26 | EMPHA | O | Emphasis control (on/off) output pin:High = emphasis mode. Low = none-emphasis mode. |
| 27 | LOCK | O | PLL lock state output pin:High = PLL locked state. Low = PLL unlocked state. |
| 28 | ERROR | O | Input data error detect signal output:High = error detected. |
| 29 | COPY | O | Copy information output pin |
| 30 | BSA | O | Input data sampling frequency indication:High = 2 kHz. |
| 31 | CD | O | Input data sampling frequency indication:High = 44.1 kHz. |
| 32 | BSB | O | Input data sampling frequency indication:High = 48kHz. |
| 33 | U | O | User's bit output pin |
| 34 | DO | O | Microcontroller interface output pin |
| 35 | DI | I | Microcontroller interface input pin |
| 36 | CE | O | Microcontroller interface chip enable input pin |
| 37 | CL | O | Microcontroller interface clock input pin |
| 38 | MODE | I | Microcontroller interface control input:High = microcontroller interface active mode.<br>Low = microcontroller interface inactive mode. |
| 39 | $DV_{DD}$ | | Digital power supply |
| 40 | DIN1 | I | Data input pin |
| 41 | DIN2 | I | Data input pin |
| 42 | DIN3 | I | Data input pin |
| 43 | DIN4 | I | Data input pin |
| 44 | DGND | | Digital ground |

# Specifications

## Absolute Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{DD}$ max | Ta = 25°C | –0.3 to +7.0 | V |
| Input/output voltage | $V_I$ · $V_O$ | Ta = 25°C | –0.3 to $V_{DD}$ +0.3 | V |
| Ambient operating temperature | Topr | | –30 to +75 | °C |
| Ambient storage temperature | Tstg | | –55 to +125 | °C |

## Allowable Operating Range at Ta = –30°C to +75°C

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | 4.5 | 5.0 | 5.5 | V |

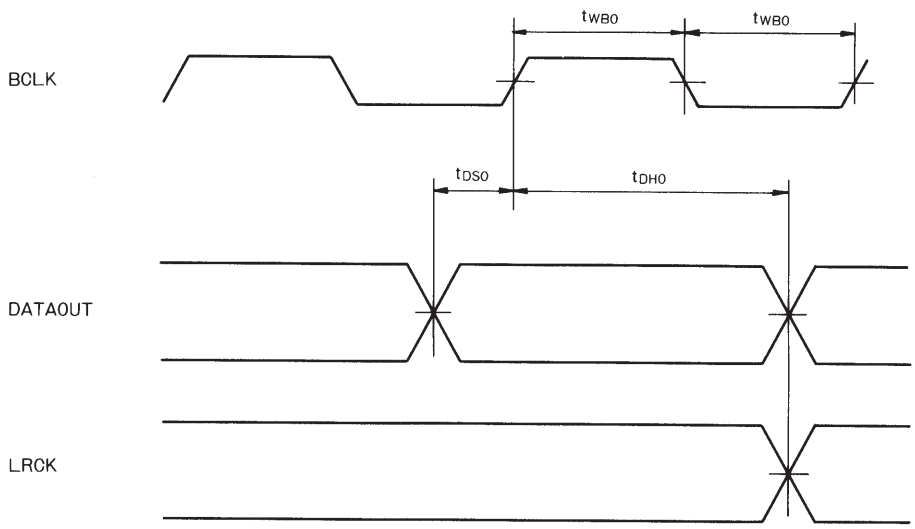
## DC Characteristics at Ta = –30 to +75°C, $V_{DD}$ = 4.5 V to 5.5 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Input high level voltage | $V_{IH}$ | *1 | 2.2 | | $V_{DD}$ + 0.3 | V |
| Input low level voltage | $V_{IL}$ | *1 | –0.3 | | 0.8 | V |
| Input high level voltage | $V_{IH}$ | *2 | 0.8 $V_{DD}$ | | $V_{DD}$ + 0.3 | V |
| Input low level voltage | $V_{IL}$ | *2 | –0.3 | | 0.2 $V_{DD}$ | |
| Output high level voltage | $V_{OH}$ | $I_{OH}$ = –1 µA | $V_{DD}$ – 0.05 | | | V |
| Output low level voltage | $V_{OL}$ | $I_{OL}$ = 1 µA | | | $V_{SS}$ + 0.05 | V |
| Current drain | $I_{DD}$ | *3 | | 11 | 12 | mA |
| Input amplitude | $V_{IN}$ | *4 | 0.4 | | $V_{DD}$ + 0.3 | $V_{P-P}$ |

## AC Characteristics at Ta = –30 to 75°C, $V_{DD}$ = 4.5 to 5.5 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Output pulse width | $t_{WBO}$ | Fs = 48kHz | 160 | | | ns |
| Output set-up time | $t_{DSO}$ | | 80 | | | ns |
| Output data hold time | $t_{DHO}$ | | 80 | | | ns |

Note 1: All input pins except DIN1, DIN2, DIN3, DIN4 and XMODE.
Note 2: XMODE pin
Note 3: $V_{DD}$=5.0V, Ta = 25 °C, input Fs=48 kHz.
Note 4: Before DIN1 to DIN4 input capacity is exceeded.

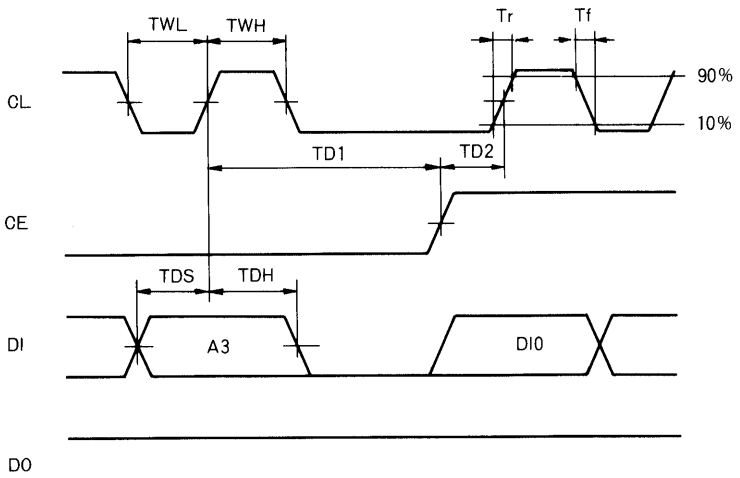


## AC Characteristics at the Microcontroller Interface Block at Ta = –30 to +75°C, $V_{DD}$ = 4.5V to 5.5V

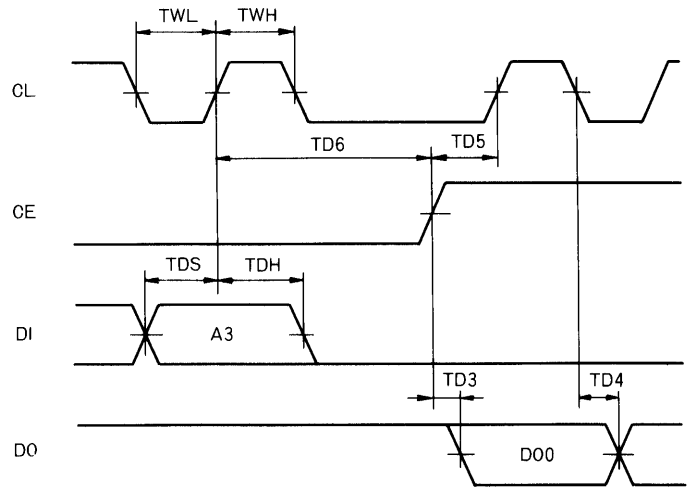
| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| CL low pulse width | TWL | | 100 | | | ns |
| CL high pulse width | TWH | | 100 | | | ns |
| Data set up time | TDS | | 50 | | | ns |
| Data hold time | TDH | | 50 | | | ns |
| CL rise time | Tr | CL, CE, DI | | | 30 | ns |
| CL fall time | Tf | CL, CE, DI | | | 30 | ns |
| CE delay time | TD1 | | 1.0 | | | µs |
| CL delay time | TD2 | | 50 | | | ns |
| Data delay time | TD3 | Load capacitance = 30 pF | | | 25 | ns |
| CL/data delay time | TD4 | Load capacitance = 30 pF | | | 50 | ns |
| CL delay time | TD5 | | 100 | | | ns |
| CL/CE delay time | TD6 | | 1.0 | | | µs |

## AC Characteristics at the Microcontroller Interface Block

Input mode operation

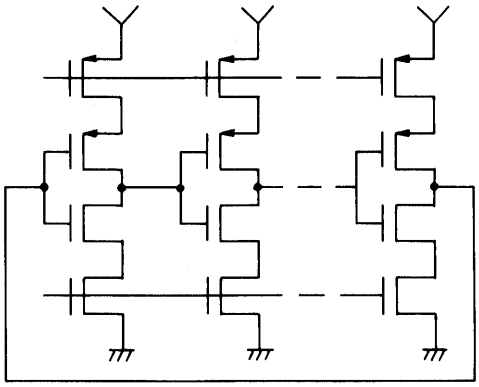



Output mode operation



## PLL VCO Functional Circuit Block

### VCO

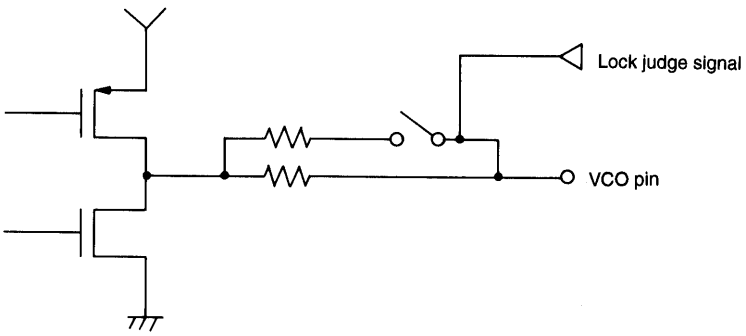


- The VCO (Voltage Controlled Oscillator) functional block consists of multiple ring oscillator ad shown above.
- The ring oscillator produces the frequencies from 3 MHz to 40 MHz according to the VCO pin voltages 0 V to 3 V.
- The VCO self oscillation frequency is determined by the VIN pin voltage.

### Phase Detector

- The phase detector circuit operates on the rising edge of the incoming signals. It compares the clock generated from the input signal with the VCO clock.

**LPF (Low-pass filter)**




- The charge pump and the LPF are shown above. The LPF time constant varies depending on the lock judge signal.

## DATA

(1) The relationship between the data input pins and the data select pins are shown in the table below.

| | SEL1 | SEL2 | DOUT |
|---|---|---|---|
| DIN1 | L | L | DIN1 data output |
| DIN2 | L | H | DIN2 data output |
| DIN3 | H | L | DIN3 data output |
| DIN4 | H | H | low level signal output (fixed level output) |

- Each input pin has an internal amplification circuit. Therefore the signal with the amplitude of 400 m $V_{P-P}$ up to $V_{DD}$+0.3 V can be input to this LSI chip. However, in the case of coaxial cable or optical module input the application will change as the sample application circuit shown later.
- Connect to the unused input pin to the GND or $V_{DD}$.

(2) The relationship between the OUTMODE pin and the two output data formats is shown in the table below.

| | | |
|---|---|---|
| OUTMODE pin | H | 20-bit LSB first data output format |
| | L | 16-bit MSB first data output format |

- IF an error is detected in an input data, that input data is not output. Instead, the previous data will be output.
- The data output is synchronized with falling edge of the bit clock.
- IF the PLL is in the Lock state, the 384 Fs or 256 Fs clock that is synchronized with the output data will be output. Note that the duty is of the 256 Fs clock is 'H:L = 2:1'. It is not 'H:L = 1:1'.

### Sub Codes

The sub code output consists of the copy inhibit signal, emphasis mode signal, sampling frequency signal, validity flag signal and user's bit. The table below details these sub code outputs.

| | |
|---|---|
| COPY inhibit signal | COPY pin level = high:Copy not inhibited.<br>COPY pin level = low:Copy inhibited. |
| Emphasis mode signal | EMPHA pin level = high:Emphasis mode.<br>EMPHA pin level = low:Non emphasis mode. |
| Sampling frequency | BSA pin level = high:32 kHz sampling frequency<br>CD pin level = high:44.1 kHz sampling frequency<br>BSB pin level = high:48 kHz sampling frequency |
| Validity flag signal | This signal is output from the V pin in sub frame unit. |
| User's bit | This signal is output from the U pin in sub frame unit. |

### Clock Modes

The control clock is specified by the VCO. The VCO has two modes: self oscillation mode and PLL mode as shown below.

| | | |
|---|---|---|
| Self oscillation mode | • XMODE pin level=low | • The VCO continues its oscillation according to the VIN pin potential. BCLK, LRCK, and FS256 clocks are not effective. |
| | • No data input | • The VCO continues its oscillation according to the VIN pin potential. FS384, BCLK, LRCK, and FS256 clocks output. |
| PLL mode | • Data input with the XMODE pin level=high | • The PLL block and the entire circuit are in the normal operation state. |

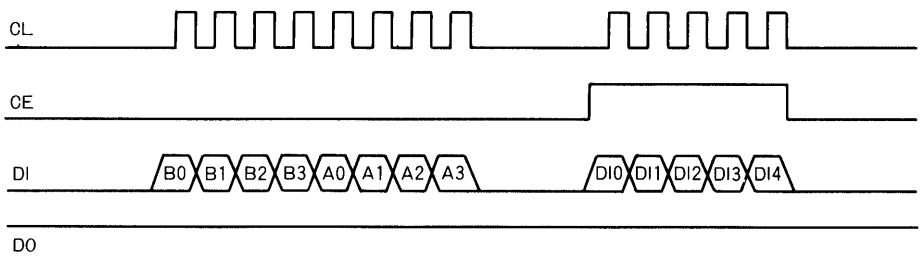
- When the STOP pin is changed to the high level, the PLL functional circuit block stops its operation and the entire circuit operation is then forced to stop. The entire circuit will start the normal operation again when the STOP pin is changed to the low level.
- If the LOCK operation is not activated in a certain fixed time period after the PLL enters the lock-up state:
  Reinitialize the PLL functional circuit block to active the lock-up mode. This should be done to prevent the PLL lock error.

## Microcontroller Interface

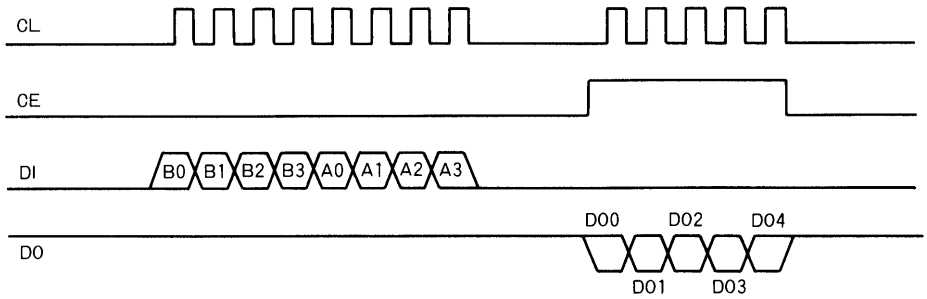
The microcontroller interface function can be used by setting the MODE pin level to high. In this function mode, the pins CE, CL, DI and DO can be used to allow the interface between the LSI chip and a microcontroller. This microcontroller interface allows the microcontroller to control and process the input pin selection output data format, copy information and sampling frequency output.

Set the mode CE, CL, and DI pins to the low when the microcontroller interface is not used.

### Input data format




### Output data format




Bits B0 to A3 of the DI signal in the format figures on the preceding page are used to specify an 8-bit address. These 8-bits are used to specify the addresses both in the input and output operations.

| | B0 | B1 | B2 | B3 | A0 | A1 | A2 | A3 |
|---|---|---|---|---|---|---|---|---|
| Data input mode | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| Data output mode | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

(1) Data input mode

Bits DI0 to DI4 of the DI signal are used to select the operation modes shown in the tables below.

| | |
|---|---|
| DI1 = L | 16-bit data MSB first output mode |
| DI1 = H | 20-bit data LSB first output mode |

| DI2 | DI3 | input pin selection | DOUT |
|---|---|---|---|
| L | L | DIN1 | DIN1 data output |
| L | H | DIN2 | DIN2 data output |
| H | L | DIN3 | DIN3 data output |
| H | H | DIN4 | low level signal output (fixed level output) |

- When the MODE pin level is set to high, the input pins and output data format are selected by the microcontroller. This means that the selection data input to the SEL1, SEL2 and OUTMODE pins has no significance.

  Just after the XMODE pin is changed to high from low, DI0 to DI4 are set to low.

(2) Data output mode

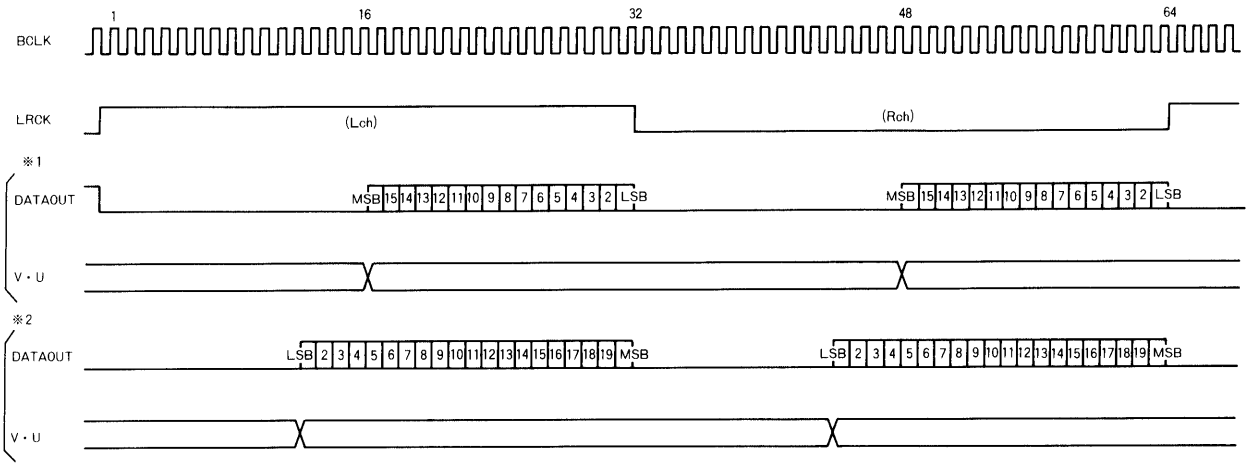
Bits DO0 to DO4 of the DO signal have the following meanings show in the tables below.

| | |
|---|---|
| DO3 = L | Copy inhibited |
| DO3 = H | Copy not inhibited |

| DO1 | DO2 | Sampling frequency selection |
|---|---|---|
| L | L | 44.1 kHz |
| L | H | 48 kHz |
| H | H | 32 kHz |

- 6 ms or longer is required to read data after the ERROR pin is changed to L. Take at least 6 ms between data read out. Any codes when DO1 is high and DO2 is low is invalid in other conditions than this.

## Timing Chart




∗1: This operation timing is based on the following conditions: OUTMODE pin level=low and DI1 bit=low
∗2: This operation timing is based on the following conditions: OUTMODE pin level=high and DI1 bit=high
V = Validity flag output. U=User's bit output.

## LOCK and ERROR Pins

Descriptions of LOCK and ERROR pins are as follows.

LOCK: Preamble detector. When two or more preambles are detected successively, this pin outputs high level signal. When XMODE pin is low or STOP pin is high or no signal input, outputs low level signal.

ERROR: When two or more preambles are not detected successively, or 8 subframes' continuous results of parity check are not accomplished, this pin outputs high level signal to indicate system error. When XMODE pin is low or STOP pin is high or no signal input, outputs high level signal.

1. Output pin conditions when error occurs.

| Output pin | XMODE is low | STOP is low | Parity error | No input signal |
|---|---|---|---|---|
| DATAOUT<br>V<br>U | Keeps the indeterminate condition of high or low. | Keeps the value just before the STOP goes to high. | Outputs preceding data. | Outputs the indeterminate data. *1 |
| CD, BSA<br>BSB, COPY<br>EMPHA | Outputs low level signal. | Outputs low level signal. | Outputs low level signal after reset. | Outputs the indeterminate data. *1 |
| DOUT | No effect by error. | No effect by error. | No effect by error. | No effect by error. |

Note 1: When input pin goes to no input signal, errors can be caused due to the timing of turning into no input signal. Take the same operation as parity error in this case.
2: When error occurring, the outputs pin's change synchronizes the timing of ERROR pin's turning into the high level. When XMODE pin is set to low or STOP pin is to high, ERROR pin goes to high at the same time and the other output pins will change as in the table above.

2. Error signals and read out timing

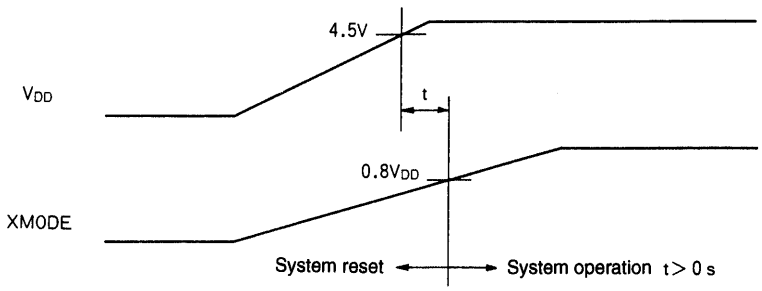
After the ERROR pin goes to low, each data will be able to be accessed after the next clock pulse.

| | |
|---|---|
| DATAOUT, V, U | Accessible as soon as ERROR pin goes to low |
| CD, BSA, BSB, COPY, EMPHA | Accessible 6 ms or later after ERROR pin goes to low |

## XMODE Pin

XMODE pin resets the system. This pin must be turned into high after 4.5 V or more power is applied to start the system normally. By setting XMODE pin to low, VCO self oscillation frequency from FS384 pin will reset the internal circuit.

### Power rise diagram

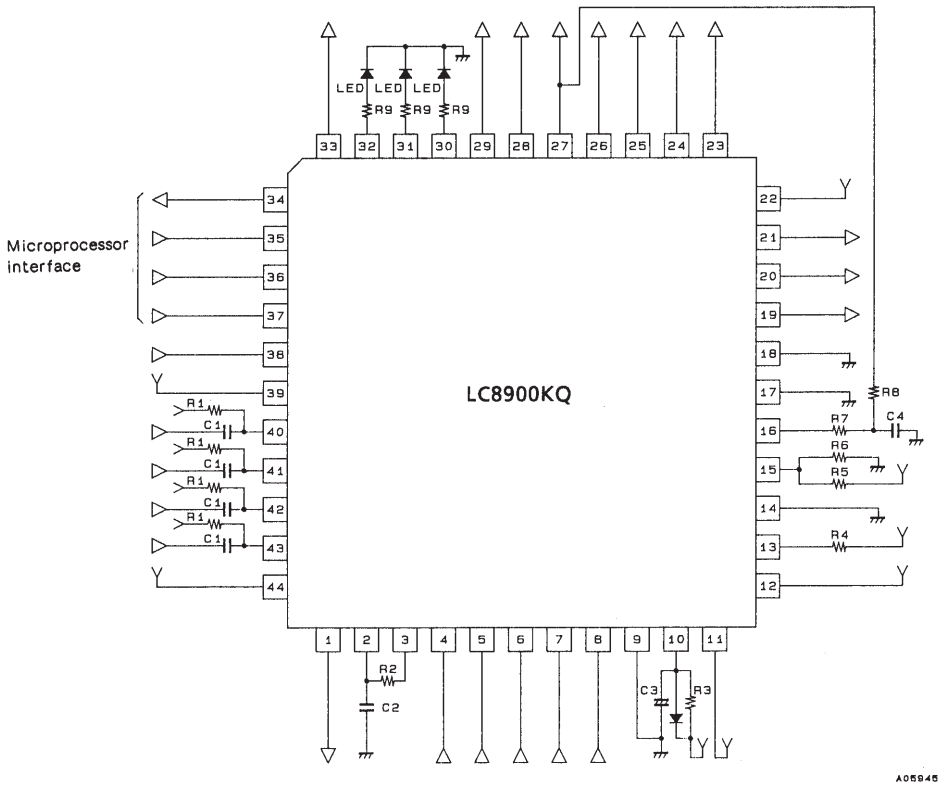



Each input pin will be accessible after XMODE turns to be on to start the system.

Microcontroller interface pins will be accessible after XMODE turns to be on to start the system.

Each data output pin will be accessible after XMODE turns to be on and ERROR pin goes to low. COPY, EMPHA, CD, BSA, and BSB cords will be accessible at least 6 ms later after ERROR pin goes to low.

## Sample Application Circuit




∗ Apply the power to $AV_{DD}$ and two $DV_{DD}$s simultaneously, or a latch up will occur.
∗ The allowable current to BSA, CD, and BSB pins is 8 mA.

## Recommended External Components

| Component type | Component code | Value |
|---|---|---|
| Resistor | R1 | 330 kΩ* |
| | R2 | 33 kΩ |
| | R3 | 10 kΩ |
| | R4 | 24 kΩ |
| | R5 | 5.1 kΩ |
| | R6 | 5.1 kΩ |
| | R7 | 150 Ω |
| | R8 | 180 kΩ |
| | R9 | 330 Ω |
| Capacitor | C1 | 0.1 µF |
| | C2 | 1000 pF |
| | C3 | 10 µF to 100 µF |
| | C4 | 0.01 µF |

*: This is a value when coaxial cables are connected to the input pins. Take C1 and replace R1 with a 56 kΩ resistor if optical cables are connected instead of coaxial cables.

## Connection to an Optical Module