HN62344B Series

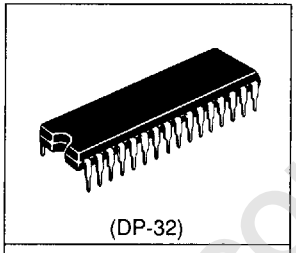
4M (512K x 8-bit) Mask ROM

■ DESCRIPTION

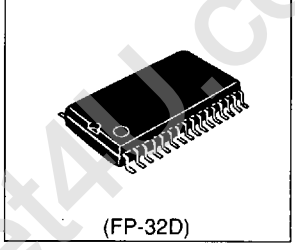
The Hitachi HN62344B is a 4-Megabit CMOS Mask Programmable Read Only Memory organized as 524,288 x 8-bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition, the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

Hitachi's HN62344B is offered with JEDEC-Standard Byte-Wide EPROM pinouts in 32-pin Plastic DIP and 32-lead Plastic SOP packages. This allows socket replacement with EPROMs and Flash Memory.



(DP-32)



(FP-32D)

■ FEATURES

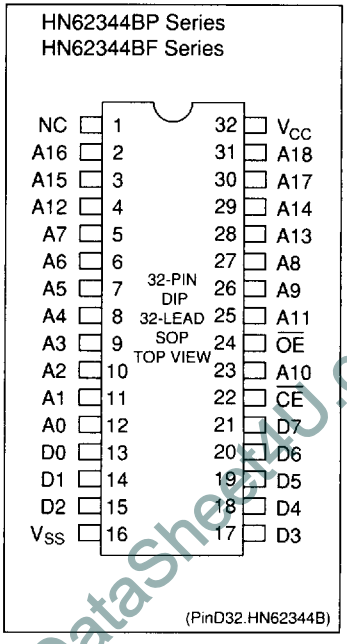
- Single Power Supply:
  V_{CC} = 5 V ± 5%
- High Speed Access Time:
  100 ns (max)
- Low Power Consumption:
  Active Current: 150 mW (typ)
  Standby Current: 5 µW (typ)
- Byte-Wide Data Organization
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Byte-Wide EPROM
  EPROM and Flash Memory Compatible
- Packages:
  32-pin Plastic DIP
  32-lead Plastic SOP

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62344BP-10	100 ns	32-pin Plastic DIP (DP-32)
HN62344BF-10	100 ns	32-lead Plastic SOP (FP-32D)

■ PIN ARRANGEMENT

HN62344BP Series
HN62344BF Series

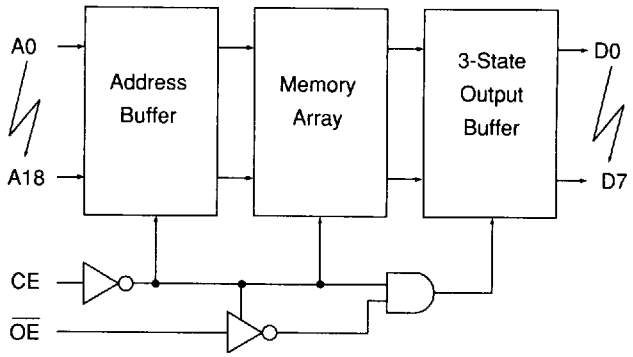


(PinD32.HN62344B)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{18}	Address
D_0 - D_7	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



(BD.HN62344B)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. With respect to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	15	pF
Output Capacitance [1]	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 5%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	10	µA	$\overline{CE}$ = 2.4 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	60	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = min.
Standby V_{CC} Current	I_{SB1}	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ - 0.2V
	I_{SB2}		3	mA	V_{CC} = 5.5 V, $\overline{CE} \geq$ 2.4V
Input Voltage	V_{IH}	2.4	V_{CC}+0.3	V	
	V_{IL}	-0.3	0.45	V	
Output Voltage	V_{OH}	2.4	-	V	I_{OH} = -205 µA
	V_{OL}	-	0.4	V	I_{OL} = 1.6 mA

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 5%, V_{SS} = 0 V, T_a = 0 to 70°C)

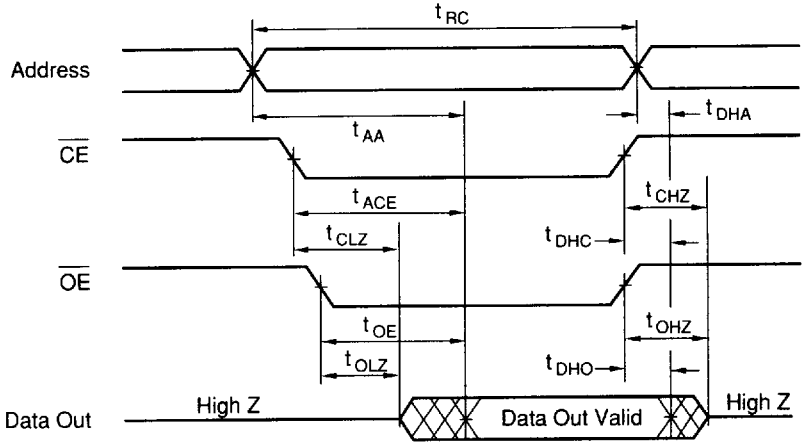
Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	Min.	Max.	Unit
Read Cycle Time	t_{RC}	100	-	ns
Address Access Time	t_{AA}	-	100	ns
Chip Enable Access Time	t_{ACE}	-	100	ns
Output Enable Access Time	t_{OE}	-	55	ns
Output Hold Time from Address Change	t_{DHA}	0	-	ns
Output Hold Time from Chip Enable	t_{DHC}	0	-	ns
Output Hold Time from Output Enable	t_{DHO}	0	-	ns
Chip Enable to Output in High Z	t_{CHZ} [1]	-	40	ns
Output Enable to Output in High Z	t_{OHZ} [1]	-	40	ns
Chip Enable to Output in Low Z	t_{CLZ}	5	-	ns
Output Enable to Output in Low Z	t_{OLZ}	5	-	ns

Note: 1. t_{CHZ}, and t_{OHZ} define the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ READ TIMING WAVEFORM



(TD.R.HN62344B)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.