FAIRCHILD

SEMICONDUCTOR®

74AC14 • 74ACT14
Hex Inverter with Schmitt Trigger Input

General Description

The 74AC14 and 74ACT14 contain six inverter gates each with a Schmitt trigger input. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

The 74AC14 and 74ACT14 have hysteresis between the positive-going and negative-going input thresholds (typically 1.0V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

Features

■ I_{CC} reduced by 50%
■ Outputs source/sink 24 mA
■ 74ACT14 has TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Package Description
74AC14SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC14SCX_NL (Note 1)	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC14SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC14MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC14MTCX_NL (Note 1)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC14PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT14SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ACT14MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT14MTCX_NL (Note 1)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT14PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Note 1: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

FACT™ is a trademark of Fairchild Semiconductor Corporation.

74AC14 • 74ACT14

Logic Symbol

IEEE/IEC

I_0 — $\overline{O}_0$
I_1 — $\overline{O}_1$
I_2 — $\overline{O}_2$
I_3 — $\overline{O}_3$
I_4 — $\overline{O}_4$
I_5 — $\overline{O}_5$

Pin Descriptions

Pin Names	Description
I_n	Inputs
$\overline{O}_n$	Outputs
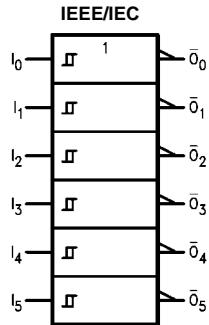
Connection Diagram

I_0 — 1 — 14 — V_{CC}
$\overline{O}_0$ — 2 — 13 — I_5
I_1 — 3 — 12 — $\overline{O}_5$
$\overline{O}_1$ — 4 — 11 — I_4
I_2 — 5 — 10 — $\overline{O}_4$
$\overline{O}_2$ — 6 — 9 — I_3
GND — 7 — 8 — $\overline{O}_3$
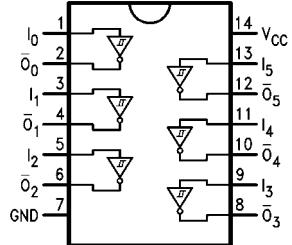
Function Table

Input	Output
A	**$\overline{O}$**
L	H
H	L

Absolute Maximum Ratings(Note 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = −0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = −0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to $V_{CC} + 0.5V$
DC Output Source	
or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C

Note 2: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Typ	$T_A = −40°C$ to $+85°C$ Guaranteed Limits		Units	Conditions
V_{OH}	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9		$I_{OUT} = −50$ μA
		4.5	4.49	4.4	4.4	V	
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46		$I_{OH} = 12$
		4.5		3.86	3.76	V	$I_{OH} = 24$ mA
		5.5		4.86	4.76		$I_{OH} = 24$ mA (Note 3)
V_{OL}	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1		$I_{OUT} = 50$ μA
		4.5	0.001	0.1	0.1	V	
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44		$I_{OL} = 12$
		4.5		0.36	0.44	V	I_{OL} 24 mA
		5.5		0.36	0.44		$I_{OL} = 24$ mA (Note 3)
I_{IN} (Note 5)	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	$V_I = V_{CC}$, GND
V_{t+}	Maximum Positive Threshold	3.0		2.2	2.2		$T_A =$ Worst Case
		4.5		3.2	3.2	V	
		5.5		3.9	3.9		
$V_{t−}$	Minimum Negative Threshold	3.0		0.5	0.5		$T_A =$ Worst Case
		4.5		0.9	0.9	V	
		5.5		1.1	1.1		
$V_{H(MAX)}$	Maximum Hysteresis	3.0		1.2	1.2		$T_A =$ Worst Case
		4.5		1.4	1.4	V	
		5.5		1.6	1.6		
$V_{H(MIN)}$	Minimum Hysteresis	3.0		0.3	0.3		$T_A =$ Worst Case
		4.5		0.4	0.4	V	
		5.5		0.5	0.5		
I_{OLD}	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}	Output Current (Note 4)	5.5			−75	mA	$V_{OHD} = 3.85V$ Min
I_{CC} (Note 5)	Maximum Quiescent Supply Current	5.5		2.0	20.0	μA	$V_{IN} = V_{CC}$ or GND

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

AC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V) (Note 6)	$T_A = +25°C$ $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	3.3	1.5	9.5	13.5	1.5	15.0	ns
		5.0	1.5	7.0	10.0	1.5	11.0	
t_{PHL}	Propagation Delay	3.3	1.5	7.5	11.5	1.5	13.0	ns
		5.0	1.5	6.0	8.5	1.5	9.5	

Note 6: Voltage Range 3.3 is 3.3V ± 0.3V

Voltage Range 5.0 is 5.0V ± 0.5V

DC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Typ	$T_A = -40°C$ to $+85°C$ Guaranteed Limits	Units	Conditions
V_{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0 | 2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	2.0 | 2.0		
V_{IL}	Maximum LOW Level Output Voltage	4.5	1.5	0.8 | 0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	0.8 | 0.8		
V_{OH}	Minimum HIGH Level Output Voltage	4.5	4.49	434 | 4.4	V	$I_{OUT} = -50\mu A$
		5.5	5.49	5.4 | 5.4		
		4.5		3.86 | 3.76	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24$ mA
		5.5		4.86 | 4.76		$I_{OH} = -24$ mA (Note 7)
V_{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1 | 0.1	V	$I_{OUT} = 50\ \mu A$
		5.5	0.001	0.1 | 0.1		
		4.5		0.36 | 0.44	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 24$ mA
		5.5		0.36 | 0.44		$I_{OL} = 24$ mA (Note 7)
I_{IN}	Maximum Input Leakage Current	5.5	±0.1	±1.0	μA	$V_I = V_{CC}$, GND
$V_{H(MAX)}$	Maximum Hysteresis	4.5		1.4 | 1.4	V	$T_A =$ Worst Case
		5.5		1.6 | 1.6		
$V_{H(MIN)}$	Minimum Hysteresis	4.5		0.4 | 0.4	V	$T_A =$ Worst Case
		5.5		0.5 | 0.5		
V_{t+}	Maximum Positive Threshold	4.5		2.0 | 2.0	V	$T_A =$ Worst Case
		5.5		2.0 | 2.0		
V_{t-}	Minimum Negative Threshold	4.5		0.8 | 0.8	V	$T_A =$ Worst Case
		5.5		0.8 | 0.8		
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6	1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	Minimum Dynamic	5.5		75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}	Output Current (Note 8)	5.5		−75	mA	$V_{OHD} = 3.85V$ Min
I_{CC}	Maximum Quiescent Supply Current	5.5		2.0 | 20.0	μA	$V_{IN} = V_{CC}$ or GND

Note 7: All outputs loaded; thresholds on input associated with output under test.

Note 8: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for ACT

Symbol	Parameter	V_CC (V) (Note 9)	T_A = +25°C C_L = 50 pF			T_A = −40°C to +85°C C_L = 50 pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay Data to Output	5.0	3.0	8.0	10.0	3.0	11.0	ns
t_{PHL}	Propagation Delay Data to Output	5.0	3.0	8.0	10.0	3.0	11.0	ns

Note 9: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance for AC for ACT	25.0 80	pF	V_{CC} = 5.0V

**Physical Dimensions** inches (millimeters) unless otherwise noted

0.335 − 0.344
(8.509 − 8.738)

14 13 12 11 10 9 8

0.228 − 0.244
(5.791 − 6.198)

LEAD NO. 1
IDENT

1 2 3 4 5 6 7

30°
TYP

0.010
(0.254) MAX

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) × 45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008
(0.203) TYP

0.014 − 0.020
(0.356 − 0.508) TYP

M14A (REV H)
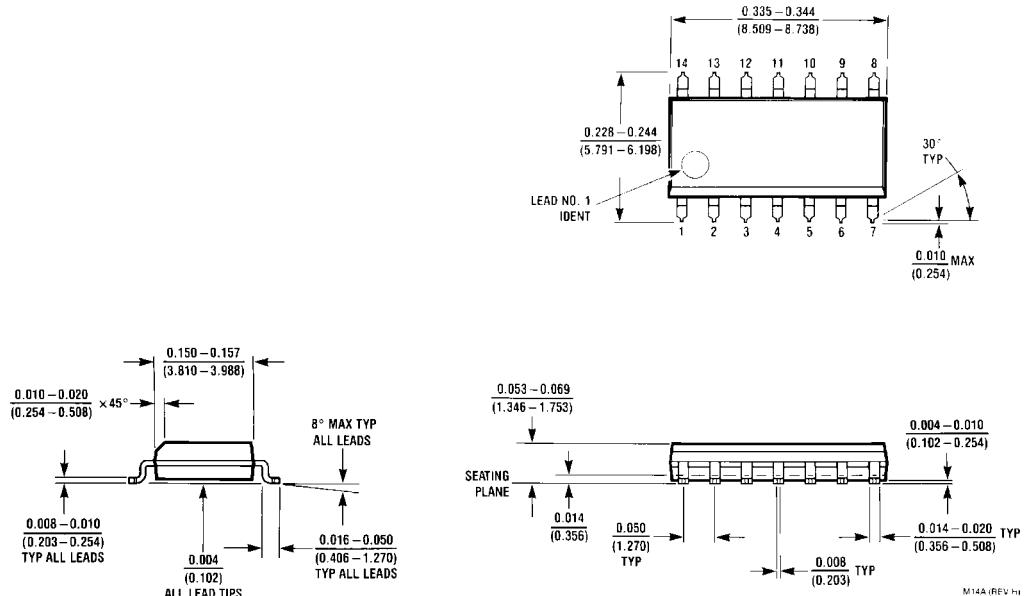
14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

10.2±0.1

-A-

1.1 TYP

14   8

7.8

5.3±0.1

-B-

3.9

0.2 C B A
ALL LEAD TIPS

PIN #1 IDENT.

1   7

LAND PATTERN RECOMMENDATION

14   13   9   8

5.01 TYP

9.27 TYP

(2.13 TYP)

1   2   6   7

1.27 TYP   0.6 TYP

ALL LEAD TIPS

2.1 MAX.

0.1 C

1.8±0.1

-C-

0.15±0.05

1.27 TYP

0.35-0.51

0.12 M C A

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.15-0.25

7° TYP

GAGE PLANE

0.25

0°-8° TYP

0.60±0.15

SEATING PLANE

1.25
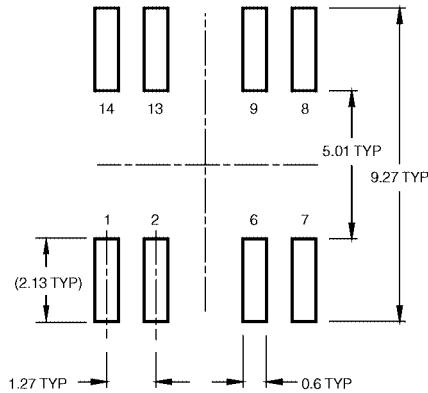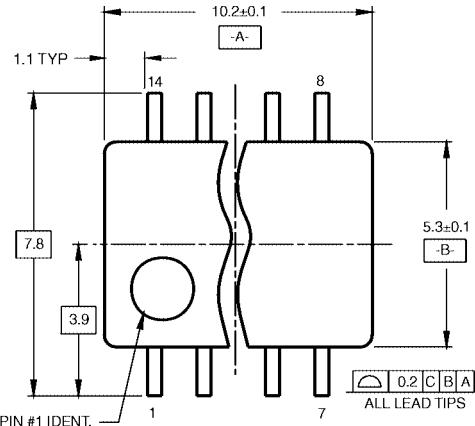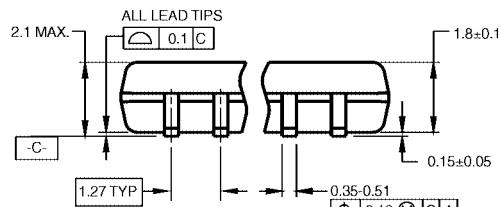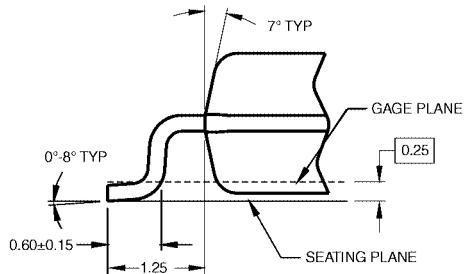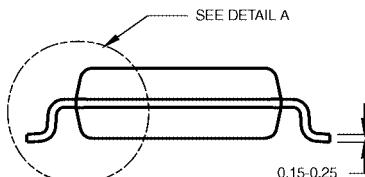
DETAIL A

NOTES:
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION,
   ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
   FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

5.0±0.1
-A-

0.43 TYP

14   8

6.4

3.2

4.4±0.1
-B-

1

7

PIN #1 IDENT.

0.2 C B A
ALL LEAD TIPS

7.72

4.16

1.78

0.65   0.42

LAND PATTERN RECOMMENDATION

1.2 MAX

ALL LEAD TIPS
0.1 C

0.90 +0.15 -0.10

-C-

0.65

0.19 - 0.30

0.10±0.05

0.13 M   A   B S   C S

SEE DETAIL A

0.09-0.20

12.00° TOP & BOTTOM

R0.09 min

GAGE PLANE

0.25

0°-8°

0.6±0.1

1.00

R0.09 min

SEATING PLANE

DETAIL A
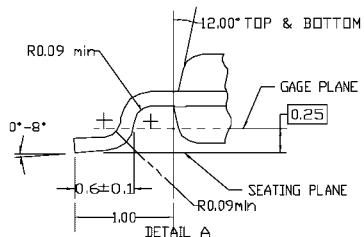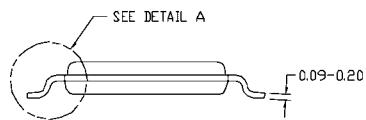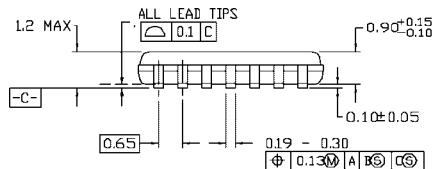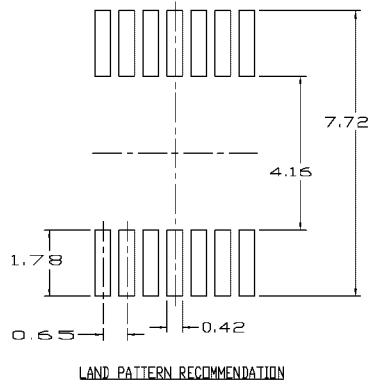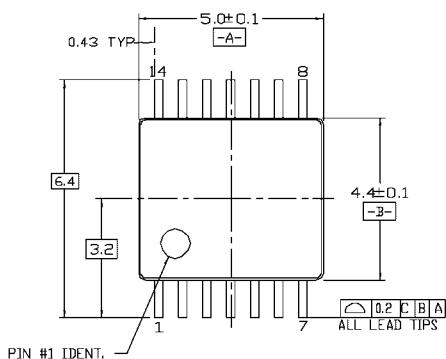
NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14 rev D

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)
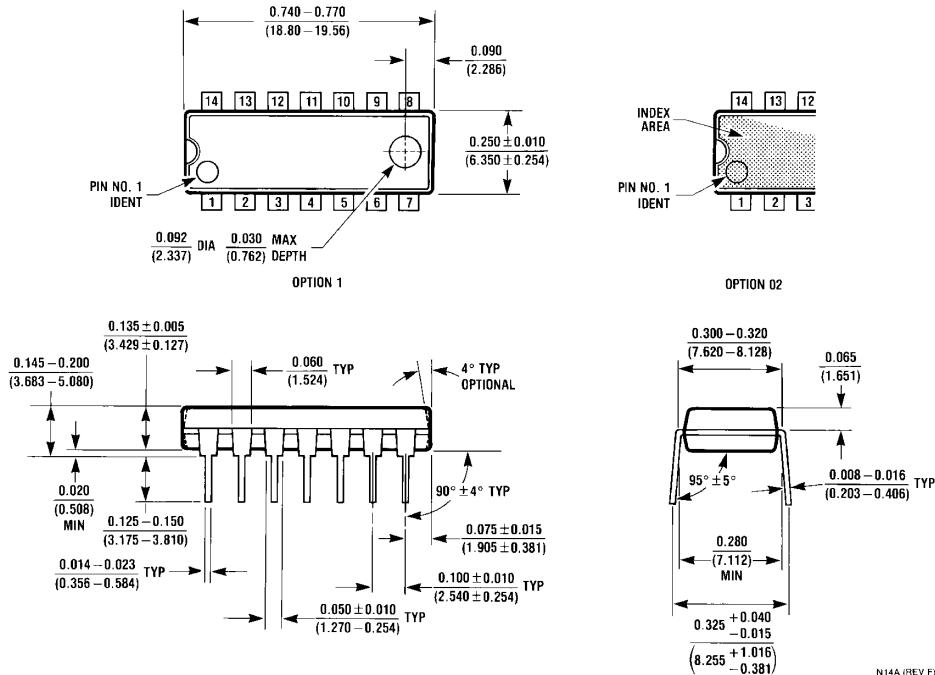
14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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