PRELIMINARY
Note : This is not a final specification
Some parametric limits are subject to change.

M5M51R16AWG -10L, -12L, -15L, -10H, -12H, -15H

1048576-BIT(65536-WORD BY 16-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M51R16AWG is a 1048576-bit CMOS static RAM organized as 65536 words by 16-bits, which are fabricated using high-performance CMOS technology. The use of CMOS cells and periphery results in a high density and low power static RAM.

The M5M51R16AWG can achieve low stand-by current and low operation current and ideal for the battery back-up application.

The M5M51R16AWG is packaged in a 48-pin chip scale package which is a high reliability and high density surface mount device (SMD). Using this type of devices, it becomes very easy to design a small system.

The M5M51R16AWG is fully compatible with the M5M51R16WG.

FEATURE

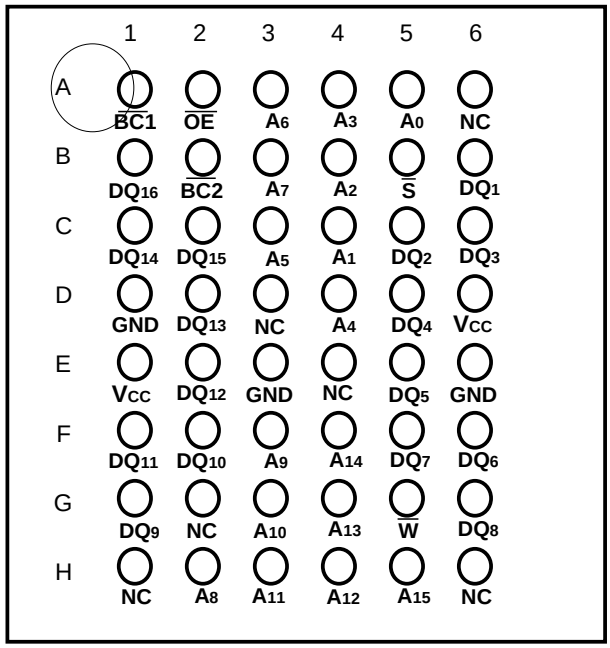
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M51R16AWG- 10L M5M51R16AWG- 12L M5M51R16AWG- 15L	100ns 120ns 150ns	10mA (1MHz)	4µA
M5M51R16AWG- 10H M5M51R16AWG- 12H M5M51R16AWG- 15H	100ns 120ns 150ns		2µA

- Single +1.8V~2.7V power supply
- Low power down current 0.05µA(typ.)
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by $\overline{S}$,$\overline{BC}$1 and $\overline{BC}$2
- Data hold on +1.0V power supply
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Separate control of lower and upper bytes by $\overline{BC}$1 and $\overline{BC}$2
- Package
  48-pin chip scale package(CSP)
  Ball pitch : 0.75mm
  Package size: 7.0mm x 8.5mm

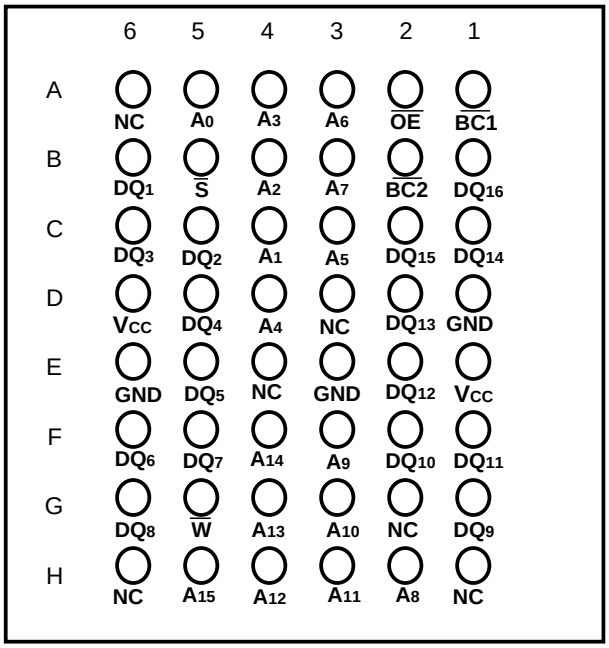
APPLICATION

Small capacity memory units.

PIN CONFIGURATION (TOP VIEW)



PIN CONFIGURATION (BOTTOM VIEW)



Outline 48FJA

NC : NO CONNECTION

FUNCTION

The operation mode of the M5M51R16A series are determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$, $\overline{OE}$, $\overline{BC1}$ and $\overline{BC2}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{BC1}$ and/or $\overline{BC2}$ and the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{BC1}$, $\overline{BC2}$ or $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{BC1}$ and/or $\overline{BC2}$ and $\overline{S}$ are in an active state. ($\overline{BC1}$ and/or $\overline{BC2}$=L, $\overline{S}$=L)

When setting $\overline{BC1}$ at a high level and the other pins are in an active state, upper-Byte are in a selectable mode in which both reading and writing are enabled, and lower -Byte are in a non-selectable mode. And when setting $\overline{BC2}$ at a high level and the other pins are in an active state, lower-Byte are in a selectable mode in which both reading and writing are enabled, and upper -Byte are in a non-selectable mode.

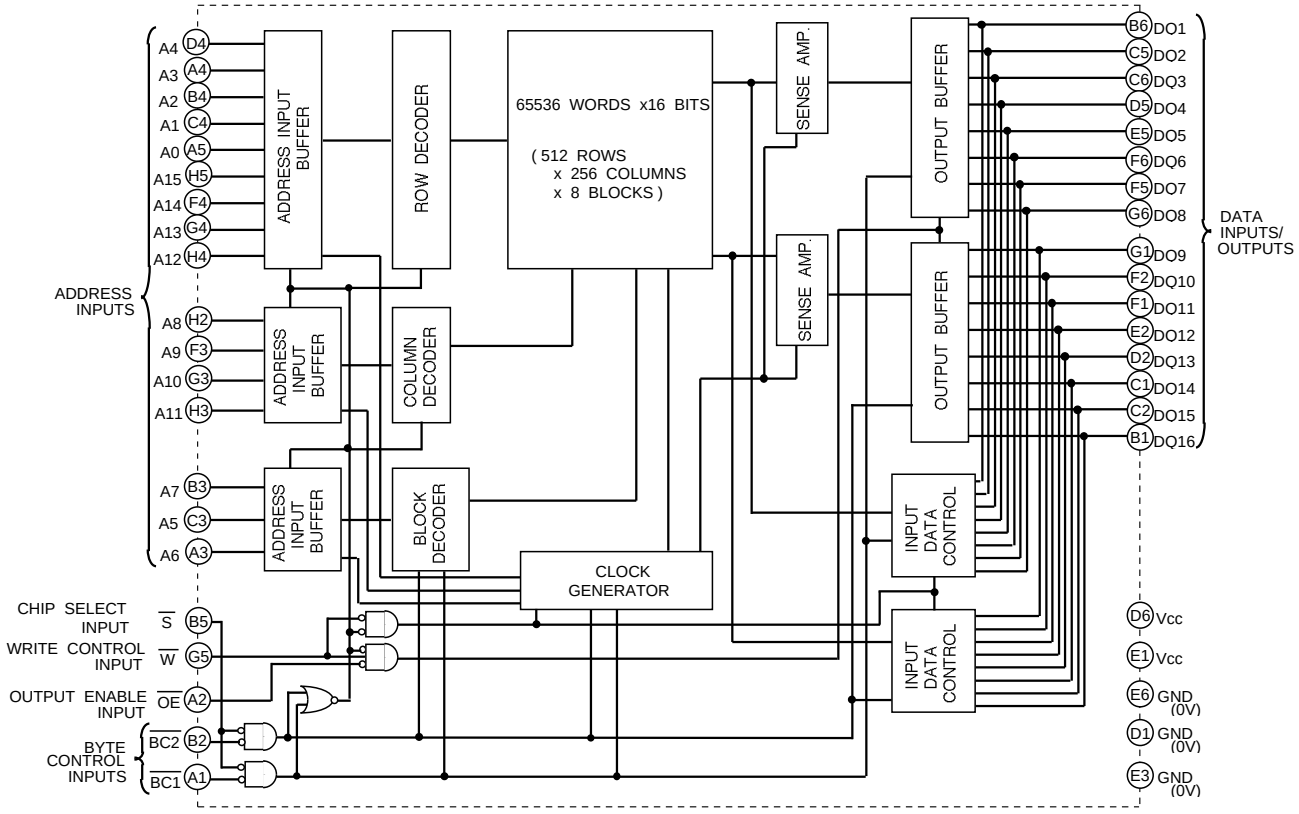
When setting $\overline{BC1}$ and $\overline{BC2}$ at a high level or $\overline{S}$ at a high level, the chips are in a non-selectable mode in which both reading and writing are disabled.
In this mode, the output stage is in a high-impedance state, allowing OR -tie with other chips and memory expansion by $\overline{BC1}$, $\overline{BC2}$ and $\overline{S}$. $\overline{S}$, $\overline{BC1}$ and $\overline{BC2}$ control the power down feature. When $\overline{S}$, $\overline{BC1}$ and $\overline{BC2}$ go high, the power supply current is reduced as low as the stand-by current which is specified as Icc3 or Icc4, and the memory data can be held at +1.0V power supply, enabling battery back-up operation during power-failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	$\overline{BC1}$	$\overline{BC2}$	Mode	DQ1~8	DQ9~16	Icc
L	H	L	L	L	Word Read	Dout	Dout	Active
L	H	L	H	L	Upper-Byte Read (Lower-Byte Non selection)	High-Z	Dout	Active
L	H	L	L	H	Lower-Byte Read (Upper-Byte Non selection)	Dout	High-Z	Active
L	L	X	L	L	Word Write	Din	Din	Active
L	L	X	H	L	Upper-Byte Write (Lower-Byte Non selection)	High-Z	Din	Active
L	L	X	L	H	Lower-Byte Write (Upper-Byte Non selection)	Din	High-Z	Active
L	H	H	X	X	Output disable	High-Z	High-Z	Active
X	X	X	H	H	Non selection	High-Z	High-Z	Stand-by
H	X	X	X	X	Non selection	High-Z	High-Z	Stand-by

(High-Z=High-impedance)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to GND	-0.2 ~ 4.6	V
V_I	Input voltage		-0.2* ~ Vcc+0.2(max.4.6V)	V
Vo	Output voltage		0 ~ Vcc	V
Pd	Power dissipation	Ta=25°C	1	W
Topr	Operating temperature		0 ~ 70	°C
Tstg	Storage temperature		-65 ~150	°C

* -1.0V in case of AC (Pulse width ≤ 30ns)

DC ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, Vcc = 1.8V~2.7V, unless otherwise noted)

Symbol	Parameter	Conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			0.7 x Vcc		Vcc+0.2V	V
V_{IL}	Low-level input voltage			-0.2*		0.4	V
V_{OH}	High-level output voltage	I_{OH} = -0.1mA		1.6			V
V_{OL}	Low-level output voltage	I_{OL} = 0.1mA				0.2	V
I_I	Input current	V_I =0 ~Vcc				±1	µA
Io	Output current in off-state	$\overline{BC1}$ and $\overline{BC2}$ = V_{IH} or $\overline{S}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0~ Vcc				±1	µA
I_{CC1W}	Word operation(16bit) Active supply current (AC,TTL level)	$\overline{BC1}$ and $\overline{BC2}$ = V_{IL}, $\overline{S}$ = V_{IL} other inputs = V_{IH} or V_{IL} Output-open(duty 100%)	Min cycle		15	25	mA
I_{CC2W}			1MHz		7	10	mA
I_{CC1B}	Byte operation(8bit) Active supply current (AC,TTL level)	($\overline{BC1}$ = V_{IH} and $\overline{BC2}$ = V_{IL}) or ($\overline{BC1}$ = V_{IL} and $\overline{BC2}$ = V_{IH}) , $\overline{S}$ = V_{IL} ,other inputs = V_{IH} or V_{IL} Output-open(duty 100%)	Min cycle		10	15	mA
I_{CC2B}			1MHz		5	8	mA
I_{CC3}	Stand-by current	1) $\overline{S}$≥Vcc-0.2V, other inputs = 0~Vcc	-L			4	µA
		2) $\overline{BC1}$ and $\overline{BC2}$ ≥Vcc-0.2V,$\overline{S}$≤0.2V, other inputs = 0~Vcc	-H			2	µA
I_{CC4}	Stand-by current	$\overline{BC1}$ and $\overline{BC2}$ = V_{IH} or $\overline{S}$ = V_{IH}, other inputs = 0~Vcc				0.3	mA

* -1.0V in case of AC (Pulse width ≤ 30ns)

CAPACITANCE (Ta = 0 ~ 70°C, Vcc = 1.8V~2.7V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
C_I	Input capacitance	V_I=GND, V_i=25mVrms, f=1MHz			6	pF
C_O	Output capacitance	V_O=GND, V_o=25mVrms, f=1MHz			10	pF

Note 1: Direction for current flowing into an IC is positive (no mark).

Note 2: Typical value is Vcc = 2.0V, Ta = 25°C

Note 3: C_I,C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, Vcc = 1.8V~2.7V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level • • • • • • • V_{IH} = 0.7 x Vcc + 0.2V, V_{IL} = 0.2V
Input rise and fall time • • • • 5ns
Reference level • • • • • • • • V_{OH} = 0.9V, V_{OL} = 0.9V
Output loads • • • • • • • • • Fig.1,C_L = 30pF
C_L = 5pF (for ten, tdis)

Transition is measured ±200mV from steady state voltage. (for ten, tdis)

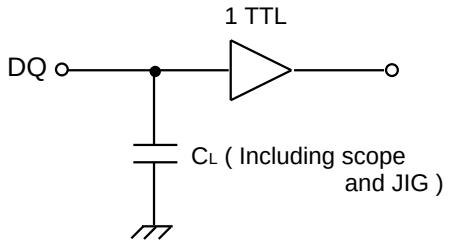


Fig.1 Output load

(2)READ CYCLE

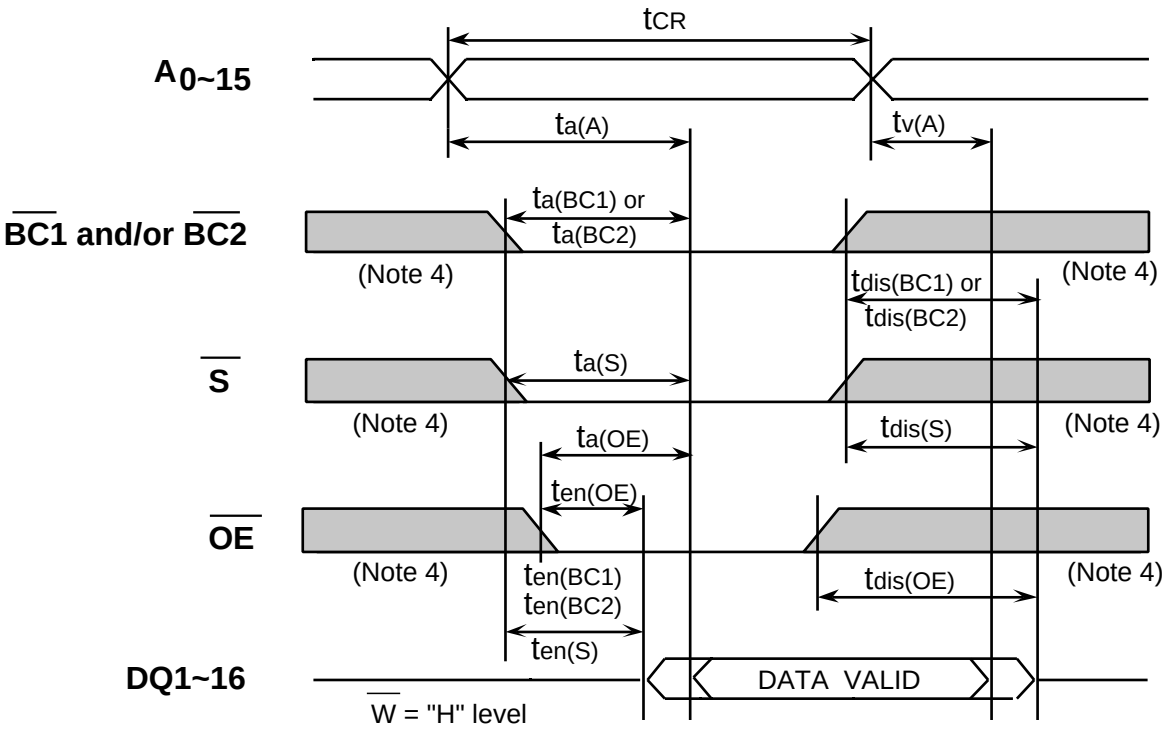
Symbol	Parameter	Limits						Unit
		-10L,-10H		-12L,-12H		-15L,-15H		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	100		120		150		ns
ta(A)	Address access time		100		120		150	ns
ta(S)	Chip select access time		100		120		150	ns
ta(BC1)	$\overline{BC}$1 access time		100		120		150	ns
ta(BC2)	$\overline{BC}$2 access time		100		120		150	ns
ta(OE)	Output enable access time		50		60		75	ns
tdis(S)	Output disable time after $\overline{S}$ high		35		40		50	ns
tdis(BC1)	Output disable time after $\overline{BC}$1 high		35		40		50	ns
tdis(BC2)	Output disable time after $\overline{BC}$2 high		35		40		50	ns
tdis(OE)	Output disable time after $\overline{OE}$ high		35		40		50	ns
ten(S)	Output enable time after $\overline{S}$ low	10		10		10		ns
ten(BC1)	Output enable time after $\overline{BC}$1 low	10		10		10		ns
ten(BC2)	Output enable time after $\overline{BC}$2 low	10		10		10		ns
ten(OE)	Output enable time after $\overline{OE}$ low	5		5		5		ns
t_V(A)	Data valid time after address change	10		10		10		ns

(3)WRITE CYCLE

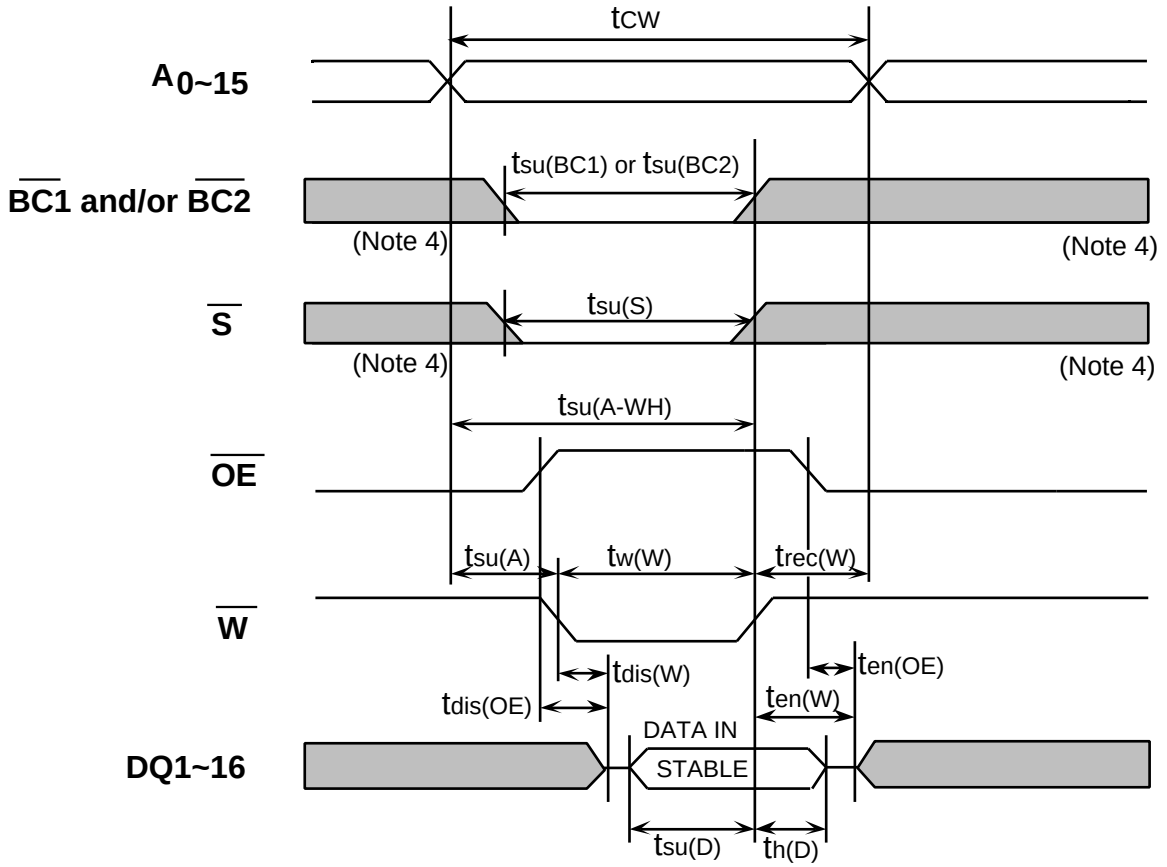
Symbol	Parameter	Limits						Unit
		-10L,-10H		-12L,-12H		-15L,-15H		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	100		120		150		ns
tw(W)	Write pulse width	75		85		100		ns
tsu(A)	Address set up time	0		0		0		ns
tsu(A-WH)	Address set up time with respect to $\overline{W}$	85		100		120		ns
tsu(BC1)	$\overline{BC}$1 setup time	85		100		120		ns
tsu(BC2)	$\overline{BC}$2 setup time	85		100		120		ns
tsu(S)	Chip select set up time	85		100		120		ns
tsu(D)	Data set up time	50		55		60		ns
th(D)	Data hold time	0		0		0		ns
trec(W)	Write recovery time	0		0		0		ns
tdis(W)	Output disable time after $\overline{W}$ low		35		40		50	ns
tdis(OE)	Output disable time after $\overline{OE}$ high		35		40		50	ns
ten(W)	Output enable time after $\overline{W}$ high	5		5		5		ns
ten(OE)	Output enable time after $\overline{OE}$ low	5		5		5		ns
ten(BC1)	Output enable time after $\overline{BC}$1 low	10		10		10		ns
ten(BC2)	Output enable time after $\overline{BC}$2 low	10		10		10		ns

(4) TIMING DIAGRAMS

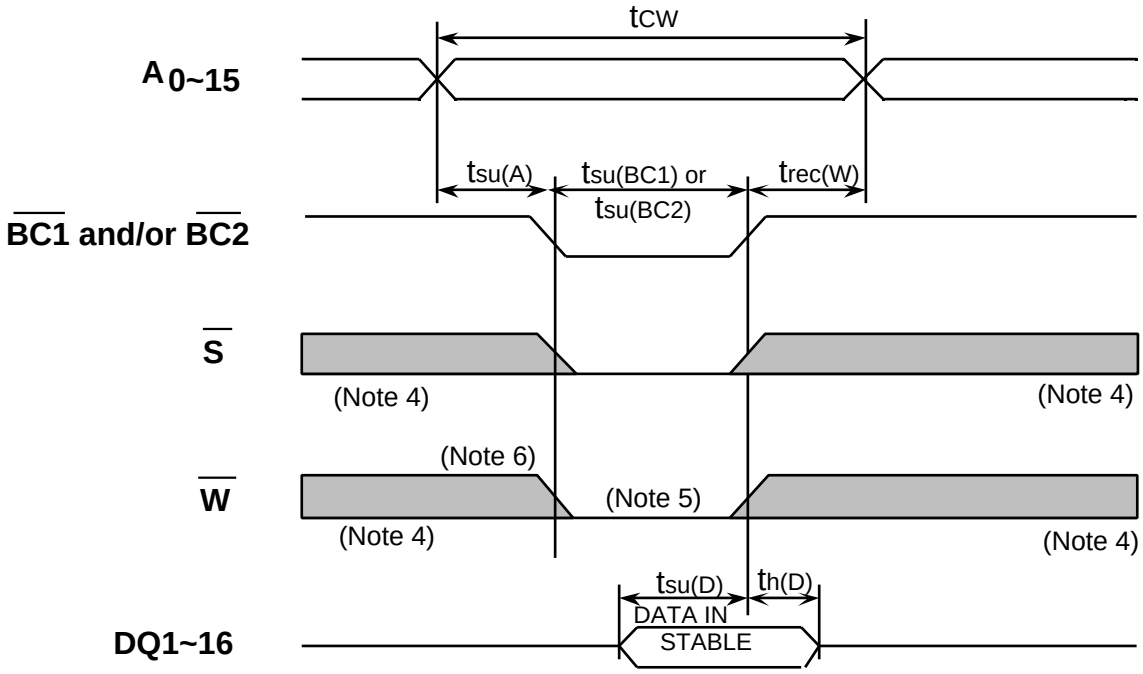
Read cycle



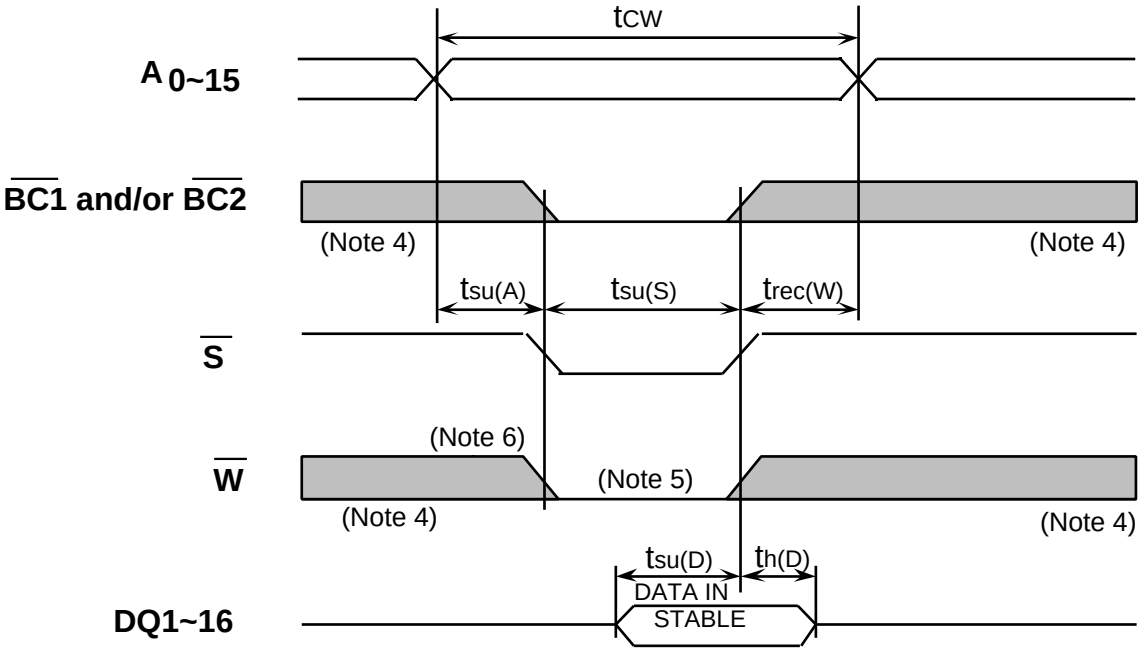
Write cycle ($\overline{W}$ control mode)



Write cycle ($\overline{BC}$1, $\overline{BC}$2 control mode)



Write cycle ($\overline{S}$ control mode)



Note 4: Hatching indicates the state is "don't care".

Note 5: Writing is executed while $\overline{S}$ low overlaps $\overline{BC}$1 and/or $\overline{BC}$2 low and $\overline{W}$ low.

Note 6: When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{BC}$1 and/or $\overline{BC}$2 or falling edge of $\overline{S}$, the outputs are maintained in the high impedance state.

Note 7:Don't apply inverted phase signal externally when DQ pin is output mode.

Note 8:ten,tdis are periodically sampled and are not 100% tested.

Note 9:tCR(Read cycle time) is defined as whole time from reading address set up to this address change under read mode set condition by $\overline{S}$,$\overline{W}$,$\overline{OE}$,$\overline{BC}$1 and/or $\overline{BC}$2.

Note 10:tCW(Write cycle time) is defined as whole time from writing address set up to this address change under write mode set condition by $\overline{S}$,$\overline{W}$,$\overline{BC}$1 and/or $\overline{BC}$2.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, unless otherwise noted)

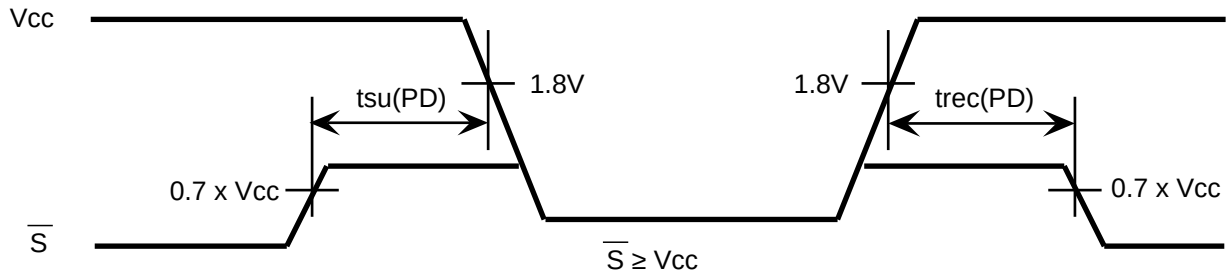
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{cc(PD)}$	Power down supply voltage			1.0			V
$V_{I(S)}$	Chip select input $\overline{S}$	1.8V ≤ Vcc(PD)		0.7 x Vcc			V
		1.0V ≤ Vcc(PD) ≤ 1.8V			$V_{cc(PD)}$		
$V_{I(BC)}$	Byte control inputs $\overline{BC1}$ and $\overline{BC2}$	1.8V ≤ Vcc(PD)		0.7 x Vcc			V
		1.0V ≤ Vcc(PD) ≤ 1.8V			$V_{cc(PD)}$		
$I_{CC(PD)}$	Power down supply current	Vcc = 2.0V 1) $\overline{S}$ ≥ Vcc - 0.2V other inputs = 0~Vcc 2) $\overline{BC1}$ and $\overline{BC2}$ ≥ Vcc - 0.2V $\overline{S}$ ≤ 0.2V,other inputs = 0~Vcc	-L			2	µA
			-H		0.05	1	

(2) TIMING REQUIREMENTS (Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
tsu(PD)	Power down set up time		0			ns
trec(PD)	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$\overline{S}$ control mode



$\overline{BC1}$ and $\overline{BC2}$ control mode