128Kx24 Asynchronous SRAM, 5V

FEATURES

- 128Kx24 bit CMOS Static
- Random Access Memory Array
  - Fast Access Times: 12 and 15ns
  - Master Output Enable and Write Control
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- Surface Mount Package
  - 119 Lead BGA (JEDEC MO-163), No. 391
  - Small Footprint, 14mm x 22mm
  - Multiple Ground Pins for Maximum Noise Immunity
- Single +5V (±10%) Supply Operation
- DSP Memory Solution
  - Motorola DSP5600x™
  - Analog Devices SHARC™

DESCRIPTION

The EDI8L24128CxxBC is a 5V, three megabit SRAM constructed with three 128Kx8 die mounted on a multi-layer laminate substrate. With 12 to 15ns access times, x24 width and a 5V operating voltage, the EDI8L2418C is ideal for creating a single chip memory solution for the Motorola DSP5600x or a two chip solution for the Analog Devices SHARC™ DSP.

The single or dual chip memory solutions offer improved system performance by reducing the length of board traces and the number of board connections compared to using multiple monolithic devices. For example, the capacitance load on the data lines for the BGA package is 58% less than a monolithic SOJ solution.

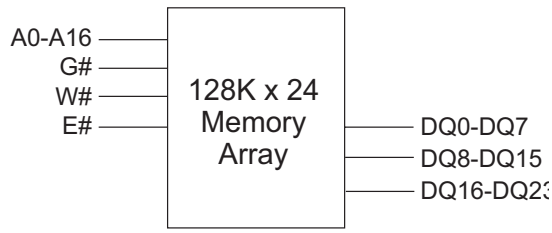
The JEDEC Standard 119 lead BGA provides a 44% space savings over using 128Kx8, 300mm wide SOJs and the BGA package has a height of 100mm compared to 148mm for the SOJ packages.

FIG. 1 PIN CONFIGURATION

	1	2	3	4	5	6	7
A	NC	A_0	A_1	A_2	A_3	A_4	NC
B	NC	A_5	A_6	E	A_7	A_8	NC
C	DQ_{12}	NC	NC	NC	NC	NC	DQ_0
D	DQ_{13}	V_{CC}	GND	GND	GND	V_{CC}	DQ_1
E	DQ_{14}	GND	V_{CC}	GND	V_{CC}	GND	DQ_2
F	DQ_{15}	V_{CC}	GND	GND	GND	V_{CC}	DQ_3
G	DQ_{16}	GND	V_{CC}	GND	V_{CC}	GND	DQ_4
H	DQ_{17}	V_{CC}	GND	GND	GND	V_{CC}	DQ_5
I	NC	GND	V_{CC}	GND	V_{CC}	GND	NC
J	DQ_{18}	V_{CC}	GND	GND	GND	V_{CC}	DQ_6
K	DQ_{19}	GND	V_{CC}	GND	V_{CC}	GND	DQ_7
L	DQ_{20}	V_{CC}	GND	GND	GND	V_{CC}	DQ_8
M	DQ_{21}	GND	V_{CC}	GND	V_{CC}	GND	DQ_9
N	DQ_{22}	V_{CC}	GND	GND	GND	V_{CC}	DQ_{10}
O	DQ_{23}	NC	NC	NC	NC	NC	DQ_{11}
P	NC	A_9	A_{10}	W	A_{11}	A_{12}	NC
Q	NC	A_{13}	A_{14}	G	A_{15}	A_{16}	NC

Pin DESCRIPTION

A0-16	Address Inputs
E#	Chip Enables
W#	Master Write Enable
G3	Master Output Enable
DQ0-23	Common Data
	Input/Output
V_{CC}	Power (+5V±10%)
GND	Ground
NC	No Connection



Absolute Maximum Ratings*

Voltage on any pin relative to V_{SS}	-0.5V to 7.0V
Operating Temperature T_S (Ambient) Commercial Industrial	 0°C to + 70°C -40°C to +85°C
Storage Temperature	-55°C to +125°C
Power Dissipation	3 Watts
Output Current.	20 mA
Junction Temperature, T_J	175°C

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.3	—	+0.8	V

Capacitance

(f=1.0MHZ, V_{IN}=V_{CC} OR V_{SS})

Parameter	Symbol	Max	Unit
Address Lines	C_L	8	pf
Data Lines	$C_{D/Q}$	10	pf
Write & Output Enable Line	W#, G#	8	pf
Chip Enable Lines	E#	8	pf

Truth Table

E#	W#	G#	Mode	Output	Power
H	X	X	Standby	High Z	I_{CC2}, I_{CC3}
L	H	H	Output Deselect	High Z	I_{CC1}
L	H	L	Read	Data Out	I_{CC1}
L	L	X	Write	Data In	I_{CC1}

DC Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C)

Parameter	Symbol		Conditions	Min	Type	Max	Units
Operating Power Supply Current	I_{CC1}	W# = V_{IL}, $I_{I/O}$ = 0mA, Min Cycle		200	270	mA	
Standby (TTL) Power Supply Current	I_{CC2}	E# ≥ V_{IH}, V_{IN} ≥ V_{IL} or V_{IN} ≥ V_{IH}, f = 0MHz			45	mA	
Full Standby Power CMOS	I_{CC3}	E# ≥ V_{CC} -0.2V				10	mA
Supply Current		V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≥ 0.2V					
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}	—	—	±10	µA	
Output Leakage Current	I_{LO}	$V_{I/O}$ 0V to V_{CC}		—	—	±10	µA
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		—	—	0.4	V

AC Test Conditions

Fig. 1

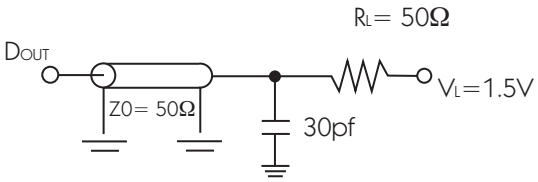
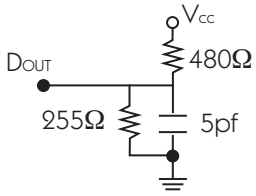


Fig. 2



Input Pulse Levels	V_{SS} to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

Note: For t_{EHQZ}, t_{GHQZ} and t_{WLQZ}, CL = 5pF Figure 2

AC Characteristics Read Cycle

Parameter	Symbol		12ns		15ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	12		15		ns
Address Access Time	t_{AVQV}	t_{AA}		12		15	ns
Chip Enable Access Time	t_{ELQV}	t_{ACS}		12		15	ns
Chip Enable to Output in Low Z[1]	t_{ELQX}	t_{CLZ}	3		3		ns
Chip Disable to Output in High Z[1]	t_{EHQZ}	t_{CHZ}		6		7	ns
Output Hold from Address Change	t_{AVQX}	t_{OH}	3		3		ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		6		7	ns
Output Enable to Output in Low Z[1]	t_{GLQX}	t_{OLZ}	0		0		ns
Output Disable to Output in High Z[1]	t_{GHQZ}	t_{OHZ}		6		7	ns

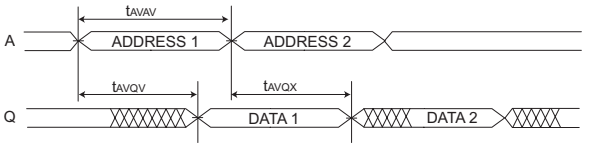
1. This parameter is guaranteed by design but not tested.

AC Characteristics Write Cycle

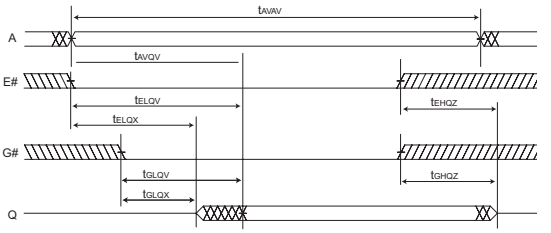
Parameter	Symbol		12ns		15ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	12		15		ns
Chip Enable to End of Write	t_{ELWH} t_{ELEH}	t_{CW} t_{CW}	9 9		9 9		ns ns
Address Setup Time	t_{AVWL} t_{AVEL}	t_{AS} t_{AS}	0 0		0 0		ns ns
Address Valid to End of Write	t_{AVWH} t_{AVEH}	t_{AW} t_{AW}	9 9		10 10		ns ns
Write Pulse Width	t_{WLWH} t_{ELEH}	t_{WP} t_{WP}	10 10		11 11		ns ns
Write Recovery Time	t_{WHAX} t_{EHAX}	t_{WR} t_{WR}	0 0		0 0		ns ns
Data Hold Time	t_{WHDX} t_{EHDX}	t_{DH} t_{DH}	0 0		0 0		ns ns
Write to Output in High Z[1]	t_{WLQZ}	t_{WHZ}	0	6	0	7	ns
Data to Write Time	t_{DVWH} t_{DVEH}	t_{DW} t_{DW}	6 6		7 7		ns ns
Output Active from End of Write[1]	t_{WHQX}	t_{WLZ}	3		3		ns

1. This parameter is guaranteed by design but not tested.

FIG. 2
TIMING WAVEFORM — READ CYCLE



Read Cycle 1 (W# High; G, E Low)



Read Cycle 2 (W# High)

FIG. 3
WRITE CYCLE — W# CONTROLLED

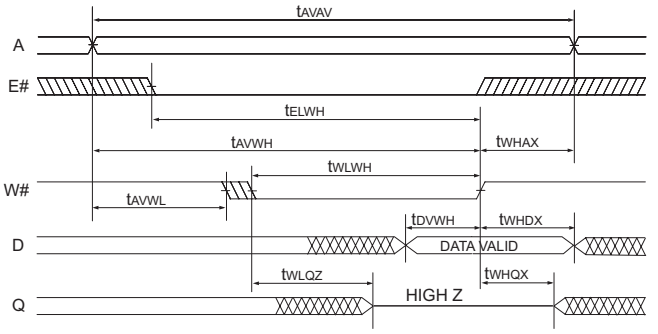
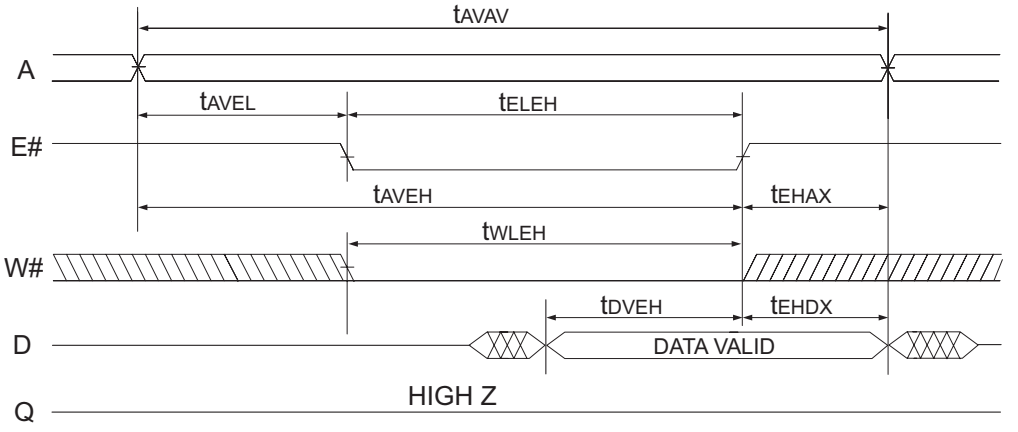
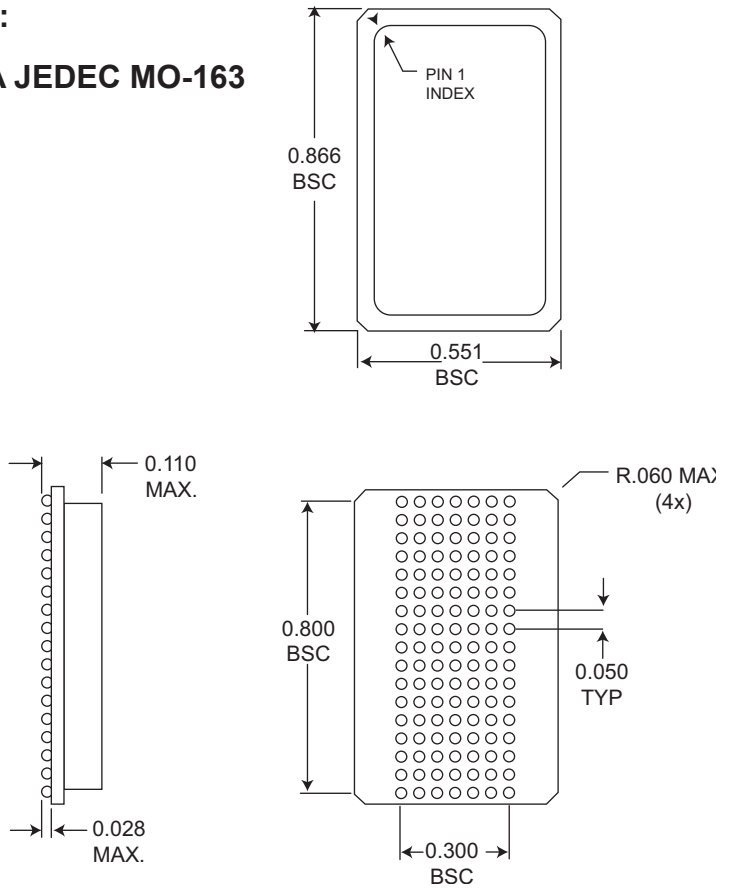


FIG. 4
WRITE CYCLE — E# CONTROLLED



PACKAGE 391:

119 LEAD BGA JEDEC MO-163



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

Commercial (0°C to +70°C)

Part Number	Speed (ns)	Package No.
EDI8L24128C12BC	12	391
EDI8L24128C15BC	15	391

Industrial (-40°C to +85°C)

Part Number	Speed (ns)	Package No.
EDI8L24128C12BI	12	391
EDI8L24128C15BI	15	391