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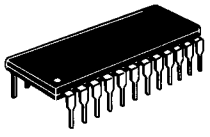
MCCS146818B
MCCS156818B

Advance Information

Real Time Clock plus SRAM
Real Time Clock plus SRAM Module
CMOS

MCCS146818BP
MCCS156818BP

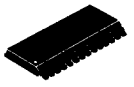


P SUFFIX
PLASTIC
CASE 709

MCCS146818BFN

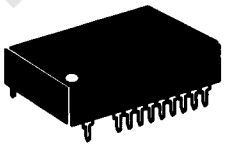
FN SUFFIX
PLASTIC
CASE 776

MCCS156818BDW



DW SUFFIX
SOG
CASE 751F

MCCS146818BM
MCCS146818B1M
MCCS156818BM
MCCS156818B1M



M SUFFIX
MODULE
CASE 905

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SECTION 1
INTRODUCTION

The MCCS146818B and MCCS156818B Real-Time Clock family, referred to in this document as the 18B, is compatible with the DS1285/1287/1287A line. The MCCS146818BM/B1M and MCCS156818BM/B1M devices include a crystal and lithium cell battery encapsulated into a module.

These devices include the unique MOTEL concept for use with both Motorola and Intel microprocessor timing cycles. These devices combine five important features: 1) a complete time-of-day clock with alarm and a one hundred year calendar, 2) a programmable interrupt for alarm and timing functions, 3) a square wave generation circuit, 4) 114 bytes of ultra low power SRAM, and 5) the modules need no external parts. The MCCS146818B family interfaces with 1-MHz processor buses and the MCCS156818B family with 2-MHz processor buses, while consuming very little power, allowing the module battery to last a long period of time.

The real time clock plus SRAM has two distinct uses. First, it is a CMOS part that includes all the common battery backed-up functions such as SRAM, time, and calendar. Second, the devices may be used with a CMOS microprocessor to relieve the processor of the timekeeping workload, and to extend the available SRAM of the MPU. In addition the module includes a 32.768-kHz crystal and lithium cell encapsulated into the module.

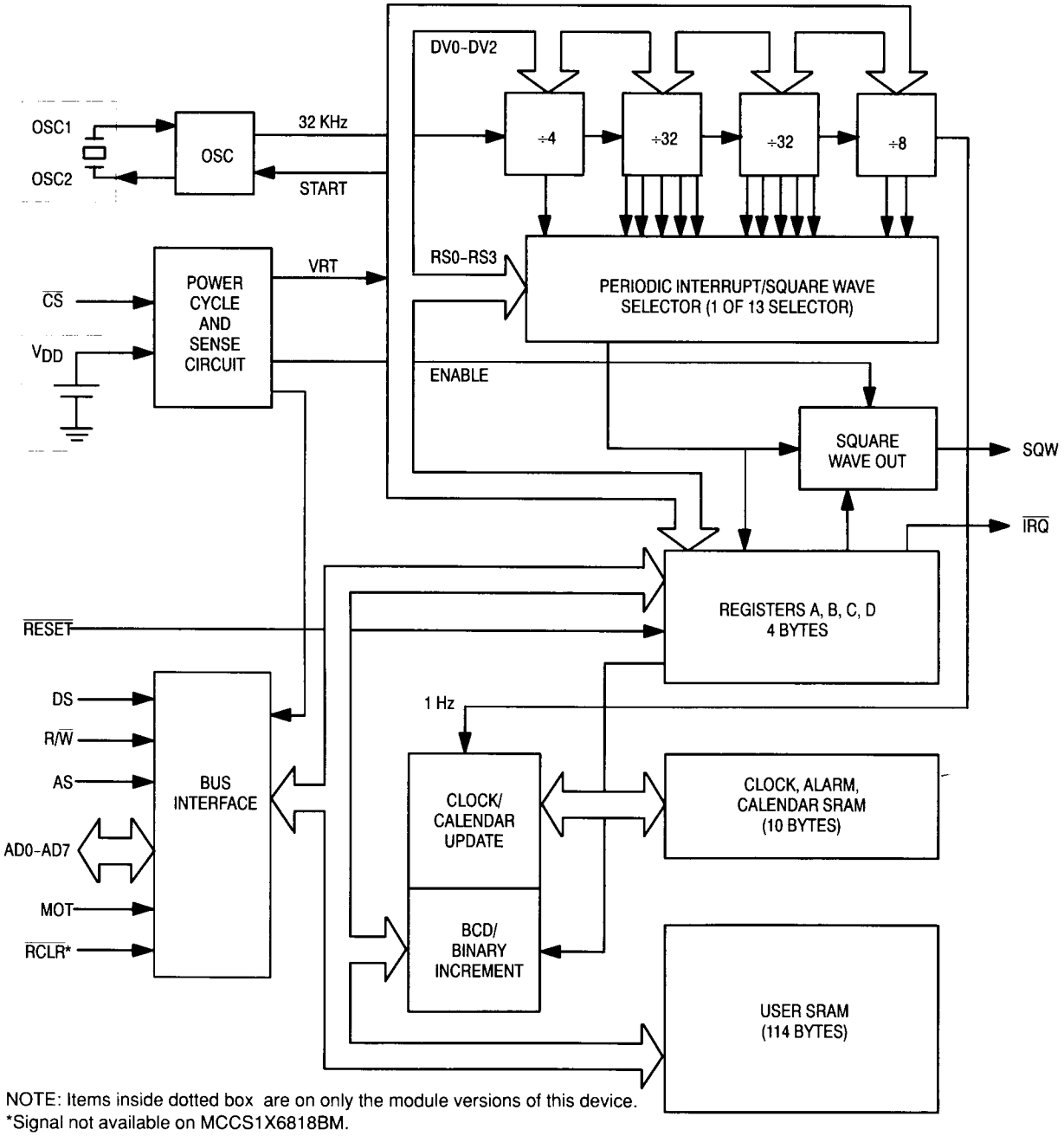
The only difference between the two RTCMs is that the 18B1M is able to erase (set to $FF) all of the built-in general-purpose SRAM by momentarily grounding the $\overline{RCLR}$, while the device is in standby mode. This feature is not available on the 18BM.

General Features

- Pin compatible with DS1285
- Counts seconds, minutes, hours, days, day of the week, date of month and year with leap year compensation
- Binary or BCD data representation
- 12/24 hour mode
- Daylight savings time option
- Multiplexed bus for pin efficiency
- Interfaced with software as 128 bytes of SRAM
  - 14 bytes of clock and control registers
  - 114 bytes of general-purpose SRAM
- Programmable square wave signal
- Three interrupts are separately software maskable and testable
  - Time-of-day alarm
  - Timed interrupt, once per second to once per day
  - End of clock update cycle
- Operating temperature range 0 to 70°C
- Digital inputs/outputs are TTL, NMOS, and CMOS compatible
- Application information included in Section 6.0

Module Features

- Ultra long battery life (see Section 6.2 Item 3)
- Drop-in replacement for IBM PC/AT computer clock calendar (BM only)
- Pin for pin compatible with DS1287A/DS1287
- 18B1M equipped with SRAM clear function
- No external parts required
- 1 minute per month accuracy at room temperature



NOTE: Items inside dotted box are on only the module versions of this device.
*Signal not available on MCCS1X6818BM.

Figure 1.1. Block Diagram

SECTION 2
ELECTRICAL CHARACTERISTICS

2.1 MAXIMUM RATINGS (Voltage referenced to V_{SS}, see Note 1)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	5.5	V
All Input Voltages Except OSC1	V_{in}	− 0.5 to V_{DD} + 0.5	V
Current Drain per Pin Excluding V_{DD} and V_{SS}	I_{in}	± 15	mA
Storage Temperature 18B 18B1M/18BM	T_{stg}	− 65 to + 150 0 to + 70	°C

NOTES:
1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics table or pin descriptions section.
2. These devices contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

2.2 THERMAL CHARACTERISTICS

Characteristic	Package	Symbol	Value	Unit
Thermal Resistances	PDIP	$R_{\theta JA}$	66	°C/W
		$R_{\theta JC}$	20	
	PQCC	$R_{\theta JA}$	100	°C/W
		$R_{\theta JC}$	23	
	SOG	$R_{\theta JA}$	TBD	°C/W
		$R_{\theta JC}$	TBD	
	Module	$R_{\theta JA}$	TBD	°C/W
		$R_{\theta JC}$	TBD	

TBD = To be determined.

2.3 DC ELECTRICAL CHARACTERISTICS

(V_{BATT} = 3.0 V, V_{DD} = 0 V, T_A = 25°C, Stand-by Mode)

Characteristics	Symbol	Guaranteed Limits				Unit
		MCCS146818B		MCCS156818B		
		Min	Max	Min	Max	
Range of Operation (see Figure 3.2 for BP and BFN) Input Ignored, Outputs Three-Stated, Oscillator Enabled	f_{osc}	32.76750	32.76850	32.76750	32.76850	kHz
V_{BATT} Standby Current	I_{BATT}	—	700	—	500	nA

2.4 DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 4.75 to 5.25 V, T_A = 0 to 70°C, Voltages Referenced to V_{SS})

Characteristics	Test Conditions	Symbol	Guaranteed Limits				Unit
			MCCS146818B		MCCS156818B		
			Min	Max	Min	Max	
Output Voltage (AD0–AD7, SQW)	I_{OH} = I_{OL} < 10 µA	V_{OL} V_{OH}	— V_{DD} – 0.1	0.1 —	— V_{DD} – 0.1	0.1 —	V
Output High Voltage (see Note 1)	I_{OH} = 1.0 mA	V_{OH}	2.4	—	2.4	—	V
Output Low Voltage	I_{OL} = 4.0 mA, All Outputs	V_{OL}	—	0.4	—	0.4	V
Input High Voltage (AD0–AD7, DS, MOT, AS, R/$\overline{W}$, $\overline{CS}$, $\overline{RESET}$)		V_{IH}	2.2	V_{DD} + 0.3	2.2	V_{DD} + 0.3	V
Input Low Voltage (AD0–AD7, DS, R/$\overline{W}$, $\overline{CS}$, MOT, $\overline{RESET}$, AS)		V_{IL}	– 0.3	+ 0.8	– 0.3	+ 0.8	V
All Other Inputs (Input Pulldown) (see Note 2)		I_{in}	—	1.0	—	1.0	µA
Three-State Leakage	$V_{SS} \le V_{out} \le V_{DD}$	I_{OZ}	—	+ 10	—	+ 10	µA
Open Drain Leakage			—	± 10	—	± 10	nA
Power Supply Current	Bus Idle XTAL on Pins 2 and 3 Squarewave Out Disabled	I_{DD}	—	10	—	10	mA

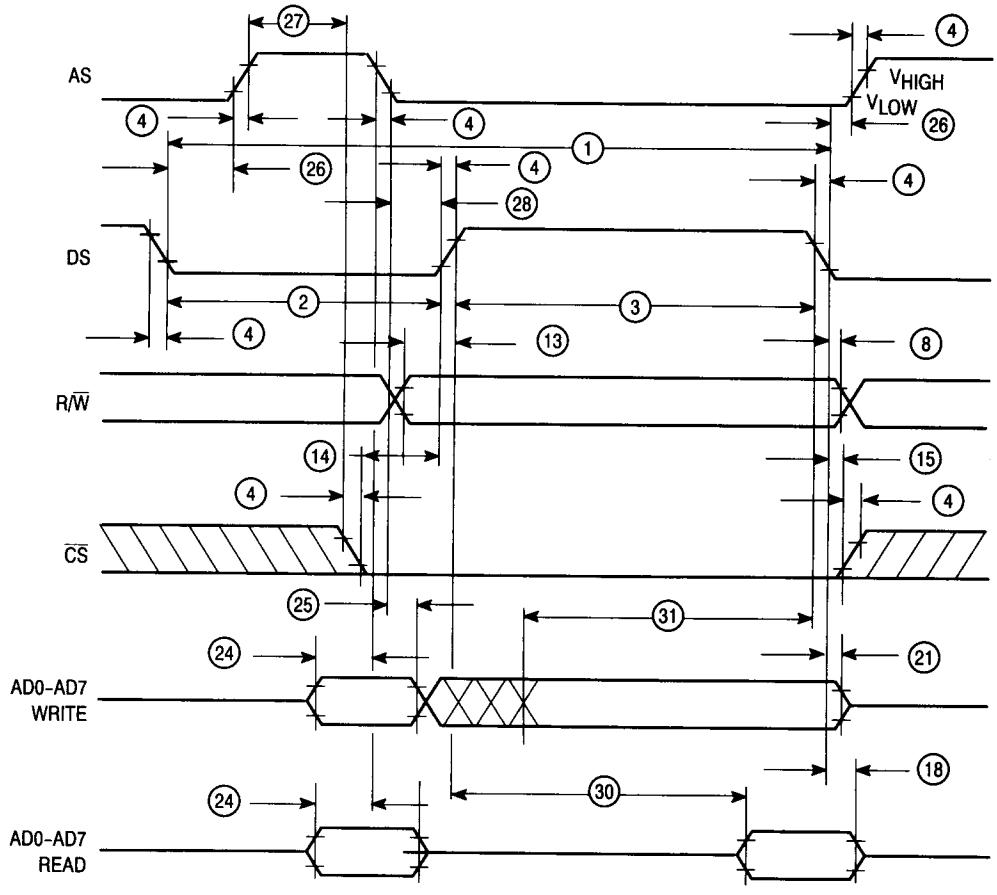
NOTES:
1. All outputs except $\overline{IRQ}$. $\overline{IRQ}$ has an open drain.
2. MOT has a 20 kΩ pulldown resistor. $\overline{RCLR}$ has a 20 kΩ pullup resistor.

2.5 BUS TIMING (V_{DD} = 4.5 to 5.5 V, C_L = 130 pF, T_A = 0 to 70°C)

Num.	Characteristics	Symbol	Guaranteed Limits				Unit
			MCCS146818B		MCCS156818B		
			Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	450	—	450	—	ns
2	Pulse Width, DS Low or R/$\overline{W}$ High	t_{WEL}	150	—	150	—	ns
3	Pulse Width, DS High or R/$\overline{W}$ Low	t_{WEH}	240	—	240	—	ns
4	Input Rise and Fall Time	t_r, t_f	—	30	—	30	ns
8	R/$\overline{W}$ Hold Time from DS Going Low	t_{RWH}	10	—	10	—	ns
13	R/$\overline{W}$ Setup Time Before DS	t_{RWS}	80	—	80	—	ns
14	Chip Select Setup Time Before DS or $\overline{WR}$ or $\overline{RD}$	t_{CS}	10	—	10	—	ns
15	Chip Select Hold Time from DS	t_{CH}	0	—	0	—	ns
18	Read Data Hold Time	t_{DHR}	10	80	10	80	ns
21	Write Data Hold Time	t_{DHW}	0	—	0	—	ns
24	Multiplexed Address Valid Time to AS/ALE Fall	t_{ASL}	30	—	30	—	ns
25	Multiplexed Address Hold Time	t_{AHL}	10	—	10	—	ns
26	Delay Time DS to AS/ALE Rise	t_{ASD}	20	—	20	—	ns
27	Pulse Width, AS/ALE High	t_{PASH}	40	—	40	—	ns
28	Delay Time, AS/ALE Going Low to DS Change or $\overline{WR}$ Change	t_{ASED}	30	—	30	—	ns
30	Peripheral Output Data or $\overline{WR}$ Change Delay Time from DS or $\overline{RD}$	t_{DDR}	20	240	20	240	ns
31	Peripheral Data Setup Time	t_{DSW}	75	—	75	—	ns

2.6 SWITCHING CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_A = 0 to 70°C)

Num.	Description	Symbol	Guaranteed Limits				Unit
			MCCS146818B		MCCS156818B		
			Min	Max	Min	Max	
33	$\overline{RESET}$ Pulse Width	t_{RWL}	5	—	5	—	µs
34	$\overline{RESET}$ Delay Time	t_{RLH}	5	—	5	—	µs
35	$\overline{IRQ}$ Release from DS	t_{IRDS}	—	2	—	2	µs
36	$\overline{IRQ}$ Release from $\overline{RESET}$	t_{IRR}	—	2	—	2	µs



NOTE: $V_{HIGH} = V_{IH}$ or V_{OH}
$V_{LOW} = V_{IL}$ or V_{OL}

Figure 2.1. Read/Write Timing for Motorola Bus Cycle

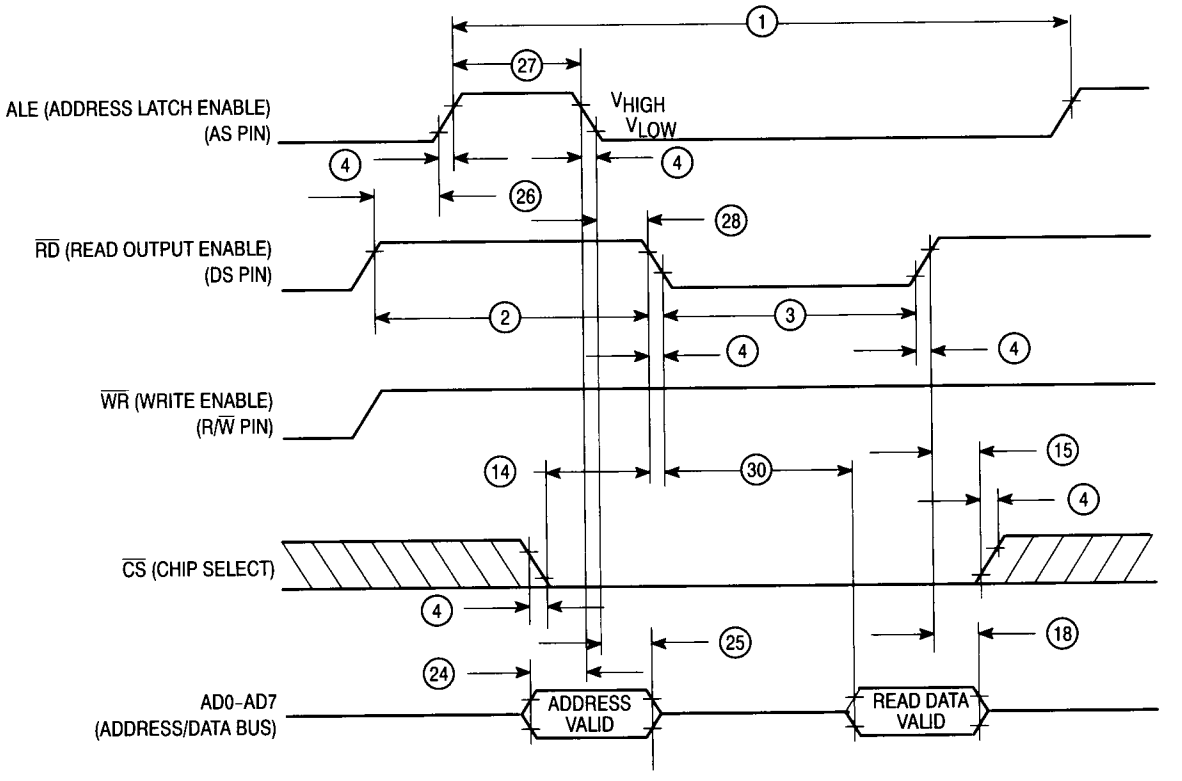


Figure 2.2. Intel Bus Read Cycle

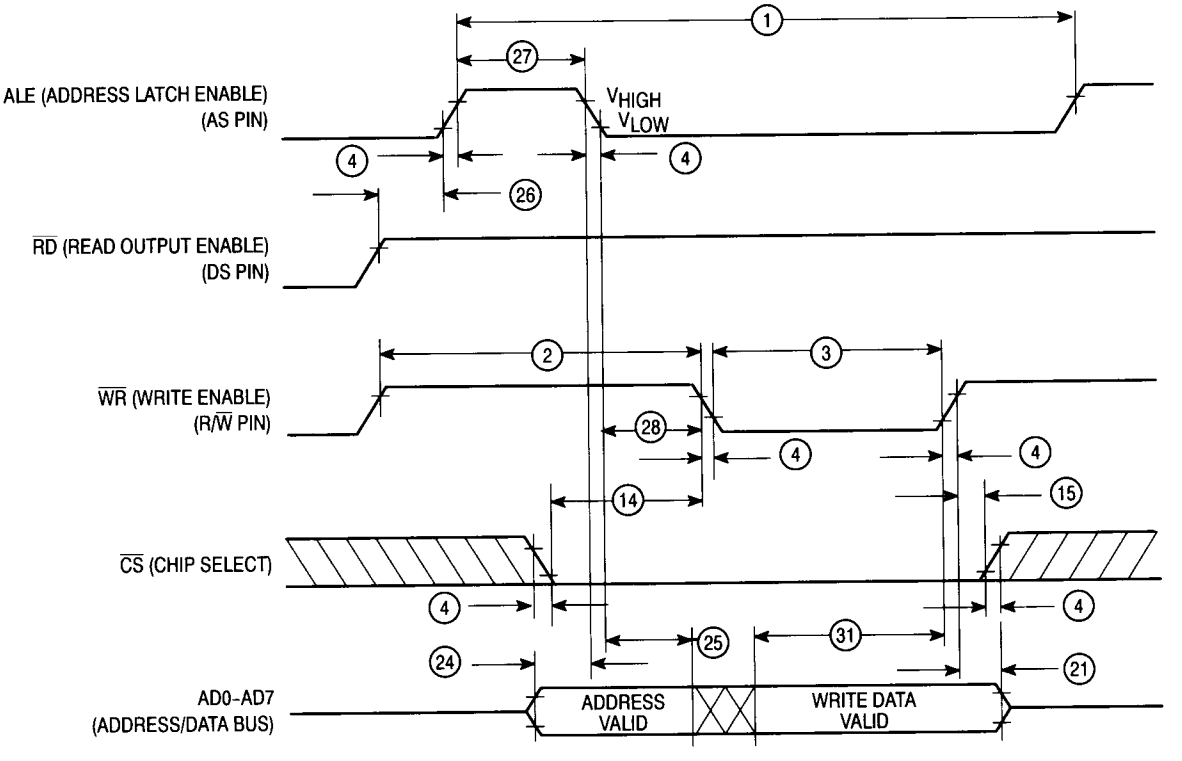
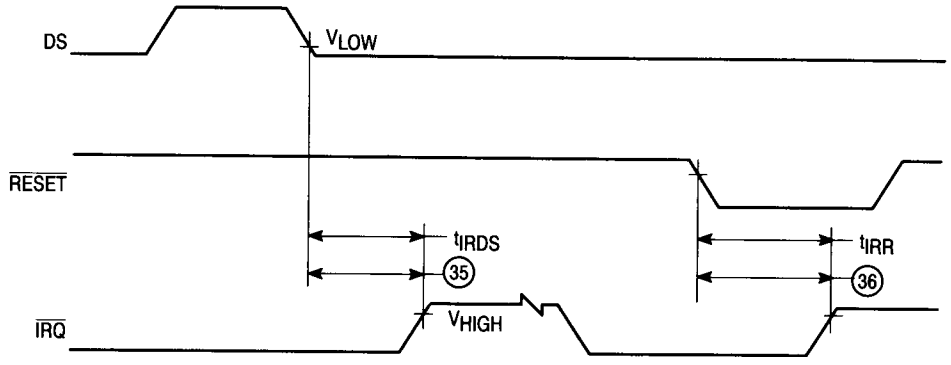


Figure 2.3. Intel Bus Write Cycle



NOTE: $V_{HIGH} = V_{DD} - 2.0$ V, $V_{LOW} = 0.8$ V for $V_{DD} = 5.0$ V ± 10%

Figure 2.4. $\overline{IRQ}$ Release Delay

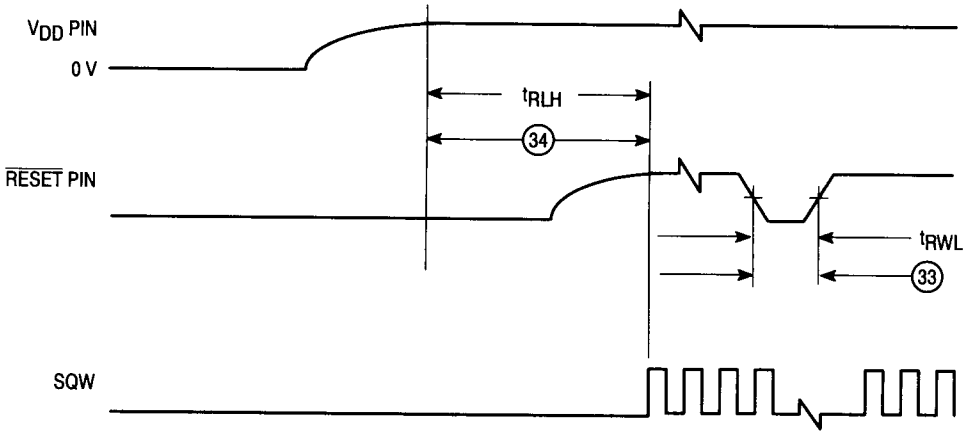
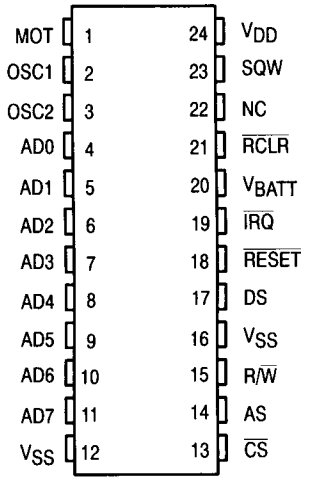
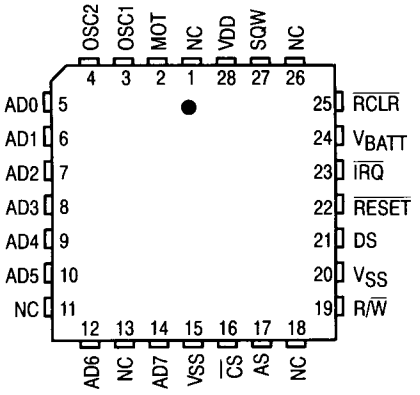


Figure 2.5. Power-Up Timing

SECTION 3
PIN DESCRIPTIONS

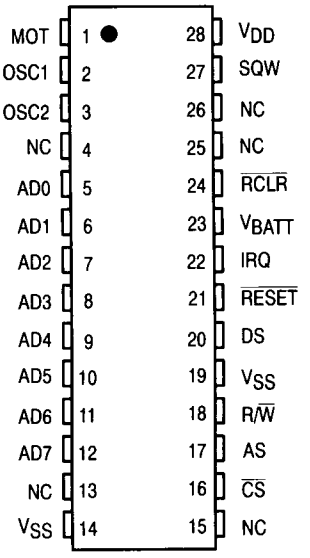


MCCS146818BP
MCCS156818BP
CASE 709
PLASTIC DIP



NC = No Connection

MCCS146818BFN
CASE 776
PQCC



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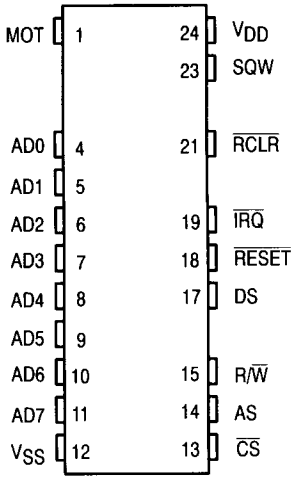
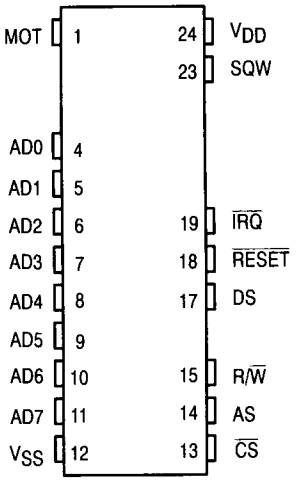
CASE 751F
SOG



MCCS146818B1M
MCCS156818B1M
CASE 905
MODULE



MCCS146818BM
MCCS156818BM
CASE 905
MODULE

Figure 3.1. Pin Assignments

PDIP* Pin #	PQCC Pin #	SOG Pin #	Pin Name	Description
1	2	1	MOTOROLA/INTEL MOT	This input pin is used to select different bus timing structures. When V_{DD} or a logic high is applied to this pin, the 18B responds to a Motorola microprocessor bus cycle. If a logic low or V_{SS} is applied to this pin, the Intel bus cycle is used. This pin should be hard-wired to V_{DD} or V_{SS} and should not change states during normal operation. See pin descriptions for R/$\overline{W}$, DS, and AS for more information. This pin has an internal 20 kΩ pulldown resistor.
2, 3	3, 4	2, 3	OSCILLATOR/ CRYSTAL OSC1, OSC2	These input/output pins serve a single function in two different ways. First, the user may attach a 32.768 kHz quartz crystal with a load capacitance of 6–8 pF to these pins to supply the on-board oscillator with a frequency reference. Second, OSC1 may be used to supply the 18B an off-chip 32.768 kHz signal to run the internal counters. This signal may be supplied from an external oscillator or other source. Figure 3.2 shows the schematic for both these configurations. Figure 3.3 shows the crystal equivalent circuit. External trimming capacitors are required and the voltage requirements are $0 V \leq V_{in} \leq V_{DD}$. The fixed input capacitor shown in Figure 3.2 may be replaced by a 5–15 pF tunable capacitor when higher accuracy is desired. Oscillator startup time is layout dependent. **Not available on module version.** Tuning measurements should **NOT** be taken from these pins. The SQW pin should be enabled and set up to output an 8.192 kHz signal via Registers A and B. Any frequency accuracy measurements should be made at the SQW pin. Measurements should be accurate to 3 decimal places. In the layout, traces MUST be kept as short as possible. No other traces should be routed under the oscillator. A ground ring around the oscillator circuit will improve noise rejection.
4–11	5–10, 12, 14	5–12	ADDRESS/DATA AD0–AD7	These input/output pins are the media for which data and information is passed to and from the system microprocessor or other host. These pins are multiplexed and supply the 18B with both address and data. An address is applied to these pins, and then an address select is applied to the AS pin (see the AS pin description). After the address is applied the SRAM or clock location may be read from or written to depending on the other control signals applied to the 18B. During a read cycle the data is valid after the DS or $\overline{RD}$ signal is applied. The delay is defined by t_{DDR} in the timing characteristics. The bus returns to a high impedance state after DS is removed. During a write cycle the data must be stable before the DS goes low or $\overline{WR}$ signal goes high. This parameter is also supplied in the ac characteristics of this data sheet. The address must be valid just prior to the fall of AS. These pins have an active pulldown of approximately 100 kΩ in standby mode.

*Module pin assignments are the same as for the PDIP unless otherwise noted in the Description column.

PDIP* Pin #	PQCC Pin #	SOG Pin #	Pin Name	Description
13	16	16	CHIP SELECT $\overline{CS}$	This input pin is used by the host's address decoding scheme to select or enable this device. This signal must be stable over the entire cycle. If unused, this input should be grounded. If grounded, the application must always use AS and DS in pairs, as any AS latches a new address into the internal address latch. For instance, if the $\overline{CS}$ pin is grounded and an AS occurs, an address is latched into the internal address buffer and internal decoding takes place to select the proper SRAM or clock location. At this point, a DS should be applied to act upon the data in that SRAM or clock location. DS can not be continually pulsed to access the same or next address. When V_{DD} is below $V_{BATT} \times 1.25$, the 18B internally inhibits access cycles by internally disabling the $\overline{CS}$ input. This action protects both the 18B clock data and SRAM data from a spurious write during a power cycle. This pin has an active pulldown of approximately 100 kΩ.
14	17	17	ADDRESS STROBE AS	This input pin is used to demultiplex the address/data bus. When an address is supplied to the 18B, this pin is pulsed, latching the address into internal latches. After this occurs, the data may then be transferred to or from the 18B via the address/data bus. This pin has an active pulldown of approximately 100 kΩ. See **Application Information** for more information.
15	19	18	READ/WRITE R/$\overline{W}$	The MOTEL circuit treats the R/$\overline{W}$ input pin in one of two ways. When a Motorola type processor is connected, R/$\overline{W}$ is a level sensitive input that indicates whether the current cycle is a read or write cycle. A read cycle is indicated with a high level on R/$\overline{W}$ while DS is high, a write cycle is a low on R/$\overline{W}$ during DS. The second interpretation of R/$\overline{W}$ is as negative write pulses, $\overline{WR}$, from an Intel processor. The MOTEL circuit in this mode gives R/$\overline{W}$ the same meaning as a write (W) pulse on many generic SRAMs. This pin has an active pulldown of approximately 100 kΩ.
17	21	20	DATA STROBE DS	This input pin has two interpretations via the MOT circuit. When emanating from a Motorola type processor, DS is a positive pulse during the latter portion of the bus cycle, and is variously called DS (data strobe), E (enable), and $\phi 2$ ($\phi 2$ clock or phase 2 clock). During read cycles, DS signifies the time that the 18B is to drive the bidirectional bus. In write cycles, the trailing edge of DS causes the 18B to latch the written data. See **Application Information**, item 2, for more information. The second MOT interpretation of DS is that of $\overline{RD}$ emanating from the Intel processor. In this case, DS identifies the time period when the 18B drives the bus with read data. This interpretation of DS is also the same, and an output-enable signal on a typical memory. This pin has an active pulldown of approximately 100 kΩ.

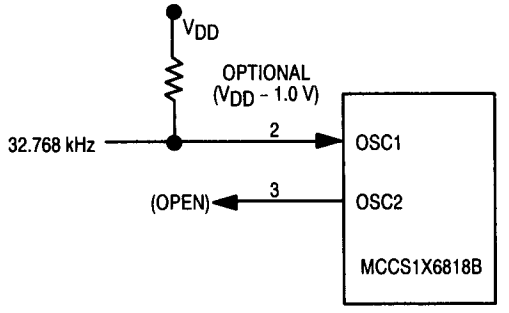
*Module pin assignments are the same as for the PDIP unless otherwise noted in the Description column.

PDIP* Pin #	PQCC Pin #	SOG Pin #	Pin Name	Description
18	22	21	RESET $\overline{\text{RESET}}$	This input pin does not affect the clock, calendar or SRAM functions of the 18B. On power up, the $\overline{\text{RESET}}$ pin should be held low for the specified item, t_{RLH}, in order for the power supply to stabilize during the power cycle. When $\overline{\text{RESET}}$ is low the following occurs: a) Periodic interrupt enable (PIE) bit is cleared to zero. b) Alarm interrupt enable (AIE) bit is cleared to zero. c) Update ended interrupt flag (UF) bit is cleared to zero. d) Interrupt request status flag (IRQF) bit is cleared to zero. e) Periodic interrupt flag (PF) is cleared to zero. f) The device is not accessible. g) Alarm interrupt flag (AF) bit is cleared to zero. h) $\overline{\text{IRQ}}$ pin is in a high impedance state. i) Square wave output enable (SQWE) is cleared to zero. j) Update ended interrupt enable (UIE) is cleared to zero. This connection allows the 18B to go in and out of power fail without affecting any of the control registers. $\overline{\text{RESET}}$ function is not available when $V_{DD} < (1.25 \times V_{BAT})$. This pin has an active pulldown of approximately 100 kΩ.
19	23	22	INTERRUPT REQUEST $\overline{\text{IRQ}}$	This output pin is an active-low open-drain to ground output of the 18B that may be used as an interrupt input to a processor. This $\overline{\text{IRQ}}$ output remains low as long as the status bit (bits 7–4 of Register C) causing the interrupt is present and the corresponding interrupt enable bit (bits 6–4 of Register B) is set. To clear the $\overline{\text{IRQ}}$ pin, the processor program normally reads Register C. The $\overline{\text{RESET}}$ pin also clears pending interrupts. When no interrupt conditions are present, the $\overline{\text{IRQ}}$ level is in the high impedance state. Multiple interrupting devices may thus be connected to an $\overline{\text{IRQ}}$ bus with one pullup at the processor. $\overline{\text{IRQ}}$ is disabled during Stand-by Mode.
20	24	23	BACKUP POWER V_{BATT}	This input pin supplies the 18B with power while the system is in Stand-by Mode. This input is designed for a 3.0 volt lithium cell. This voltage needs to be held between 2.2 and 3 volts for proper operation. The nominal write protect trip point voltage at which access to the 18B is prohibited, is set by internal circuitry as $1.25 \times V_{BATT}$. A maximum load of 700 nA at 25°C in the absence of V_{DD} should be used to size the battery or other source. See DC CHARACTERISTICS table. This device is optimized for a lithium cell. If a Ni-Cad is used the application must not allow the charging voltage at V_{BATT} to exceed the $V_{BATT} \times 1.25$ criteria. If the voltage at the V_{BATT} pin is too great, the device's internal power switching circuit disallows access to the device. **Not available on module version.**
21	25	24	SRAM CLEAR $\overline{\text{RCLR}}$	This input pin is used to set to logic high ($FF) all 114 bytes of general-purpose SRAM, but does not affect the RAM associated with the clock and calendar functions or registers. In order to clear the SRAM, $\overline{\text{RCLR}}$ must be forced to an input logic low (V_{SS}) during battery backup mode, when V_{DD} is not applied. This can be done by placing a jumper from $\overline{\text{RCLR}}$ to V_{SS} while the device is powered down. This pin has an internal 20 kΩ pullup. **Not available on 18BM version.** This pin must be left open in normal operation.

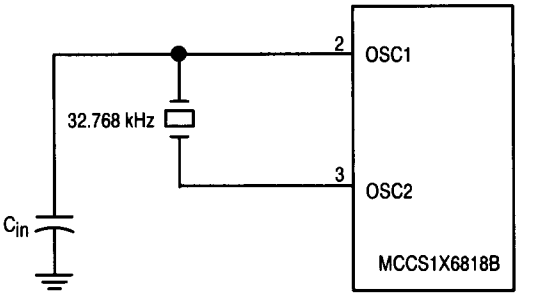
*Module pin assignments are the same as for the PDIP unless otherwise noted in the Description column.

PDIP* Pin #	PQCC Pin #	SOG Pin #	Pin Name	Description
23	27	27	SQUARE WAVE SQW	This output pin can output a signal from one of the 13 taps provided by the 15 internally-divided stages. The frequency of the SQW may be altered by programming Register A, as shown in Table 4.2. The SQW signal may be turned on by setting the SQWE (square wave enable) bit in Register B to a '1', logic high.
24	28	28	POWER V_{DD}	DC power, + 5 Vdc, is provided to the 18B via this pin. This pin supplies power only during normal operation. During stand-by mode, power is supplied via the V_{BATT} pin.
12, 16	15, 20	14, 19	POWER V_{SS}	These pins supply the 18B with system ground. One ground is convenient to ground the back-up battery; however, this ground may also be used as a system ground along with the battery ground. Both pins should be grounded for optimum performance. **Pin 16 not available on module version.**
22	1, 11, 13, 18, 26	4, 13, 15, 25, 26	NO-CONNECT NC	These pins are not connected to any internal device. **Pin 22 not available on module version.**

*Module pin assignments are the same as for the PDIP unless otherwise noted in the Description column.



3.2a — EXTERNAL SOURCE

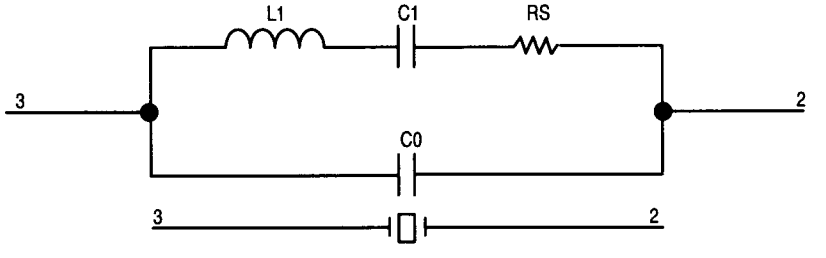


The value of C_{in} should be chosen according to the suppliers specifications.

3.2b — CRYSTAL SOURCE

NOTE: Figure not relevant to module versions.

Figure 3.2. Oscillator Input Configurations



f_{osc}	32.768 kHz
R_S (max)	50 kΩ
C_0 (max)	1.7 pF
C_1	0.003 pF
Q	40 k
C_{XTAL}	6–8 pF*
C_{in}	2–10 pF Fixed*

*May vary due to board layout

NOTE: Figure not relevant to module versions.

Figure 3.3. Crystal Equivalent Circuit

SECTION 4
REGISTER DESCRIPTIONS

4.1 INTRODUCTION

The 18B has four control registers which are accessible to the processor. The four registers are also fully accessible during the update cycle.

4.2 REGISTER A — READ/WRITE — ($0A)

Bit	7	6	5	4	3	2	1	0
Function	UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

Bit 7 — UIP — Update in Progress

The update in progress bit is a status flag that may be monitored by the user program. When UIP is a '1', if the update cycle is not in progress it will soon begin. When UIP is a '0', the update cycle is not in progress and will not be for at least 244 µs. The time, calendar, and alarm information in SRAM is fully available to the program when the UIP bit is '0'. The UIP is a read-only bit, and is not affected by $\overline{\text{RESET}}$. Writing the SET bit in Register B to a '1' inhibits any update transfer and clears the UIP status bit. This bit is read only.

Bits 6, 5, 4 — DV2, DV1, DV0 — Divider

These three bits are used to turn the oscillator on and off and to reset the count-down chain. A pattern of '010' is the only combination of bits that will turn the oscillator on and allow the 18B to keep time. A pattern of '11X' will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of '010' is written to DV2, DV1, DV0. '000' may be written to DV2–DV0 to turn off the oscillator to conserve power during shipping and storage. See Table 4.1 for more information.

Table 4.1. Divider Configurations

DV2	DV1	DV0	Divider $\overline{\text{RESET}}$	Oscillator
0	0	0	No	Off
0	0	1	No	Off
0	1	0	No	On
0	1	1	No	Off
1	0	0	No	Off
1	0	1	No	Off
1	1	0	Yes	On
1	1	1	Yes	On

Bits 3, 2, 1, 0 — RS3, RS2, RS1, RS0 — Rate Select

The four rate selection bits select one of 13 taps of the 15-stage divider, or disable the divider output. The tap selected may be used to generate an output square wave (SQW) and/or a periodic interrupt. The user may do one of the following:

1) Enable the interrupt with the PIE bit
2) Enable the SQW output pin with the SQWE bit
3) Enable both at the same time at the same rate
4) Enable neither

Table 4.2 lists the periodic interrupt rates and the square wave frequencies that may be chosen with the RS bits. These four bits are read/write bits that are not affected by $\overline{\text{RESET}}$.

Table 4.2. Periodic Interrupt and Square Wave Output Frequency

RS3	RS2	RS1	RS0	Periodic Interrupt Rate TPI	SQW Output Frequency
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 µs	8.192 kHz
0	1	0	0	244.141 µs	4.096 kHz
0	1	0	1	488.284 µs	2.048 kHz
0	1	1	0	976.562 µs	1.024 kHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

4.3 REGISTER B — READ/WRITE — ($0B)

Bit	7	6	5	4	3	2	1	0
Function	SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

Bit 7 — SET

When the SET bit is '0', the update cycle functions normally by advancing the clock count once per second. When the SET bit is written to a '1', any update cycle is inhibited and the program may initialize the time and calendar bytes without an update occurring during initialization. SET is a read/write bit that is not modified by $\overline{\text{RESET}}$ or an internal function of the 18B.

Bit 6 — PIE — Periodic Interrupt Enable

This bit is a read/write bit that allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{\text{IRQ}}$ pin low. The user writes a '1' to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3, RS2, RS1, and RS0 bits in Register A. A '0' in PIE blocks $\overline{\text{IRQ}}$ from being initiated by a Periodic Interrupt, but the PF bit is still set at the periodic rate. PIE is not modified by any internal 18B functions, but is cleared to '0' by $\overline{\text{RESET}}$.

Bit 5 — AIE — Alarm Interrupt Enable

This bit is a read/write bit that when set to a '1', permits the Alarm Flag (AF) bit in Register C to assert $\overline{\text{IRQ}}$. An Alarm Interrupt occurs when the three time bytes equal the three alarm bytes (including a "don't care" alarm code by binary 11XXXXXX). When the AIE bit is a '0', the AF bit does not initiate an $\overline{\text{IRQ}}$ signal. The $\overline{\text{RESET}}$ pin clears AIE to '0'. The internal functions do not affect the AIE bit.

Bit 4 — UIE — Update-Ended Interrupt Enable

This bit enables the Update-ended Flag (UF) bit in Register C to assert $\overline{\text{IRQ}}$ allowing an interrupt when an update is finished. The $\overline{\text{RESET}}$ pin does not affect the UIE. (The SET bit, Bit 7, going high resets this bit on the MCCS156818B only.)

Bit 3 — SQWE — Square Wave Enable

When this bit is set to a '1' by the user, a square wave signal at the frequency specified in the rate selection bits (RS3–RS0) in Register A appears on the SQW pin. When the SQWE bit is set to a '0', the SQW pin is held low. The state of SQWE is cleared by the $\overline{\text{RESET}}$ pin. This bit is reset to '0' when V_{DD} is cycled.

Bit 2 — DM — Data Mode

This bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and may be read by the user, but is not modified by any internal functions or $\overline{\text{RESET}}$. A '0' in DM signifies binary-coded-decimal (BCD) data, a '1' in DM signifies binary data.

Bit 1 — 24/12 — 24/12 Control Bit

This establishes the format of the hours bytes as either the 24-hour mode (24/12 = '1') or the 12-hour mode (24/12 = '0'). This bit is affected only by the software; $\overline{\text{RESET}}$ does not change this bit.

Bit 0 — DSE — Daylight Savings Enable

This bit is a read/write bit that allows the program to enable two special updates (DSE = '1'). On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM, it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a '0'. DSE is not changed by any internal operations or $\overline{\text{RESET}}$. The day of week byte must be set for the DSE function to operate properly.

4.4 REGISTER C — READ ONLY — ($0C)

Bit	7	6	5	4	3	2	1	0
Function	IRQF	PF	AF	UF	0	0	0	0

Bit 7 — IRQF — Interrupt Request Flag

This bit is set to a '1' when one or more of the following are true:

1) PF = PIE = '1'
2) AF = AIE = '1'
3) UF = UIE = '1'

i.e., IRQF = (PF × PIE) + (AF × AIE) + (UF × UIE)

Any time the IRQF bit is a '1', the $\overline{\text{IRQ}}$ pin is driven low. All flag bits (bits 4–6 of Register C) are cleared after Register C is read or when $\overline{\text{RESET}}$ occurs.

Bit 6 — PF — Periodic Interrupt Flag

This bit is a read-only bit that is set to a '1' when a particular edge is detected on the selected tap of the divider chain. The RS3–RS0 bits establish the periodic rate. PF is set to a '1' independent of the state of the PIE bit. PF being a '1' initiates an $\overline{\text{IRQ}}$ signal and sets the IRQF bit only when PIE is also a '1'. The PF bit is cleared by a $\overline{\text{RESET}}$ or a read of Register C.

Bit 5 — AF — Alarm Flag

A '1' in this bit indicates that the current time has matched the alarm time. A '1' in AF causes the $\overline{\text{IRQ}}$ pin to go low and a '1' to appear in the IRQF only when the AIE bit is also set to a '1'. A $\overline{\text{RESET}}$ or a read of Register C clears AF.

Bit 4 — UF — Update-Ended Interrupt Flag

This bit is set after each update cycle. When the UIE bit is a '1', the '1' in UF causes the IRQF bit to be a '1', asserting $\overline{\text{IRQ}}$. UF is cleared by a Register C read or a $\overline{\text{RESET}}$.

Bits 3–0 — Unused

These bits are unused and are read as 0. They can not be written.

4.5 REGISTER D — READ ONLY — ($0D)

Bit	7	6	5	4	3	2	1	0
Function	VRT	0	0	0	0	0	0	0

Bit 7 — VRT — Valid SRAM and Time

This bit indicates the condition of the contents of the SRAM. A '0' appears in the VRT bit when V_{BATT} < 2.2 V. This indicates invalid data in SRAM or questionable data in SRAM. The VRT is a read-only bit that is not modified by the $\overline{RESET}$ pin. The VRT bit can be reset only by reading Register D. For the module, this indicates a bad battery and the device may need replacement.

Bits 6–0 — Unused

These bits are not used and should not be written to.

SECTION 5
FUNCTIONAL DESCRIPTION

5.1 ADDRESS MAP

Figure 5.1 shows the address map of the 18B. The memory consists of 114 general-purpose SRAM bytes; 10 SRAM bytes that contain the time, calendar, and alarm data; and 4 SRAM bytes that contain control and status information. All 128 bytes are directly readable and writeable by the processor program except for the following: 1) Registers C and D are read only, 2) bit 7 of Register A is read only, and 3) the high-order bit of the seconds byte is read only and is always '0'. The contents of the four control and status registers (A, B, C, and D) are described in **Register Descriptions**, Section 4.

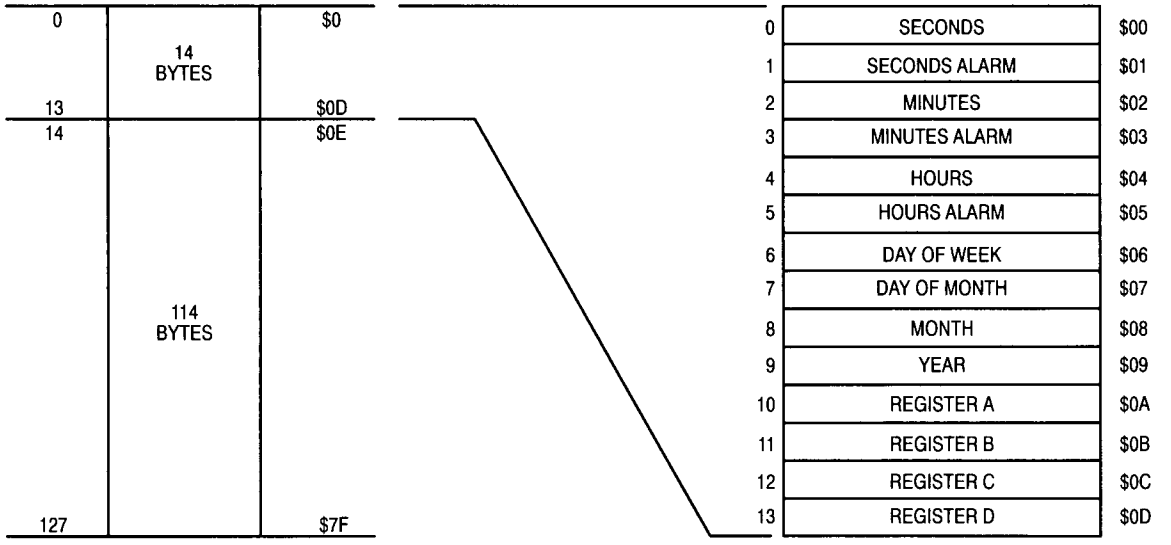


Figure 5.1. Address Map

5.2 TIME, CALENDAR, AND ALARM LOCATIONS

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar, and alarm by writing to these SRAM locations. The contents of the 10 time, calendar, and alarm bytes may be either binary-coded-decimal (BCD) or binary. Before initializing the internal registers, the SET bit in Register B should be set to a '1' to prevent time/calendar updates from occurring. The program initializes the 10 locations in the selected format (binary or BCD), then indicates the format in the data mode (DM) bit of Register B. All 10 time, calendar, and alarm bytes must use the same data mode, binary or BCD. The SET bit may now be cleared to allow updates. Once initialized, the real-time clock makes all updates in the selected data mode. The data mode cannot be changed without reinitializing the 10 data bytes.

Table 5.1 shows the binary and BCD formats of the 10 time, calendar, and alarm locations. The 24/12 bit in Register B establishes whether the hour locations represent 1-to-12 or 0-to-23 hours. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high-order bit of the hours byte represents PM when it is a '1'.

The three alarm bytes may be used in two ways. First, when the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second usage is to insert a don't care code in any hexadecimal byte from $C0 to $FF. That is, the two most significant bits of each byte, when set to '1', create a don't care situation. An alarm interrupt each hour is created with a don't care code in the hours alarm locations. Similarly, an alarm is generated every minute with don't care codes in the hours and minutes alarm bytes. The don't care codes in all three alarm bytes create an interrupt every second.

Table 5.1. Time, Calendar, and Alarm Data Modes

Address Location	Function	Decimal Range	Range	
			Binary Data Mode	BCD Data Mode
$0	Seconds	0-59	$00–$3B	$00–$59
$1	Second Alarm	0–59	$00–$3B	$00–$59
$2	Minutes	0–59	$00–$3B	$00–$59
$3	Minute Alarm	0–59	$00–$3B	$00–$59
$4	Hours 12 Hour 24 Hour	 1–12 0–23	 $01–$0C AM $81–$8C PM $00–$17	 $1-$12 AM $81–$92 PM $00–$23
$5	Hour Alarm 12 Hour 24 Hour	 1–12 0–23	 $01–$0C AM $81–$8C PM $00–$17	 $01–$12 AM $81–$92 PM $00–$23
$6	Day of Week Sunday = 1	 1–7	 $01–$07	 $01–$07
$7	Day of Month	1–31	$01–$1F	$01–$31
$8	Month	1–12	$01–$0C	$01–$12
$9	Year	0–99	$00–$63	$00–$99

5.3 STATIC CMOS SRAM

The 114 bytes of general-purpose SRAM are not dedicated within the 18B. They can be used by the processor program, and are fully available during the update cycle.

While time and calendar information must use battery back-up, very frequently there is other nonvolatile data that must be retained when main power is removed. The 114 user SRAM bytes serve the need for low-power CMOS battery-backed storage, and extend the SRAM available to the program.

5.4 POWER DOWN CONSIDERATIONS

During and after the power source conversion, the V_{in} maximum specification must never be exceeded. Failure to meet the V_{in} maximum specification can cause a virtual SCR to appear, which may result in excessive current drain and destruction of the part. During the transition from system to battery power, the designer of a battery backed-up system must protect data integrity, minimize power consumption, and ensure hardware reliability.

When V_{DD} is applied to the 18B, and reaches a level of greater than V_{BATT} pin potential x 1.25, the device becomes accessible. When V_{DD} falls below V_{BATT} x 1.25, the chip select input is internally forced to an inactive level regardless of the value of $\overline{CS}$ at the input pin, and the 18B is write protected. When the 18B is in a write protected state, all inputs are ignored and all outputs are in a high impedance state.

For the module, while V_{DD} is less than V_{BATT}, the device is powered by the internal lithium cell.

5.5 UPDATE CYCLE

The 18B executes an update cycle once per second provided the DV0–DV2 divider bits are 010 and the SET bit (in Register B) is clear. When an update cycle occurs, the contents of an internal SRAM is updated by one second. A transfer of the user copy SRAM to the internal SRAM occurs prior to the update when a write to any of the timekeeping SRAM has been detected between update cycles. After the update cycle is finished, the new values will be written to the user copy of the timekeeping SRAM.

An exception to the update cycle occurs when the SET bit in Register B is set to a '1'. The SET bit in a '1' state permits the program to initialize the time and calendar bytes by inhibiting update transfers. If the SET bit is set to a '1', SRAM will be frozen, but the internal copy of SRAM will continue to keep time and will issue an alarm match if it occurs. Upon the release of the SET bit, update cycles would result with a transfer of data to the user copy SRAM.

The primary function of the update cycle is to increment the seconds byte, check for overflow, increment the minutes byte when appropriate and so forth through the year of the century byte. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match occurs or if a don't care code (11XXXXXX) is present in all three positions.

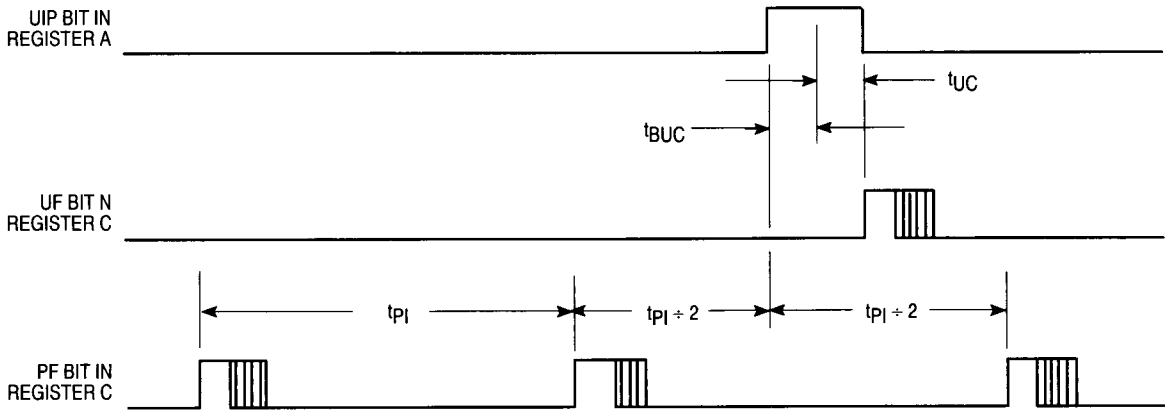
Three methods of accommodating non-availability during update are usable by the program. In discussing the three methods, it is assumed that at random points user programs are able to call a subroutine to obtain the time of day.

The first method of avoiding the update cycle uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that 999 ms are available to read valid time and date information. During this time a display could be updated or the information could be transferred to continually available SRAM. Before leaving the interrupt service routing, the IRQF bit in Register C should be cleared.

The second method uses the UIP in Register A to determine if the update cycle is in progress or not. The UIP bit will pulse once per second. After the UIP bit goes high, the update cycle begins 244 µs before the time/calendar data may be valid. The user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C. Periodic interrupts that occur at a rate of greater than $t_{BUC} + t_{UC}$ (see Figure 5.2) allow valid time and date information to be read at each occurrence of the periodic interrupt. The reads should be completed within $(t_{PL}/2) + t_{BUC}$ to ensure that data is not read during the update cycle.

To properly set up for daylight savings time operation, the user must set the time at least one second before the roll over will occur (i.e., 1:59:59 AM).



t_{PI} = Periodic Interrupt Time Interval (500 ms, 125 ms, 62.5 ms, etc. per Table 2)
t_{UC} = Update Cycle Time (1984 µs)
t_{BUC} = Delay Time Before Update Cycle (244 µs)

Figure 5.2. Update Ended and Periodic Relationships

5.6 DIVIDER STAGES

The 18B has 13 binary-divider stages following the time base as shown in the block diagram. The output of the dividers is a 1 Hz signal to the update system logic. The dividers are controlled by three divider bits (DV2, DV1, DV0) in Register A. The only time base for this device is 32.768 kHz. The divider chain may be held at reset, which allows precision setting of the time. When the divider is changed from reset to an operation time base, the first update system is one second later.

5.7 SQUARE-WAVE OUTPUT SELECTION

Thirteen divider taps are made available to a 1-of-13 selector as shown in the block diagram. The first purpose of selecting a divider tap is to generate a square wave output signal at the SQW pin. The RS0–RS3 bits in Register A establish the square wave frequency as listed in Table 4.2. The SQW frequency selection shares the 1-of-13 selector with the periodic interrupts.

Once the frequency is selected, the output of the SQW pin may be turned on and off under program control with the square wave output selection bit (SQWE bit) in Register B. The 18B then generates a symmetrical waveform at the time of execution. The square wave output pin has a number of potential uses. For example, it can serve as a frequency standard for internal use or as a frequency synthesizer, or could be used to generate one or more audio tones under program control.

5.8 INTERRUPTS

The RTC plus SRAM includes three separate fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at rates from once-per-second to one-per-day. The periodic interrupt may be selected for rates from half-a-second to 122 µs. The update-ended interrupt may be used to indicate to the program that an update cycle is completed. Each of these independent interrupt conditions is described in greater detail in other sections of this data sheet.

The processor program selects which interrupts, if any, it wishes to receive. Three bits in Register B enable the three interrupts. Writing a '1' to an interrupt-enable bit allows the interrupt to be initiated when the event occurs. A '0' in the interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted due to the interrupt cause.

If an interrupt flag is already set when the interrupt becomes enabled, the $\overline{IRQ}$ pin is immediately activated, though the interrupt causing the event may have occurred much earlier. Thus, there are cases where the programs should clear such earlier interrupts before first enabling new interrupts.

When an interrupt event occurs, a flag bit is set to a '1' in Register C. Each of the three interrupt sources has separate flag bits in Register C, which are set independent of the state of the corresponding enable bits in Register B. The flag bit may be used with or without enabling the corresponding enable bits.

In the software scanned or polling case, the program does not enable the interrupt. The interrupt flag bit becomes a status bit, which the software interrogates when it wishes. When the software detects that the flag is set, it is an indication to the software that the interrupt event occurred since the bit was last read.

However, there is one precaution. The flag bits in Register C are cleared (record of the interrupt event is erased) when Register C is read. Double latching is included with Register C so the bits that are set are stable through the read cycle.

All bits that are high when read by the program are cleared, and new interrupts (on any bits) are held after the read cycle. One, two, or three flag bits may be found to be set when Register C is used. The program should inspect all utilized flag bits every time register C is read to insure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as one of the three interrupted sources has its flag and enables bits set. The IRQF bit in Register C is a '1' whenever the $\overline{IRQ}$ pin is being driven low.

The processor program can determine that the RTC initiated the interrupt by reading Register C. A '1' in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the part. The act of reading Register C clears all the then active flag bits, plus the IRQF bit. When the program finds IRQF set, it should look at each of the individual flag bits in the same byte which have the corresponding interrupt-mask bit set and service each interrupt which is set. Again, more than one interrupt-flag may be set.

5.9 PERIODIC INTERRUPT SELECTION

The periodic interrupt allows the $\overline{IRQ}$ pin to be triggered from once every 500 ms to once every 122 μs. The periodic interrupt is separate from the alarm interrupt, which may be output from once per second to once per day.

Table 4.2 shows that the periodic interrupt rate is selected with the same Register A bits that select the square wave frequency. Changing one also changes the other. But each function may be separately enabled so that a program could switch between the two features or use both. The SQW pin is enabled by the SQWE bit in Register B. Similarly the periodic interrupt is enabled by the PIE bit in Register B.

Periodic interrupt is usable by practically all real time systems. It can be used to scan for all forms of inputs from contact closure to serial receive bits or bytes. It can be used in multiplexing displays or with software counters to measure inputs, create output intervals, or await the next needed software function.

SECTION 6
APPLICATION INFORMATION

6.1 MCCS1X6818B APPLICATIONS

Refer to Figure 6.1, Figure 6.2 and the following notes for application examples.

1. The MCCS146818B (18B) will drop directly into an MC146818A (18A) circuit with some modifications. The user may use the 18B if the following steps are taken:

   a) Cut trace or wire going to CKFS on the 18A; this is a battery connection on the 18B. The user needs to supply battery back-up power to this pin. A 3.0 V lithium cell is suggested.

   b) Cut the trace or wire to CKOUT on the 18A; this pin is used to clear the contents of the SRAM in stand-by mode on the 18B.

   c) It is not recommended to connect any signal to the NC on the 18B. Therefore, it is suggested that the user cut the wire or trace going to these pins and leave them open.

   d) The user will need to disconnect the battery from V_{DD} on the 18A. The battery connection for the 18B is on the V_{BATT} pin. While Ni-Cads may be used (see V_{BATT} in Pin Descriptions) the part is designed for a lithium cell.

   e) The 18B is a one-frequency device. The only crystal this chip accepts is the 32.768 kHz 6–8 pF type. If the user has the 1, 2, or 4 MHz crystal or oscillator in the 18A circuit, these will need to be replaced with the 32.768 kHz type. For this reason, the 18B cannot be used in applications that take advantage of the 18A's 1, 2, or 4 MHz clock outputs.

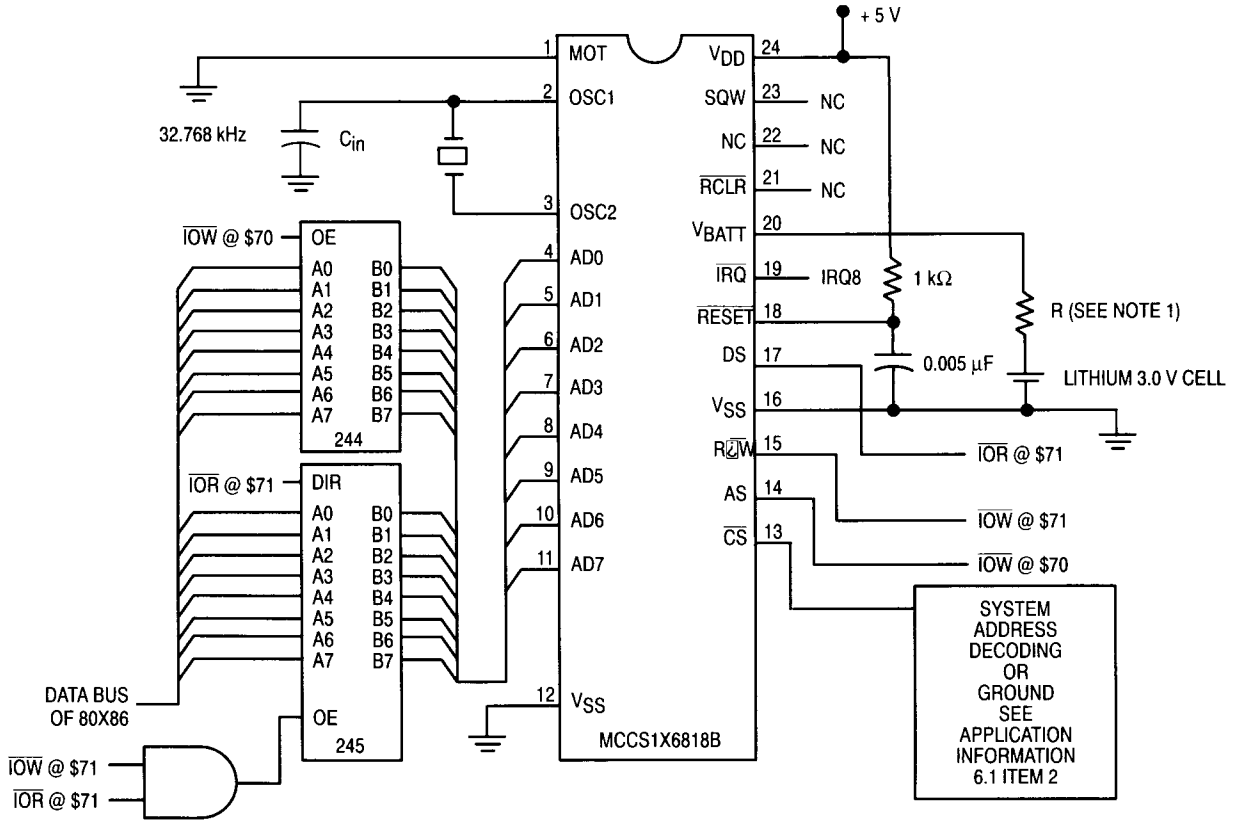
   f) V_{SS} is used for a system ground. The 18A used this as a stand-by input signal. This function is now done internally and this trace or wire will need to be replaced with a system ground or with a battery ground.

   g) The user may also wish to replace the 18A with an 18B1M, which will eliminate all the above except items b) and e). The $\overline{RCLR}$ pin on the 18B1M will need to be clipped off for proper operation. Or, the user may wish to use the 18BM which already has the $\overline{RCLR}$ pin clipped. The 18BM includes the 18B along with a crystal and a battery encapsulated into a module. The 18B1M is the same module with $\overline{RCLR}$ available.

2. In some applications, the user may choose to tie $\overline{CS}$ directly to ground. This is acceptable; however, this will force the programmer to always apply AS and DS in pairs. This means that if $\overline{CS}$ is grounded, any ALE (IBM/Intel timing cycle) will cause a new address to be latched into the 18B. It is good practice to use the AS and DS signals in pairs at any time in any application. It is also good practice to use a true chip select derived from address decoding for $\overline{CS}$.

If $\overline{CS}$ is grounded, the user must always use AS and DS in pairs since any AS will latch a new address into the internal address latch. For instance, If the $\overline{CS}$ pin is grounded and an AS occurs, an address is latched into the internal address buffer and internal decoding takes place to select the proper SRAM or clock location. At this point, a DS should be applied to act upon the data in said SRAM or clock location.

3. C_{in} is dependent on C_L of the XTAL being selected. The recommended C_L of the crystal is 6–8 pF.
4. This device is optimized for a lithium cell. If a Ni-Cad is used the application must not allow the charging voltage at the V_{BATT} pin to exceed the $V_{BATT} \times 1.25$ criteria. That is, if the voltage at the V_{BATT} pin is too great, the device's internal power switching circuit will disallow access to the device.
5. For the MCCS156818B, care should be taken when using an external TTL clock reference. The upper rail must be limited to V_{BATT} + 0.6 V.



NOTES:
1. Motorola recommends that this resistor be used as a design consideration based on knowledge of the internal circuitry of the 18B. This resistor is **not** required for UL approval and may be omitted.
2. The IBM AT writes a 7-bit address to I/O port $70 and then reads the data from I/O port $71 or writes I/O address $71. This is a typical application for a non-multiplexed bus.
3. C_{in} is dependent on C_L of XTAL being selected.

Figure 6.1. IBM/INTEL Application Circuit
Multiplexed Bus IBM PC/AT
Intel 80X86 Multiplexed Bus Microprocessors

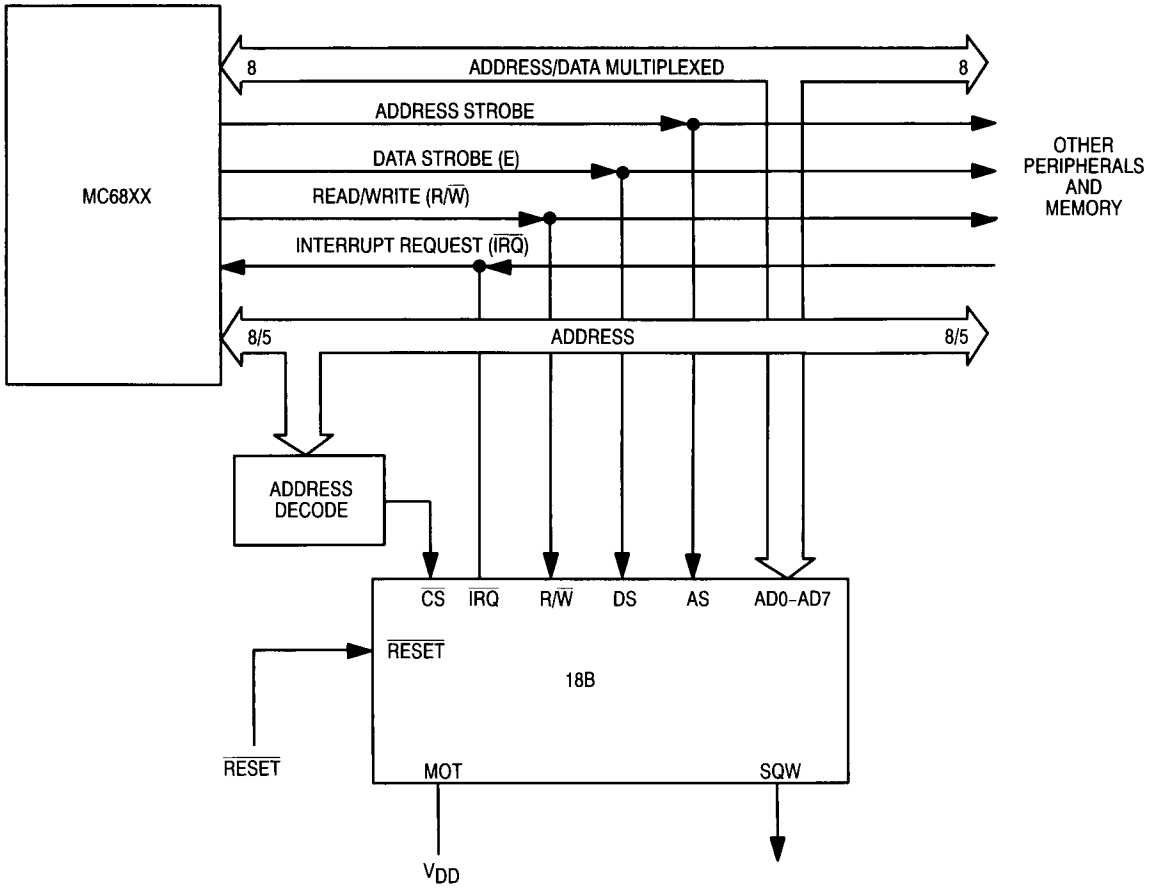


Figure 6.2. 18B Interfaced with Motorola Compatible Multiplexed Bus

6.2 MODULE APPLICATIONS

Refer to Figure 6.3 and the following notes for application examples.

1. The MCCS146818B1M will drop directly into an 18A circuit with some modifications. The user may use the 18B1M if the following steps are taken;

   a) Cut trace or wire going to $\overline{RCLR}$ on 18B. This pin is used to clear the contents of the SRAM in stand-by mode. The user may also choose an 18BM which has the $\overline{RCLR}$ pin already clipped.

   b) The user will need to disconnect the battery and charging circuit from V_{DD}. The battery is now internal and requires no charging.

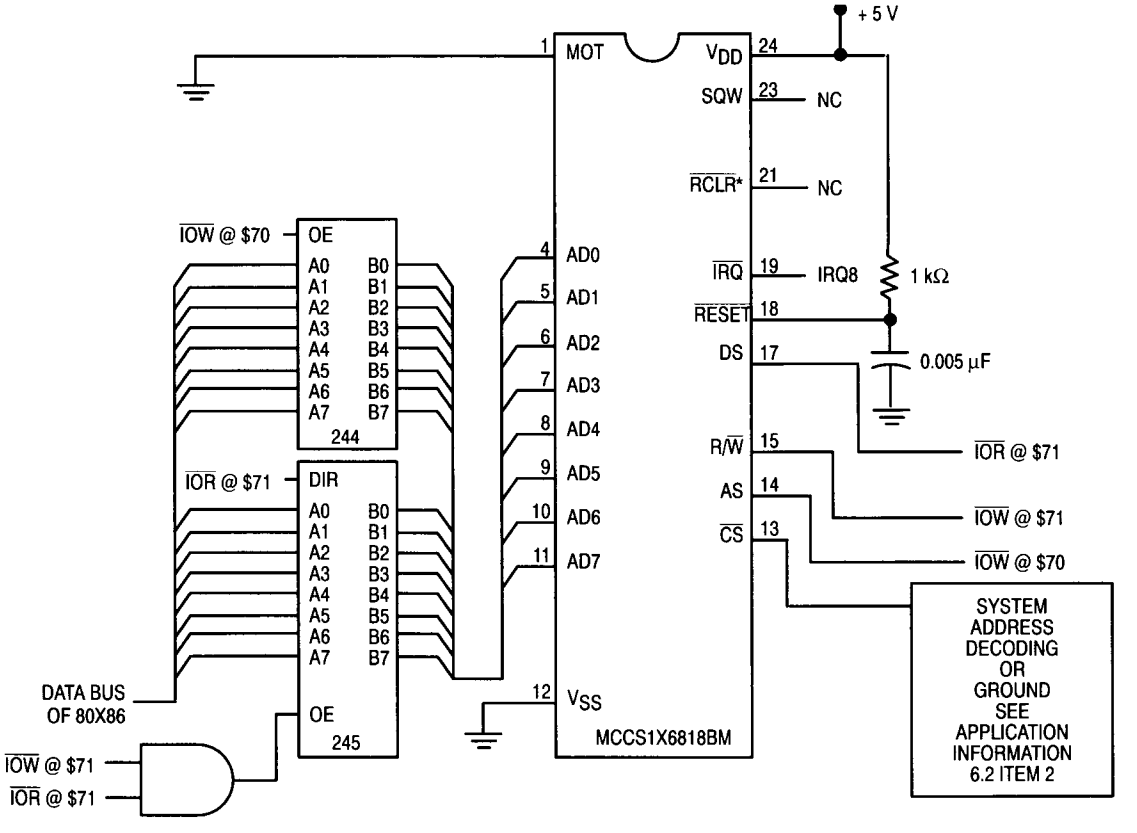
2. In some applications the user may choose to tie $\overline{CS}$ directly to ground. This is acceptable; however, this will force the programmer to always apply AS and DS in pairs. This means that if $\overline{CS}$ is grounded, any ALE (IBM/Intel timing cycle) will cause a new address to be latched into the 18B1M. It is good practice to use the AS and DS signals in pairs at any time in any application. It is also good practice to use a true chip select derived from address decoding for $\overline{CS}$.

If $\overline{CS}$ is grounded the user must always use AS and DS in pairs since any AS will latch a new address into the internal address latch. For instance, If the $\overline{CS}$ pin is grounded and an AS occurs, an address is latched into the internal address buffer and internal decoding takes place to select the proper SRAM or clock location. At this point, a DS should be applied to act upon the data in said SRAM or clock location.

3. Battery is sealed from outside contaminants, thus increasing battery reliability. The RTC chip pulls 500 to 700 nA at 25°C. The battery installed has a 42 mAh capacity.

42 mAh/700 nA = 60,000 h (MCCS146818B)
42 mAh/500 nA = 84,000 h (MCCS156818B)

Actual battery life is dependent on duty cycle (computer on time/computer off time), where a larger duty cycle indicates a longer battery life of the RTC. The above formulas are for approximation only.

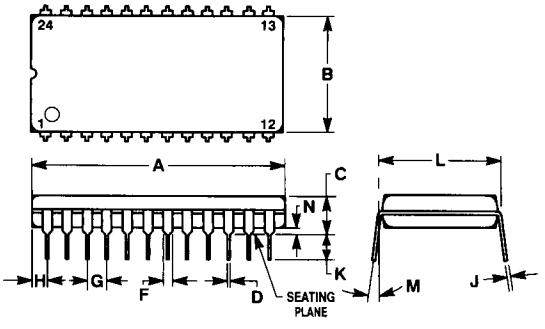


NOTE: $\overline{RCLR}$ not available on 18BM devices.

Figure 6.3. IBM/INTEL Application Circuit
Multiplexed Bus IBM PC/AT
Intel 80X86 Multiplexed Bus Microprocessors

SECTION 7
PACKAGE DIMENSIONS

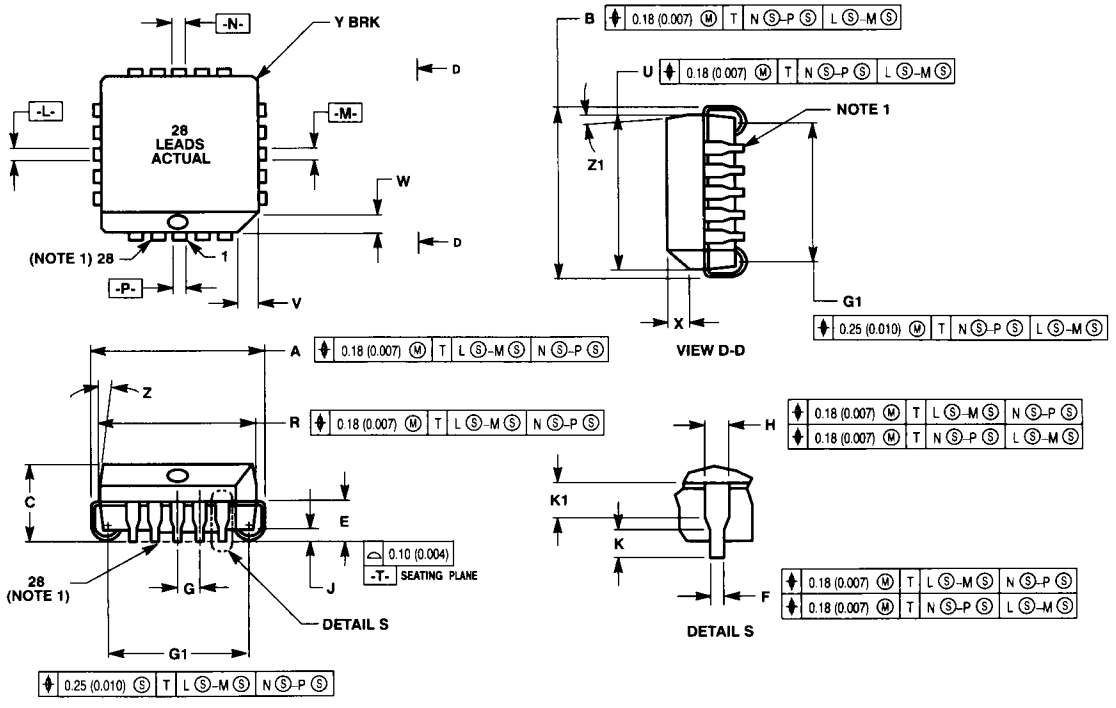
7.1 P SUFFIX, PLASTIC DIP (Case 709-02)



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. 709-01 OBSOLETE, NEW STANDARD 709-02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

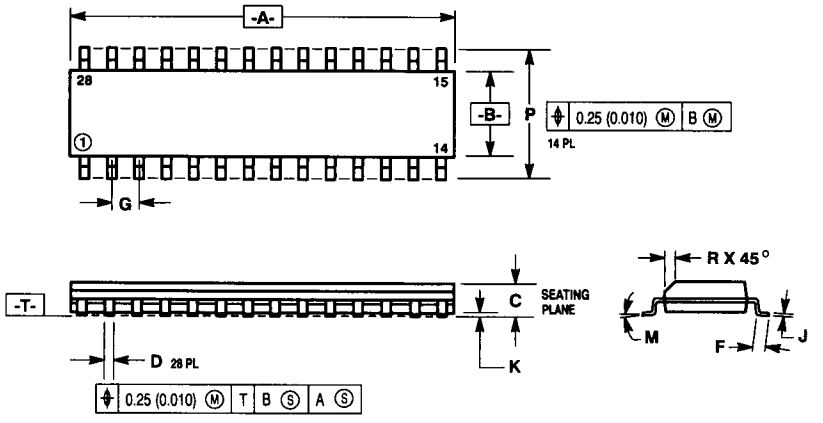
7.2 FN SUFFIX, PQCC (Case 776-02)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	11.43	11.58	0.450	0.456
U	11.43	11.58	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2 °	10 °	2 °	10 °
G1	10.42	10.92	0.410	0.430
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

NOTES:
1. **DUE TO SPACE LIMITATION, CASE 776-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 28 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.
7. 776-01 OBSOLETE, NEW STANDARD 776-02.

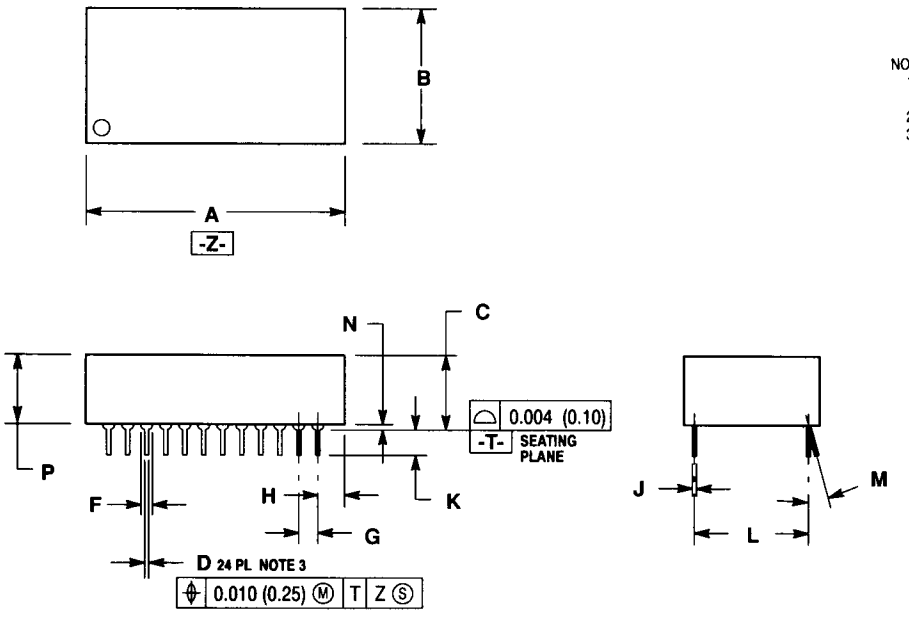
7.3 DW SUFFIX, SOG (Case 751F-03)



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.711
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.229	0.317	0.0090	0.0125
K	0.127	0.292	0.0050	0.0115
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

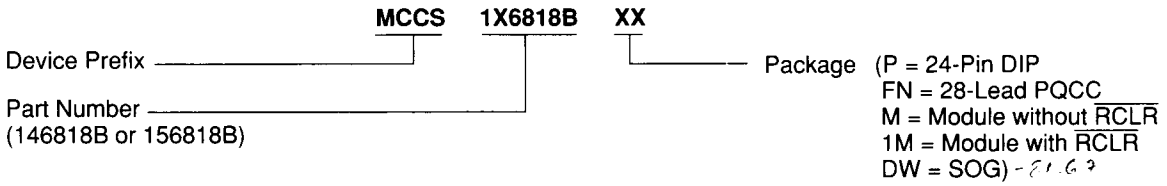
7.4 MODULE (Case 905-01)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. VARIOUS LEADS MISSING, DEPENDENT ON PART TYPE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	33.02	34.54	1.300	1.360
B	17.40	18.16	0.685	0.715
C	8.92	10.01	0.351	0.394
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BASIC		0.100 BASIC	
H	2.54	3.56	0.100	0.140
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BASIC		0.600 BASIC	
M	0°	15°	0°	15°
N	0.23	0.74	0.009	0.029
P	8.51	9.27	0.335	0.365

SECTION 8
ORDERING INFORMATION



Full Part Numbers —		
	MCCS146818BP	MCCS156818BP
	MCCS146818BFN	MCCS156818BM
	MCCS146818BM	MCCS156818B1M
	MCCS146818B1M	MCCS156818BDW

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