

<b>SANYO</b>	No. 3438A	<b>LC65404A</b>
		(A/D Converter, FLT drivers, PWM Output, and On-chip 4Kbyte ROM) <b>4-bit Single Chip Microcomputer for Control Applications</b>

The LC65404A is a 52-pin CMOS 4-bit single chip microcomputer. It consists of a high-speed core CPU with the minimum cycle time = 0.92 $\mu$ F, 8-bit AD converter with 8 input channels, 4Kbyte ROM and a 1Kbit RAM (256 x 4 bits).

The LC65404A has a total of 41 input/output (I/O) port pins; 29 for high withstand outputs (Drivers for fluorescent display tubes and LEDs), and 12 for input/output (including the alternative pins to interrupt inputs and serial input).

In addition, this single-chip microcomputer has a two-channel timer. This timer circuit block can be used as a general-purpose timer, watchdog timer, time base timer, PWM type DA converter, melody tone generator and the like within application products. It is designed based on various standby operation modes. As a result, the LC65404A microcomputer can be embedded into many kinds of home appliances as, for example, display control and timer control in audio visual products.

There is another microcomputer with almost all the LC65404A functions but oscillation circuit design and ambient operating temperature range. Its chip name is LC65204A. This single chip device has a subclock function and its operating temperature range is from minus 30 °C (-30) to plus 70 °C (+70). For detailed information, refer to its catalog. Note that the LC65404A should be used with the X1 pin connected to the V<sub>DD</sub> and the X2 pin left open.

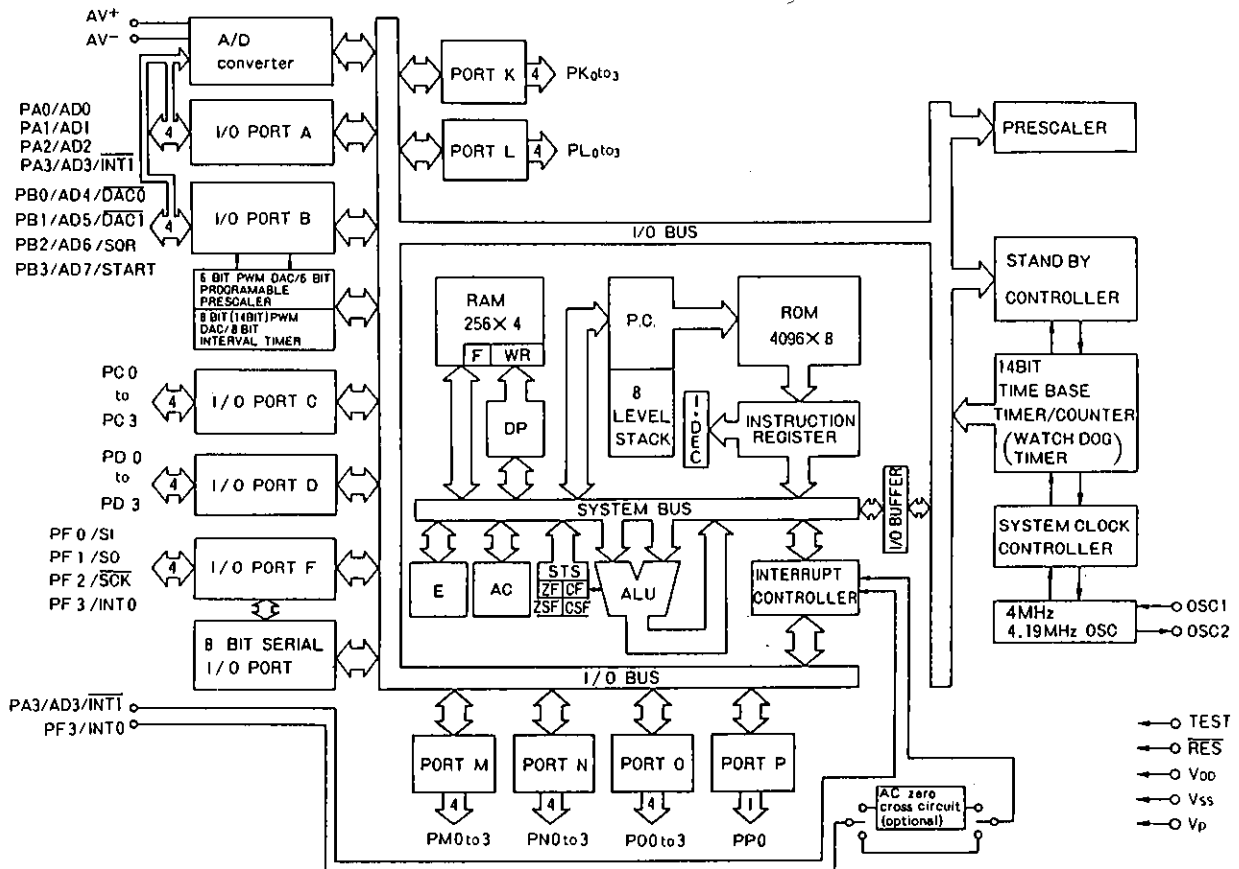
#### Features:

- Seventy-seven instructions
- On-chip storage capacity; 4Kbyte ROM and 1Kbit (256 x 4 bits) RAM
- Minimum instruction cycle time: 0.92 $\mu$ s (4.33MHz at V<sub>DD</sub> = 4.5V or greater)  
1.84 $\mu$ s (2.17MHz at V<sub>DD</sub> = 4.0V or greater)
- Reduced power dissipation mode through system clock selection by software
  - Main system clock = 4.19MHz : 0.95 $\mu$ s, 1.9 $\mu$ s and 30.6 $\mu$ s
- Operating temperature: T<sub>a</sub> = -30 °C to +85 °C
- Working register/Flag function
  - (16 flags + 8 working registers ) x 4 banks
- Stacks : 8 levels
- I/O ports : 41 (Total)
  - High-voltage withstand output ports : 21
  - High-voltage withstand input/output ports : 8
  - Medium-voltage withstand input/output ports : 3
  - Input/output ports : 9
- AD converter (sequential comparison type)
  - 8-bit Accuracy x 8 channels
- Timer : 2 channels
  - Timer 1 (interval timer) : Also used as the PWM DAC and applicable to a divider at melody tone generation.
  - Time base timer for clock generation : 14-level divider on-chipped
- PWM DAC output : Also used as timer 1.
  - 6-bit PWM DAC + 8-bit PWM DAC or 14-bit PWM DAC
- Serial input/output interface (LSB first)
  - 8-bit input/output
- AC zero cross detection circuit
  - The AC zero cross detection circuit is allowed to be internally connected to the PF3/INT0 pin through option data specification.

# LC65404A

- Interrupt function: 5 interrupt sources and 4 vector addresses
  - External interrupt sources: 2
  - Timer interrupt sources: 2
  - Serial input/output interrupt source: 1
- On-chip oscillation stabilization period wait function: Effective at the reset.
- Oscillation circuit: 1 type
  - Main clock: 4.19MHz Crystal oscillation or 4.0MHz Ceramic oscillation
- Standby function: two modes; HALT mode and HOLD mode
- Supply voltage: 3.0V to 6.0V
- Package: DIP-52S
- Evaluation Tools: LC65999 (evaluation chip) + EVA800/850-TB651XX/2XX/3XX/4XX  
LC65PG20X/40X (piggyback)

System Block Diagram



**Development Support**

The development support tools for the LC65404A are as follows:

(1) User's Manual

[LC65204A/404A User's Manual]

(2) Development Tool Manual

[EVA800/850-LC651XX/2XX/3XX/4XX Development Tool Manual]

(3) Development Tools

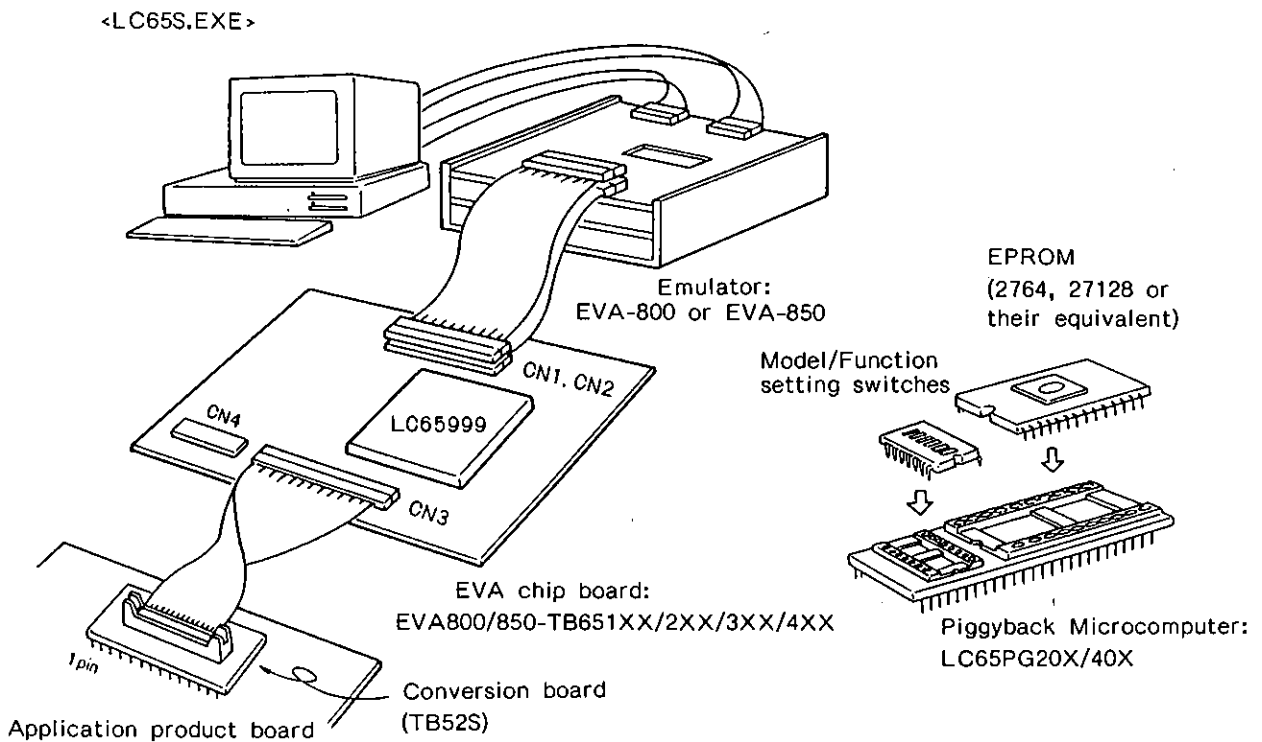
3-1. Program development tools

- i. MS-DOS Host Computer System and Cross Assembler (note 1)
- ii. Cross Assembler --- MS-DOS-based Cross Assembler : LC65S.EXE

3-2. Program evaluation tools

- i. Evaluation Chip: LC65999
- ii. Piggyback Microcomputer : LC65PG20X/40X
- iii. Emulator : EVA-800 main unit and EVA chip board, or EVA-850 main unit and EVA chip board (note 2)

**Outline of the Development Support System**

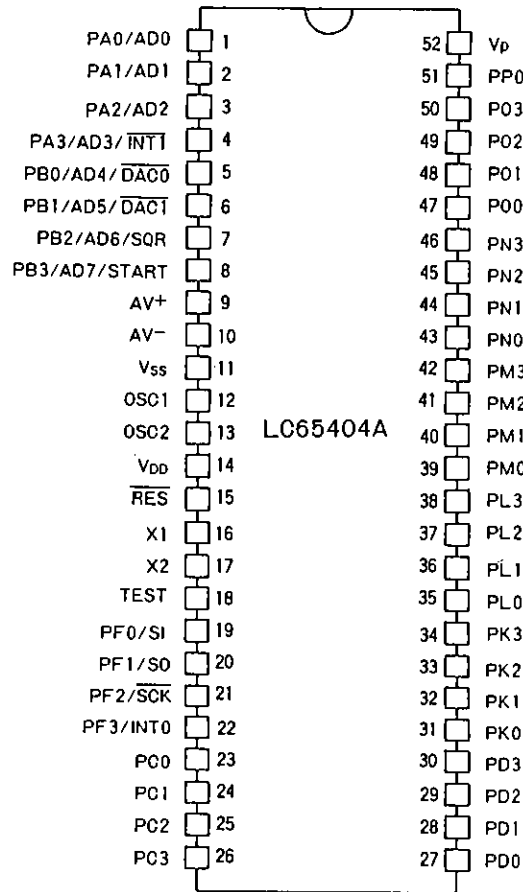


(Note 1) MS-DOS: A trademark of Microsoft Corporation.

(Note 2) The EVA-800 and EVA-850 are general names given to emulators. They are qualified with suffixes (A, B, ...) because the emulators are updated very often. So use the latest version of the emulators by checking the suffixes carefully prior to program debug.

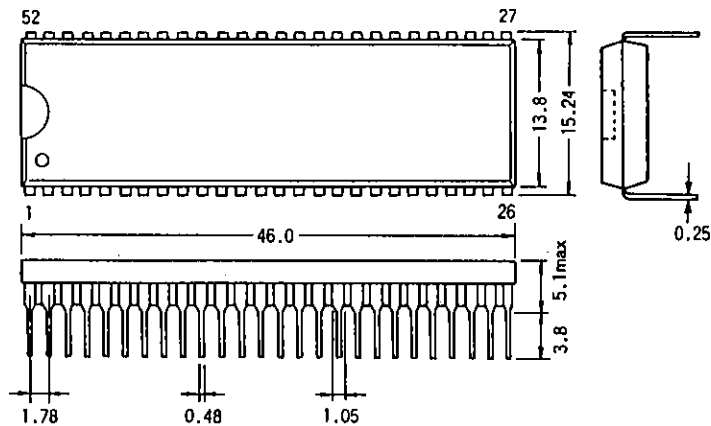
# LC65404A

## LC65404A Pin Assignment



## Package Dimensions : 3128

(unit: mm)



SANYO : DIP52S

## Pin Description

Pin Name	No.Of Pins	I/O	Functional Description	Output Driver	Option	Reset Status	Unused Pin Handling
VDD	1	—	Power supply pin	—	—	—	—
VSS	1	—					
TEST	1	I	LSI test pin. This pin should be connected to the VSS pin during operation and has an internal pull-down resistor.	—	—	—	Always connected to the VSS pin.
RES	1	I	System reset input. This pin has an internal pull-up resistor.	—	—	—	—
AV <sup>+</sup>	1	—	Reference voltage input pin for A/D conversion	—	—	—	Always connected to the VSS pin.
AV <sup>-</sup>	1	—					
OSC1	1	I	Oscillation circuit component pins for system main clock generation. If external clock input is used, leave the OSC2 pin open and connect the external clock generator to the OSC1 pin. Feed-back resistor is internally provided.	—	—	—	—
OSC2	1	O					
X1	1	I	Unusable. Always leave the X2 pin Open and connect the X1 pin to the VDD.	—	—	—	X1: connected to the VDD pin. X2: left OPEN.
X2	1	O					
Vp	1	—	Load power for FLT output internal pull-down resistor	—	—	—	Connected to the VDD pin.
PA0to3	4	I/O	<p>Input/output port pins PA0 to PA3</p> <ul style="list-style-type: none"> <li>- Port function</li> <li>4-bit data input (IP Instruction)</li> <li>4-bit data output (OP Instruction)</li> <li>1-bit input decide operation (BF/BNP instruction)</li> <li>1-bit output set and reset operations (SPB and RPB instructions)</li> <li>- Low-level threshold input</li> <li>- All these four port pins can be used for two or more purposes:</li> </ul> <p>PA0/AD0: Also used as AD converter input pin AD0</p> <p>PA1/AD1: Also used as AD converter input pin AD1</p> <p>PA2/AD2: Also used as AD converter input pin AD2</p> <p>PA3/AD3/INTT: Also used as AD converter input pin AD3 and as external interrupt signal input pin INTT</p>	Normal-voltage withstand Medium-level current type	Each port pin can be set to output type (1) or (2): (1) Open Drain (OD) output (2) Pull-up resistor output	Output transistor OFF (H-level output)	Should be set to the open drain output type and then connected to the VSS pin.
PB0to3	4	I/O	<p>Input/output port pins PB0 to PB3</p> <ul style="list-style-type: none"> <li>- These port pins have the same function as port pins PA0 to PA3.</li> <li>- Low-level threshold Input</li> <li>- All these four port pins can be used for two or more purposes:</li> </ul> <p>PB0/AD4/DAC0: Also used as AD converter input pin AD4 and 6-bit PWM output pin DAC0</p> <p>PB1/AD5/DAC1: Also used as AD converter input pin AD5 and 8-/14-bit PWM output pin DAC1</p> <p>PB2/AD6/SQR: Also used as AD converter input pin AD6 and square waveform signal output pin SQR.</p> <p>PB3/AD7/START: Also used as AD converter input pin AD7 and standby control input pin START</p>	Same as PA0 to PA3	Same as PA0 to PA3	Same as PA0 to PA3	Same as PA0 to PA3.

Continued on next page.

Continued from the preceding page.

Pin Name	No. Of Pins	I/O	Functional Description	Output Driver	Option	Reset Status	Unused Pin Handling
PC0 to 3	4	I/O	Input/output port pins PC0 to PC3 - Same as port pins PA0 to PA3 in function. - High-level threshold input - The output level of these four port pins can be set to 'H' or 'L' by option data at the same time. - FLT segment drive output	VDD-45V High-voltage withstand Medium current type	The output type of each port pin can be set to either (1) or (2) by option data. (1) Open Drain (OD) output (2) Pull-down resistor output Output level specification option: The output level of all the four port pins can be simultaneously set to 'H' or 'L' at the reset by option data.	The output level at the reset can be set to 'H' or 'L' by option data.	Set the pin(s) to the open drain output type by option data and then connect it (or them) to the Vss pin through the resistance of some kohms. In addition, be sure to set the port output level at the reset to 'L'.
PD0 to 3	4	I/O	Input/output port pins PD0 to PD3 - Same as port pins PA0 to PA3 in function and characteristic.	Same as port pins PC0 to PC3	Same as port pins PC0 to PC3	Same as port pins PC0 to PC3	Same as port pins PC0 to PC3
PF0 to 3	4	I/O	Input/output port pins PF0 to PF3 - Same as port pins PA0 to PA3 in function. - Schmitt input - All these four port pins can be used for two purposes: PF0/SI: Also used as 8-bit serial input pin SI. PF1/SO: Also used as 8-bit serial output pin SO. PF2/SCK: Also used as 8-bit serial clock pin SCK PF3/INT0: Also used as external interrupt request input INT0. The AC zero cross detection circuit can be internally added to this pin by option data (AC zero cross interrupt function available).	PF0 to PF2 Open Drain (OD) output type: Withstand voltage +15V Pull-up output type: Normal-voltage withstand PF3 Normal-voltage withstand Medium current type	(1) Output type option: Same as port pins PA0 to PA3. (2) The AC zero cross detection circuit can be internally added to the INT0 pin by option data.	Same as port pins PA0 to PA3	Set the pin(s) to the open drain output type by option data and then connect it (or them) to the Vss pin.
PK0 to 3	4	O	Output port pins PK0 to PK3 - Port functions 4-bit data output (OP Instruction) 1-bit set and reset operation (SPB and RPB instructions) 1-bit decide operation (BP and BNP instructions) - FLT segment drive output	Same as port pins PC0 to PC3	The output type of each port pin can be set to either (1) or (2). (1) Open Drain (OD) output (2) Pull-down resistor output	Output transistor OFF ('L' level output)	Set the pin(s) to the open drain output type by option data and then connect it (or them) to the VDD pin
PL0 to 3	4	O	Output port pins PL0 to PL3 - Same as port pins PK0 to PK3 in function. - FLT digit drive output	VDD-45V High-voltage withstand Large current type	Same as port pins PK0 to PK3	Same as port pins PK0 to PK3	Same as port pins PK0 to PK3
PM0 to 3	4	O	Output port pins PM0 to PM3. - Same as port pins PL0 to PL3 in function and characteristic	Same as port pins PL0 to PL3	Same as port pins PK0 to PK3	Same as port pins PK0 to PK3	Same as port pins PK0 to PK3
PN0 to 3	4	O	Output port pins PN0 to PN3. - Same as port pins PL0 to PL3 in function and characteristic	Same as port pins PL0 to PL3	Same as port pins PK0 to PK3	Same as port pins PK0 to PK3	Same as port pins PK0 to PK3
PO0 to 3	4	O	Output port pins PO0 to PO3. - Same as port pins PL0 to PL3 in function and characteristic	Same as port pins PL0 to PL3	Same as port pins PK0 to PK3	Same as port pins PK0 to PK3	Same as port pins PK0 to PK3
PP0	1	O	Output port pin PP0 - Same as port pins PL0 to PL3 except for 1-bit configuration.	Same as port pins PL0 to PL3	Same as port pins PK0 to PK3	Same as port pins PK0 to PK3	Same as port pins PK0 to PK3

User Option types

1) Oscillation circuit options

The main clock oscillation circuit and the sub clock oscillation circuit can be selected from the following optional circuits:

Option name	Optional oscillation circuit
Main clock oscillation circuit	Two-pin CF oscillation circuit
	Two-pin X'tal (crystal) oscillation circuit
	External clock input
Sub clock oscillation circuit	Unused

2) Output level option

This option is provided to set the output level of input/output ports C and D to either 'H' or 'L' at the reset. This sets the output level of the four pins at the same time.

Option name	Conditions
1. 'H' level output at the reset	Simultaneous 4-bit setting (input/output ports C and D)
2. 'L' level output at the reset	Simultaneous 4-bit setting (input/output ports C and D)

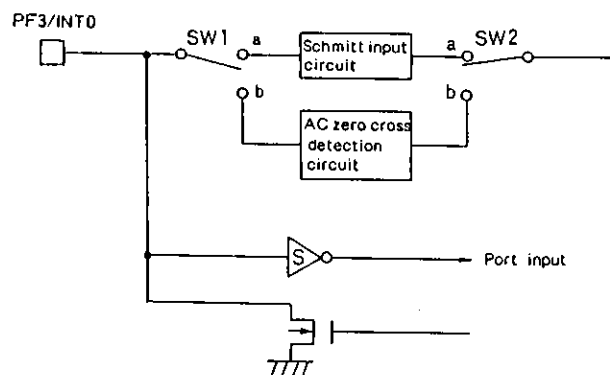
3. Watchdog reset option

The watchdog reset option is used to select the watchdog reset function. Note that the watchdog reset function utilizes the time base timer.

Option name	Conditions
1. Watchdog reset function select	An additional program routine is required in order for the time base interrupt request flag to be reset at a certain interval. This prevents the watchdog reset circuit from being activated in cases but a program upset.
2. Watchdog reset function non-select	—

4) AC zero cross detection input circuit option

The AC zero cross detection input circuit option is used to permit the INT0 pin to internally have an AC zero cross detection circuit or Schmitt input circuit.



Option name \ SW	SW1	SW2
INT0 input	a	a
AC zero cross input	b	b

5) Normal-voltage withstand/Medium-voltage withstand port output type option

This user option is used to allow the output circuit type of each normal-voltage withstand and medium-voltage input/output port pin to be set to either the open drain output or the pull-up resistor output (bit-by-bit setting only).

Option name	Circuit type	Applied ports
Open Drain (OD) output		Ports A, B and F
Pull-up resistor output		Ports A, B and F

6) High-voltage withstand port output type option

This user option is used to allow the output circuit type of each high-voltage input/output and high-voltage output port pin to either the open drain output or the pull-down resistor output (bit-by-bit setting only).

Option name	Circuit type	Applied ports
Open Drain (OD) output		Ports C and D
		Ports K, L, M, N, O and P
Pull-down resistor output		Ports C and D
		Ports K, L, M, N, O and P



LC65404A

Major LC65404A Characteristics

1. Absolute Maximum Ratings at Ta = 25 °C, Vss = 0V

Parameter	Symbol	Applied Pins and Remarks	Conditions	Limits		Unit
				VDD[V]		
Maximum Supply Voltage	VDD max	VDD			-0.3 to +7.0	V
Input Voltage	VI(1)	OSC1	At self-oscillation		Up to the voltage produced	
	VI(2)	TEST, RES, OSC1	OSC1: at external clock input		-0.3 to VDD + 0.3	
	VI(3)	AV+			-0.3 to VDD + 0.3	
	VI(4)	AV-			-0.3 to VDD + 0.3	
	VI(5)	Vp			VDD - 45 to VDD + 0.3	
Output Voltage	VO(1)	OSC2	At self-oscillation		Up to the voltage produced	V
	VO(2)	Ports K, L, M, N, O and port pin P0			VDD - 45 to VDD + 0.3	
Input/output Voltage	VI(1)	Port pins F2 to F0	At open drain output		-0.3 to +15	mA
	VI(2)	Port pins F2 to F0	At pull-up resistor output		-0.3 to VDD + 0.3	
	VI(3)	Ports C and D			VDD - 45 to VDD + 0.3	
	VI(4)	Ports A and B port pin F3			-0.3 to VDD + 0.3	
Peak Output Current	IOP(1)	Ports A, B, and F			-2 to +10	mA
	IOP(2)	Ports L, M, N, O and port pin P0			-30 to 0	
	IOP(3)	Ports C, D and K			-10 to 0	
Average Output Current	IOA(1)	Ports A, B, and F	Average value per pin for 100ms		-2 to +10	mA
	IOA(2)	Ports L, M, N, O and port pin P0			-30 to 0	
	IOA(3)	Ports C, D, and K			-10 to 0	
	ΣIOA(1)	Ports A and B	Total current value of all pins for 100ms		-16 to +80	
	ΣIOA(2)	Port F			-8 to +40	
	ΣIOA(3)	Ports L, M, N, O and port pin P0			-50 to 0	
ΣIOA(4)	Ports C, D and K			-50 to 0		
Maximum Power Dissipation	Pd max	DIP52S	Ta = -30 to +85°C		580	mW
Ambient Operating Temperature	Topr				-30 to +85	°C
Ambient Storage Temperature	Tstg				-55 to +125	

2. Allowable Operating Range at Ta = -30 °C to +85 °C, Vss = 0V

Parameter	Symbol	Applied Pins and Remarks	Conditions	Limits				
				VDD[V]	Min	Typ	Max	Unit
Operating Power Supply Voltage (including a standby mode)	VDD(1)	VDD	0.92 μs ≤ Tcyc < 36 μs		4.5		6.0	V
	VDD(2)	VDD	1.84 μs ≤ Tcyc < 36 μs		4.0		6.0	
	VDD(3)	VDD	29.4 μs ≤ Tcyc < 36 μs		3.0		6.0	
Memory backed-up Power Supply Voltage	VST	VDD	Full standby mode (HOLD mode)		1.8		6.0	V

To be continued on the next page.

LC65404A

Continued from the preceding page.

Allowable Operating Range at Ta = -30 °C to +85 °C, Vss = 0V

Parameter	Symbol	Applied Pins and Remarks	Conditions	Limits			Unit	
				VDD(V)	Min	Typ		Max
Input 'H'-level Voltage	V <sub>IH</sub> (1)	OD type port pins F2 to F0	Output Nch (N-channel) Tr.(transistor)OFF	3.0to6.0	0.80V <sub>DD</sub>		13.5	V
	V <sub>IH</sub> (2)	PU type port pins F2 to F0	Output Nch Tr. OFF	3.0to6.0	0.80V <sub>DD</sub>		V <sub>DD</sub>	
	V <sub>IH</sub> (3)	Ports A and B	Output Nch Tr. OFF	3.0to6.0	1.9		V <sub>DD</sub>	
	V <sub>IH</sub> (4)	Ports C and D	Output Nch Tr. OFF	4.5to6.0	0.80V <sub>DD</sub>		V <sub>DD</sub>	
				3.0to6.0	0.85V <sub>DD</sub>		V <sub>DD</sub>	
	V <sub>IH</sub> (5)	OSC1, START, PF3/INT0, INT1 (Note 1)	See Fig. 3 (applies to OSC1 only). Output Nch Tr. OFF (applies to other pins than OSC1).	3.0to6.0	0.80V <sub>DD</sub>		V <sub>DD</sub>	
V <sub>IH</sub> (6)	RES		1.8to6.0	0.80V <sub>DD</sub>		V <sub>DD</sub>		
Input 'L'-level Voltage	V <sub>IL</sub> (1)	Port pins F2 to F0	Output Nch Tr. OFF	3.0to6.0	V <sub>SS</sub>		0.20V <sub>DD</sub>	V
	V <sub>IL</sub> (2)	Ports A and B	Output Nch Tr. OFF	4.5to6.0	V <sub>SS</sub>		0.5	
				3.0to6.0	V <sub>SS</sub>		0.35	
	V <sub>IL</sub> (3)	Ports C and D	Output Nch Tr. OFF	3.0to6.0	V <sub>SS</sub>		0.40V <sub>DD</sub>	
	V <sub>IL</sub> (4)	TEST		4.5to6.0	V <sub>SS</sub>		0.30V <sub>DD</sub>	
				3.0to6.0	V <sub>SS</sub>		0.25V <sub>DD</sub>	
V <sub>IL</sub> (5)	OSC1, RES, PF3/INT0, INT1 (Note 1)	See Fig. 3 (applies to OSC1 only). Output Nch Tr. OFF (applies to other pins than OSC1).	3.0to6.0	V <sub>SS</sub>		0.20V <sub>DD</sub>		
V <sub>IL</sub> (6)	START		1.8to6.0	V <sub>SS</sub>		0.20V <sub>DD</sub>		
Instruction Cycle Time	T <sub>CYC</sub>		(Note 2)	(Note 2)	0.92		36	μs
Main Clock External Input Conditions	Frequency	F <sub>XOSC</sub>	OSC1	(Note 2)	3.0to6.0	3.6	4.33	MHz
	Pulse Width	T <sub>WOSCCH</sub> T <sub>WOSCCL</sub>		See Fig. 3	4.5to6.0	70		ns
					3.0to6.0	140		
	Rise and Fall Times	T <sub>OSCR</sub> T <sub>OSCF</sub>		See Fig. 3	3.0to6.0			30

(Note 1) This does not apply to the case where the AC zero cross detection circuit has been internally added to the INT0 pin by the user option data.

(Note 2) Frequencies are closely related to power supply voltages and instruction cycle times. So they should be studied in connection with supply voltages and cycle times.

LC65404A

3. Electrical Characteristics at Ta = -30 °C to +85 °C, Vss = 0V

Parameter	Symbol	Applied Pins and Remarks	Conditions	Limits			Unit	
				VDD (V)	Min	Typ		Max
Input 'H'-level Current	I <sub>IH</sub> (1)	OD type port pins F2 to F0	Output Nch (N channel) Tr. (transistor) OFF (including Nch Tr. OFF leakage current). Vin=+13.5V	3.0to6.0			+5.0	μA
	I <sub>IH</sub> (2)	OD type ports A and B, and OD type port pin F3 (including multi-functional port pins INT0, INT1 and START) (Note 1)	Output Nch (N channel) Tr. (transistor) OFF (including Nch Tr. OFF leakage current). Vin=VDD	3.0to6.0			+1.0	
	I <sub>IH</sub> (3)	RES	Vin=VDD	3.0to6.0			+1.0	
	I <sub>IH</sub> (4)	OSC1	Vin=VDD	3.0to6.0			+10	
	I <sub>IH</sub> (5)	OD type ports C and D	Output Pch Tr OFF. Vin = VDD	3.0to6.0		+30	+100	
Input 'L'-level Current	I <sub>IL</sub> (1)	OD type ports A, B and F (including multi-functional port pins INT0, INT1 and START) (Note 1)	Output Nch Tr. OFF. Vin = Vss	3.0to6.0	-1.0			μA
	I <sub>IL</sub> (2)	PU type ports A, B and F (including multi-functional port pins INT0, INT1 and START) (Note 1)	Output Nch Tr. OFF. Vin = Vss	3.0to6.0	-1.0	-0.5		mA
	I <sub>IL</sub> (3)	RES	Vin = Vss	3.0to6.0	-60	-25		μA
	I <sub>IL</sub> (4)	OSC1	Vin = Vss	3.0to6.0	-10			
	I <sub>IL</sub> (5)	OD type ports C and D	Output Pch (P channel) Tr. (transistor) OFF (including Pch Tr. OFF leakage current). Vout = VDD - 40V	3.0to6.0	-30			
Output 'H'-level Voltage	VOH(1)	PU type ports A, B and F	I <sub>OH</sub> = -50 μA	4.5to6.0	VDD-1.2			V
	VOH(2)	PU type ports A, B and F	I <sub>OH</sub> = -10 μA	3.0to6.0	VDD-0.5			
	VOH(3)	Ports L, M, N and O, and port pin P0	I <sub>OH</sub> = -20 mA	4.5to6.0	VDD-2.1			
	VOH(4)	Ports L, M, N and O, and port pin P0	I <sub>OH</sub> = -1.0 mA I <sub>OHs</sub> of other ports < -1mA	3.0to6.0	VDD-1.0			
	VOH(5)	Ports C, D and K	I <sub>OH</sub> = -5 mA	4.5to6.0	VDD-1.8			
	VOH(6)	Ports C, D and K	I <sub>OH</sub> = -1.0 mA I <sub>OHs</sub> of other ports < -1mA	3.0to6.0	VDD-1.0			
Output 'L'-level Voltage	VOL(1)	Ports A, B and F	I <sub>OL</sub> = 5 mA	4.5to6.0			1.5	V
	VOL(2)	Ports A, B and F	I <sub>OL</sub> = 1.0 mA I <sub>OLs</sub> of other ports < 1mA	3.0to6.0			0.5	

To be continued on the next page.

LC65404A

Continued from the preceding page.

Electrical Characteristics at Ta = -30 °C to +85 °C, Vss = 0V

Parameter	Symbol	Applied Pins and Remarks	Conditions	Limits			Unit			
				VDD(V)	Min	Typ		Max		
Output 'L'-level Current (the current produced by pull-down resistors)	IOL	PD type ports C, D, K, L, M, N and O, and PD type port pin P0	Output Pch (P channel) Tr. (transistor) OFF Vout=3.0V Vp=-35V	5.0	190	362	844	μA		
Output OFF Leakage Current	Ioff(1)	OD type ports K, L, M, N and O, and OD type port pin P0	Output Pch (P channel) Tr. (transistor) OFF Vout=VDD	3.0to6.0			30			
	Ioff(2)	OD type ports K, L, M, N and O, and OD type port pin P0	Output Pch (P channel) Tr. (transistor) OFF Vout=VDD-40V	3.0to6.0	-30					
Pull-up MOS Tr. Resistance	Rtru	PU type ports A, B and F	Output Nch (N channel) Tr. (transistor) OFF VIN=0V	5.0	8	12	30	kΩ		
Pull-up resistor	Ru	RES	VIN=0V	5.0	100		400	kΩ		
Pull-down resistor	Rd	PD type ports C, D, K, L, M, N and O, and PD type port pin P0	Output Pch (P channel) Tr. (transistor) OFF Vout=3.0V Vp=-35V	5.0	45	105	200	kΩ		
Hysteresis Voltage	VHYS	Port F and port pins INT0, INTT, RES and START (Note 1)		3.0to6.0		0.1VDD		V		
Serial Clock	Input Clock Cycle	TCKCY(1)	SCK	See Figure 5.	4.0to6.0	0.8		μS		
	Output Clock Cycle	TCKCY(2)	SCK	See Figure 5.	4.0to6.0	2.0X TCYC				
	Input Clock 'L'-level Pulse Width (Note 5)	TCKL(1)	SCK	See Figure 5.	4.0to6.0	0.3				
	Output Clock 'L'-level Pulse Width	TCKL(2)	SCK	See Figure 5.	4.0to6.0	TCYC				
	Input Clock 'H'-level Pulse Width (Note 5)	TCKH(1)	SCK	See Figure 5.	4.0to6.0	0.3				
	Output Clock 'H'-level Pulse Width	TCKH(2)	SCK	See Figure 5.	4.0to6.0	TCYC				
Serial Input	Data Setup Time	TICK	SI	With reference to the rising edge of the SCK signal See Fig. 5.	4.0to6.0	0.2				
	Data Hold Time	TCKI	SI		4.0to6.0	0.2				
Serial Output	Output Delay Time	TCKO	SO	With reference to the falling edge of the SCK signal. External resistance: 1 kohm. External capacitance: 50pF. See Fig. 5.	4.0to6.0		0.5			
Main Clock Self-oscillation Conditions	Crystal Oscillation	Oscillation Frequency	foscx	OSC1 OSC2 (Note 3)	3.0to6.0		4.19		MHz	
		Oscillation Stabilizing Period	tMXS			See Fig. 2			20	ms
	Ceramic Oscillation	Oscillation Frequency	fOSCCF	See Fig. 1. (Note 2)			3.92	4.0	4.08	MHz
		Oscillation Stabilizing Period	tMCFS			See Fig. 3			10	ms

(Note 3) For oscillation constants, refer to Tables 1.

To be continued on the next page.

LC65404A

Continued from the preceding page.

Electrical Characteristics at Ta = -30 °C to +85 °C, Vss = 0V

Parameter	Symbol	Applied Pins and Remarks	Conditions	Limits			Unit			
				VDD(V)	Min	Typ		Max		
AC Zero Cross Detection Input Characteristics	Input Frequency	FZIN	Apply to the case where the AC zero cross detection circuit has been internally added to the PF3/INT0 pin by the user option data.	4.5 to 6.0	40		1000	Hz		
	Input Voltage	VZIN			1.0		2.4	Vp-p		
	Detection Error	VZA			①, ②, ③ 60Hz sine wave signal input			±100	mV	
	Input Current	IHZ			①, ②, ③ VIN=VDD			+40	μA	
		IILZ			①, ②, ③ VIN=VSS			-40		
	Threshold Voltage	VT*ACM			①, ②, ③		0.3VDD	0.7VDD	V	
L-level Input Threshold Voltage	VT*ACL		①, ②, ③			VT*ACM -0.2	V			
Comparator Characteristics (with AD converter in comparator mode)	Comparison Accuracy	VCECON	AD0 to AD7	5.0 ±10%		±1	±2	LSB		
	Threshold Voltage	VTHCON				AV-	AV+	V		
	Input Voltage	VINCON				AV-	AV+			
	Reference Input Voltage	AV+	AV+				AV-		VDD	
		AV-	AV-				VSS	AV+		
	Conversion Time	TCC			Comparator speed 1/1. At 12 x TCYC.		11 (TCYC=0.92μs)	96 (TCYC=8μs)	μs	
			Comparator speed 1/2. At 23 x TCYC.		21 (TCYC=0.92μs)	92 (TCYC=4μs)				
AD Conversion Characteristics (AD converter in A/D mode)	Resolution			5.0 ±10%		8		Bit		
	Absolute Accuracy					±1	±2	LSB		
	Zero Scale Error	EzS					±1			
	Full Scale Error	EFS					±1			
	Conversion Time	TCAD			AD speed 1/1. At 26 x TCYC		24 (TCYC=0.92μs)	208 (TCYC=8μs)	μs	
					AD speed 1/2. At 51 x TCYC.		47 (TCYC=0.92μs)	204 (TCYC=4μs)		
	Reference Input Voltage	AV+	AV+				AV-	VDD	V	
		AV-	AV-				VSS	AV+		
	Reference Input Current Range	IRIF	AV+, AV-		AV+=VDD AV-=VSS		75	150	300	μA
	Analog Input Voltage Range	VAIN	AD0 to AD7				AV-		AV+	V
Analog Port Input Current	IAIN	Port pins AD0 to AD7 (with the output circuit of the input/output multi-functional port pins set to OD type)	Including output OFF leakage current. VAIN=VDD				1	μA		
			VAIN=VSS		-1					

To be continued on the next page.

Continued from the preceding page.

Electrical Characteristics at Ta = -30 °C to +85 °C, Vss = 0V

Parameter	Symbol	Applied Pins and Remarks	Conditions	Limits			Unit	
				VDD(V)	Min	Typ		Max
Dissipated Current in Normal Operation Mode (Note 4)	IDDOP(1)	VDD	4.19MHz x 1/1: High-speed operation mode (TCYC = 0.95 μs).	4.5to6.0		3	6	mA
	IDDOP(2)	VDD	4.19MHz x 1/2: High-speed operation mode (TCYC = 1.9 μs).	4.0to6.0		2	4	
	IDDOP(3)	VDD	4.19MHz x 1/32: Low-speed operation mode (TCYC = 30.5 μs).	3.0		0.3	1	
Dissipated Current in Standby Operation Mode (Note 4)	IDDST(1)	VDD	4.19MHz main clock oscillation (HALT mode)	6.0		0.8	1.5	mA
	IDDST(2)	VDD		3.0		200	500	
Dissipated current in Full standby operation mode (Note 4)	IDDST(3)	VDD	Full standby mode (HOLD mode)	1.8			1	μA
	IDDST(4)	VDD	Full standby mode (HOLD mode)	6.0			10	

(Note 4) The 'dissipated current' does not include the current flowing into the I/O port transistors, pull-up/pull-down resistors.

(Note 5) When the internal clock is used, although according to the specifications TCKL(2) and TCKH(2)(=TCYC) are output from the SCK pin with the minimum clock width, there are cases where their clock widths become shorter than TCYC due to the value of the pull-up resistor. However, it is necessary to select a value for the pull-up resistor so that even at the minimum, these clock widths exceed the 0.3 μs stipulated for TCKL(1) and TCKH(1).

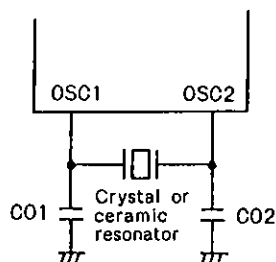


Fig. 1 Main clock oscillation circuit

Table 1. Guaranteed constants for Main clock oscillation

Oscillation type	Supplier	Oscillator	CO1	CO2
4.194304MHz crystal osc	Kinseki	HC-49/U CL=13.2pF	15pF	15pF
	Nippon Denpa	AT-51 CL=16pF	22pF	22pF
4.0MHz ceramic resonator osc	Murata	CSA4.00MG	33pF	33pF
		CST4.00MGW	Not required	Not required
	Kyocera	KBR-4.0MS	33pF	33pF
		KBR-4.0MES	Not required	Not required

CO1 and CO2 tolerance: Within ±10% (including wire capacitance)

CL: Internal load capacitance of a crystal oscillator

\*1: Three-pin (C internally provided) ceramic resonator

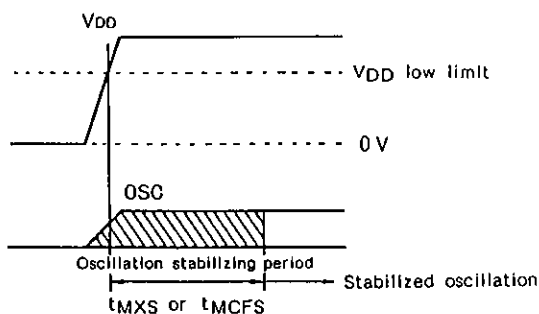


Fig. 2. Main clock oscillation stabilizing period

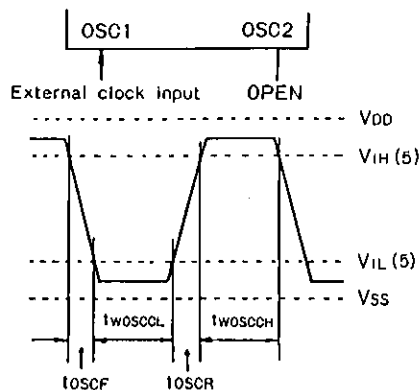
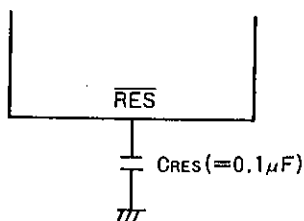


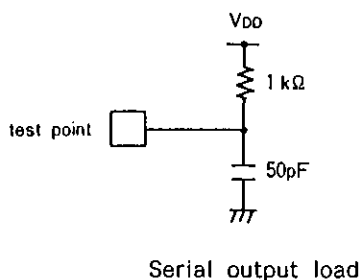
Fig.3. Input waveform of input clock (for main clock)



(Note)  
 If power stabilizing time is zero, the reset time will be 10ms to 100ms with the CRES = 0.1µF.

If the power stabilizing period is rather long, the CRES value should be set properly so that the reset time period can be longer than the main clock oscillation stabilizing period.

Fig. 4. Reset Circuit



Serial output load

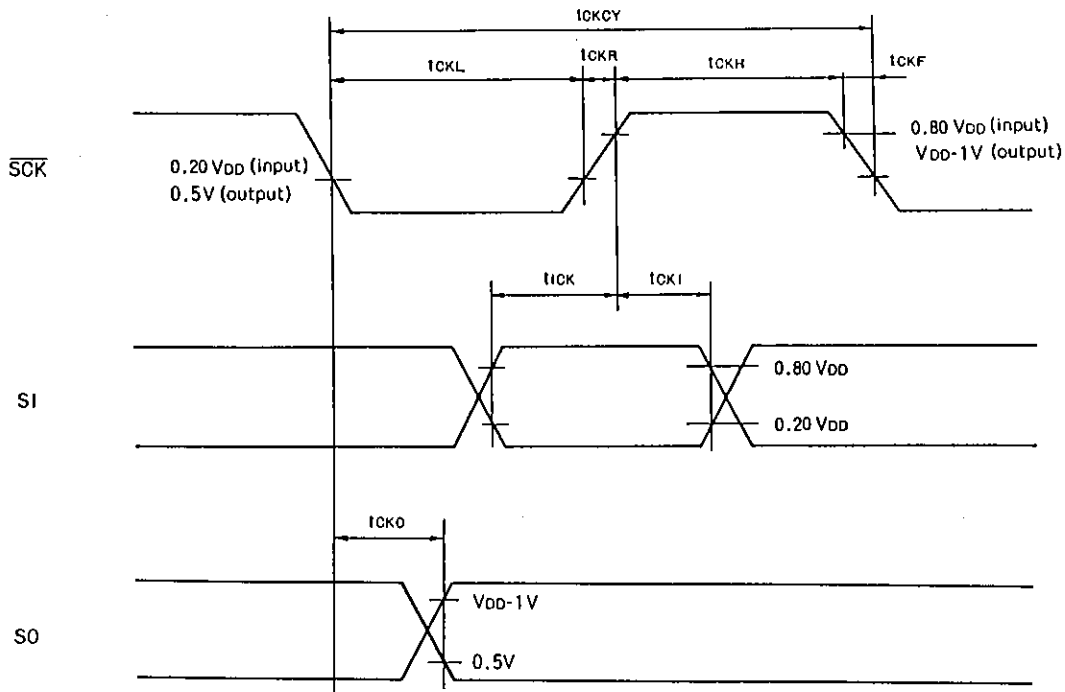
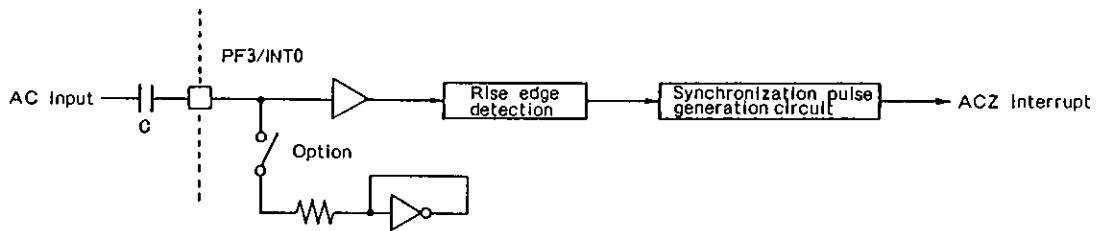
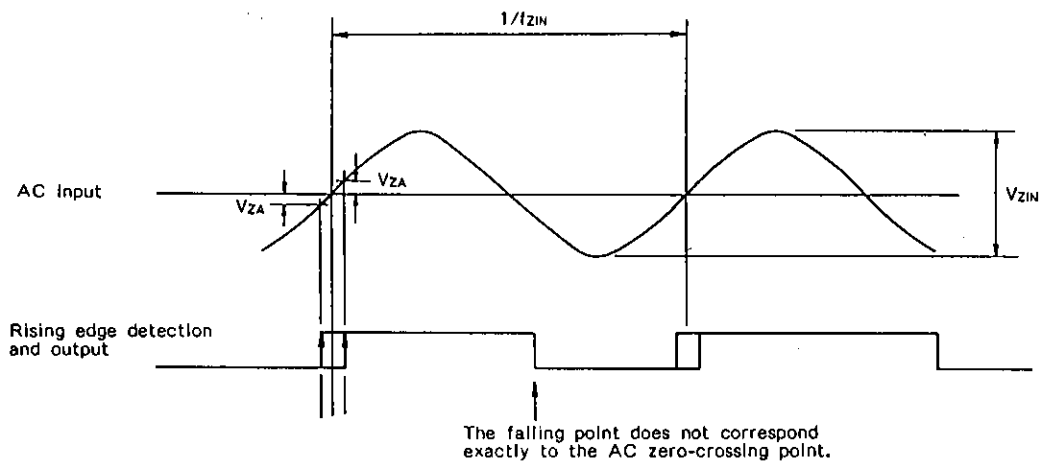


Fig. 5 Serial clock timing



<AC zero cross detection>



<AC zero cross timing>

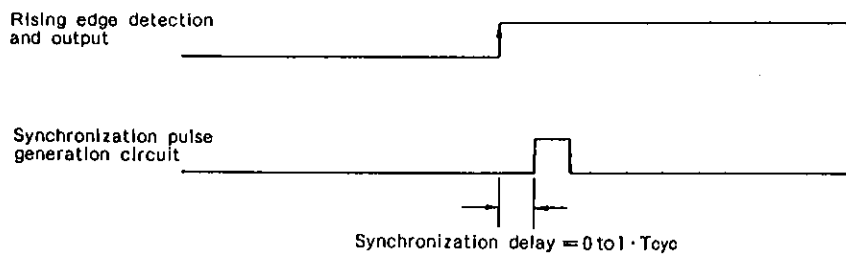


Fig. 6 AC zero cross detection



LC65404A

LC65404A Instruction Set (by Function)

Convention  
 AC : ACcumulator PC : Program Counter  
 ACt : ACcumulator bit t STACK : STACK register  
 CF : Carry Flag bAt, bHa, bLa : Working register  
 CTL : ConTrol register bLa : Working register  
 MSTEN : MaSTerinterrupt ENable flag ZF : Zero Flag  
 DP : Data Pointer ( ) [ ] : Indicates the content.  
 E : E register ← : Transfer operation and its direction  
 bFn : Flag bit n + : Addition  
 M : Memory - : Subtraction  
 M (DP) : Memory address specified by DP ^ : And  
 P (DP<sub>L</sub>) : Input/output port specified by DPL V : Or  
 GP (DP) : Pseudo port specified by DP ∨ : Exclusive Or

Instruction group Type	Mnemonic	Operation Code		Bytes	Cycles	Operations	Operating Description	Affected STS flag(s)	Remarks
		D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub>	D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>						
Accumulator Manipulation Instructions	CLA	Clear AC	1 1 0 0	0 0 0 0	1	1	AC ← 0	ZF	* 1
	CLC	Clear Cf	1 1 1 0	0 0 0 1	1	1	CF ← 0	CF	
	STC	Set CF	1 1 1 1	0 0 0 1	1	1	CF ← 1	CF	
	CMA	Complement AC	1 1 1 0	1 0 1 1	1	1	AC ← $\overline{AC}$	ZF	
	INC	Increment AC	0 0 0 0	1 1 1 0	1	1	AC ← (AC) + 1	ZF CF	
	DEC	Decrement AC	0 0 0 0	1 1 1 1	1	1	AC ← (AC) - 1	ZF CF	
	RAL	Rotate AC left through CF	0 0 0 0	0 0 0 1	1	1	AC <sub>0</sub> ← (CF), AC <sub>n+1</sub> ← (AC) <sub>n</sub> , CF ← (AC) <sub>3</sub>	ZF CF	
	TAE	Transfer AC to E	0 0 0 0	0 0 1 1	1	1	E ← (AC)		
	XAE	Exchange AC with E	0 0 0 0	1 1 0 1	1	1	(AC) ↔ (E)		
Memory Manipulation Instructions	INM	Increment M	0 0 1 0	1 1 1 0	1	1	M(DP) ← (M(DP)) + 1	ZF CF	
	DEM	Decrement M	0 0 1 0	1 1 1 1	1	1	M(DP) ← (M(DP)) - 1	ZF CF	
	SMB bit	Set M data bit	0 0 0 0	1 0 B <sub>1</sub> B <sub>0</sub>	1	1	M(DP, B <sub>1</sub> B <sub>0</sub> ) ← 1		
	RMB bit	Reset M data bit	0 0 1 0	1 0 B <sub>1</sub> B <sub>0</sub>	1	1	M(DP, B <sub>1</sub> B <sub>0</sub> ) ← 0	ZF	
Operation and Compare Instructions	AD	Add M to AC	0 1 1 0	0 0 0 0	1	1	AC ← (AC) + (M(DP))	ZF CF	
	ADC	Add M to AC with CF	0 0 1 0	0 0 0 0	1	1	AC ← (AC) + (M(DP)) + (CF)	ZF CF	
	DAA	Decimal adjust AC in addition	1 1 1 0	0 1 1 0	1	1	AC ← (AC) + 6	ZF	
	DAS	Decimal adjust AC in subtraction	1 1 1 0	1 0 1 0	1	1	AC ← (AC) + 10	ZF	
	EXL	Exclusive or M to AC	1 1 1 1	0 1 0 1	1	1	AC ← (AC) ∨ (M(DP))	ZF	
	AND	And M to AC	1 1 1 0	0 1 1 1	1	1	AC ← (AC) ∧ (M(DP))	ZF	
	OR	Or M to AC	1 1 1 0	0 1 0 1	1	1	AC ← (AC) ∨ (M(DP))	ZF	
	CM	Compare AC with M	1 1 1 1	1 0 1 1	1	1	(M(DP)) + (AC) + 1	ZF CF	
	CI data	Compare AC with immediate data	0 0 1 0 0 1 0 0	1 1 0 0 1 3 1 2 1 1 0	2	2	1 3 1 2 1 1 0 + (AC) + 1	ZF CF	
	CLI data	Compare DPL with immediate data	0 0 1 0 0 1 0 1	1 1 0 0 1 3 1 2 1 1 0	2	2	(DPL) ∨ 1 3 1 2 1 1 0	ZF	
Load and Store Instructions	LI data	Load AC with Immediate data	1 1 0 0	1 3 1 2 1 1 0	1	1	AC ← 1 3 1 2 1 1 0	ZF	* 1
	S	Store AC to M	0 0 0 0	0 0 1 0	1	1	M(DP) ← (AC)		
	L	Load AC from M	0 0 1 0	0 0 0 1	1	1	AC ← (M(DP))	ZF	
	XM data	Exchange AC with M then modify DPH with immediate data	1 0 1 0	0 M <sub>2</sub> M <sub>1</sub> M <sub>0</sub>	1	2	(AC) ↔ (M(DP)) DP <sub>n</sub> ← (DP <sub>n</sub> ) ∨ 0 M <sub>2</sub> M <sub>1</sub> M <sub>0</sub>	ZF	Whether or not ZF is affected depends on the result of exclusive-Oring between (DP <sub>n</sub> ) and 0 M <sub>2</sub> M <sub>1</sub> M <sub>0</sub> .
	X	Exchange AC with M	1 0 1 0	0 0 0 0	1	2	(AC) ↔ (M(DP))	ZF	Whether or not ZF is affected depends on the DPH content at the time when the instruction is executed.
	XI	Exchange AC with M then increment DPL	1 1 1 1	1 1 1 0	1	2	(AC) ↔ (M(DP)) DPL ← (DPL) + 1	ZF	Whether or not ZF is affected depends on the DPL increment.
	XD	Exchange AC with M then decrement DPL	1 1 1 1	1 1 1 1	1	2	(AC) ↔ (M(DP)) DPL ← (DPL) - 1	ZF	Whether or not ZF is affected depends on the DPL decrement.
RTBL	Read table data from program ROM	0 1 1 0	0 0 1 1	1	2	AC, E ← ROM (PCh, E, AC)			

Instruction group type	Mnemonic	Operation Code		Bytes	Cycles	Operations	Operating Description	Affected STS flag(s)	Remarks	
		D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub>	D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>							
Data Pointer Manipulation Instructions	LDZ data	Load DPH with Zero and DPL with immediate data respectively	1 0 0 0	13 12 11 10	1	1	DPH ← 0 DPL ← 13 12 11 10	Loads zero and immediate data 13121110 into DPH and DPL, respectively.		
	LHI data	Load DPH with immediate data	0 1 0 0	13 12 11 10	1	1	DPH ← 13 12 11 10	Loads immediate data 13121110 into DPH.		
	IND	Increment DPL	1 1 1 0	1 1 1 0	1	1	DPL ← (DPL) + 1	Increments DPL content by 1.	ZF	
	DED	Decrement DPL	1 1 1 0	1 1 1 1	1	1	DPL ← (DPL) - 1	Decrements DPL content by 1.	ZF	
	TAL	Transfer AC to DPL	1 1 1 1	0 1 1 1	1	1	DPL ← (AC)	Transfers AC content to DPL.		
	TLA	Transfer DPL to AC	1 1 1 0	1 0 0 1	1	1	AC ← (DPL)	Transfers DPL content to AC.	ZF	
	XAH	Exchange AC with DPH	0 0 1 0	0 0 1 1	1	1	(AC) ↔ (DPH)	Exchanges the contents of AC and DPH.		
	XAI	Exchange AC with working register bA <sub>i</sub>	1 1 1 0	11 10 0 0 0 0	1	1	(AC) ↔ (bA0)	Exchanges the contents of AC and a specified working register in register bank b (already selected). Note that bits t <sub>1</sub> and t <sub>0</sub> are used to specify working registers bA0, bA1, bA2 and bA3.		
	XAO		1 1 1 0	0 1 0 0	1	1	(AC) ↔ (bA1)			
	XA2		1 1 1 0	1 0 0 0	1	1	(AC) ↔ (bA2)			
XA3	1 1 1 0		1 1 0 0	1	1	(AC) ↔ (bA3)				
XHa	Exchange DPH with working register bH <sub>a</sub>	1 1 1 1	1 1 0 0	1	1	(DPH) ↔ (bH0)	Exchanges the contents of DPH and a specified working register in register bank b (already selected). Note that bit a is used to specify working registers bH0 and bH1.			
XHO		1 1 1 1	1 1 0 0	1	1	(DPH) ↔ (bH1)				
XLa	Exchange DPL with working register bL <sub>a</sub>	1 1 1 1	0 1 0 0	1	1	(DPL) ↔ (bL0)	Exchanges the contents of DPL and a specified working register in register bank b (already selected). Note that bit a is used to specify working registers bL0 and bL1.			
XLO		1 1 1 1	0 1 0 0	1	1	(DPL) ↔ (bL1)				
SRBA	Set Register Bank Address	1 1 1 1	0 0 1 0	1	1	RBF ← 1110 of SB	Sets the bank value given by the SB instruction in the register bank flag.			
Flag Manipulation Instructions	SFB flag	Set flag bit	0 1 0 1	B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>	1	1	bFn ← 1	Sets a specified flag in register bank b (already selected). Note that immediate data B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> is used to specify the flags.		
	RFB flag	Reset flag bit	0 0 0 1	B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>	1	1	bFn ← 0	Resets a specified flag in register bank b (already selected). Note that immediate data B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> is used to specify the flags.	ZF	Flags are divided into 16 groups: 0F3 to 0F0, 3F4 to 3F7, 3F11, 3F12 to 3F15. Whether ZF is set or reset depends on the content of the 4-bit group to which a specified flag belongs.
Jump and Subroutine Instructions	JMP addr	Jump in the current bank	0 1 1 0	1 P <sub>10</sub> P <sub>9</sub> P <sub>8</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	2	2	PC ← PC11 or (inverted PC11) P <sub>10</sub> P <sub>9</sub> P <sub>8</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	Makes program jump to the address specified by PC11 (or inverted PC11) and immediate data P <sub>10</sub> P <sub>9</sub> P <sub>8</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> .		If executed immediately after the BANK instruction, the current bank value will be changed (bit PC11 is inverted).
	JPEA	Jump in the current page modified by E and AC	1 1 1 1	1 0 1 0	1	1	PC <sub>7:10</sub> ← (E, AC)	Replaces lower-order 8 bits of PC with E and AC and then jumps to the address specified by the new PC content.		
	CZP addr	Call subroutine in the zero page	1 0 1 1	P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	1	1	STACK ← (P0) + 1 PC <sub>11:10</sub> , PC <sub>10:9</sub> ← 0 PC <sub>5:10</sub> ← P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	Calls a subroutine in page 0 of bank 0.		
	CAL addr	Call subroutine in the zero bank	1 0 1 0	1 P <sub>10</sub> P <sub>9</sub> P <sub>8</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	2	2	STACK ← (P0) + 2 PC <sub>11:10</sub> ← 00 P <sub>10</sub> P <sub>9</sub> P <sub>8</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	Calls a subroutine in bank 0.		
	RT	Return from subroutine	0 1 1 0	0 0 1 0	1	1	PC ← (STACK)	Returns to main routine from a subroutine.		
	RTI	Return from interrupt routine	0 0 1 0	0 0 1 0	1	1	PC ← (STACK) CF ZF ← CSF, ZSF	Returns to main routine from an interrupt servicing routine.	ZF CF	
	BANK	Change bank	1 1 1 1	1 1 0 1	1	1	PC <sub>11</sub> ← (PC <sub>11</sub> ) QP(DP)	Specifies new ROM banks or pseudo ports.		
	SB	Set bank	0 1 1 0	0 1 1 0	1	1	RBF ← 110	Specifies working register and flag banks.		
Branch Instructions	BAl addr	Branch on AC bit	0 1 1 1	0 0 1 1 0 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	2	2	PC <sub>7:10</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if (AC) = 1	Makes program branch to a specified address in the same page if a specified AC bit is set to 1. Note that immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> is used to specify addresses and another immediate data 110 used to specify AC bit.		The mnemonic will change from BA0 to BA3 depending on the value of immediate data t10.
	BNAI addr	Branch on no AC bit	0 0 1 1	0 0 1 1 0 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	2	2	PC <sub>7:10</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if (AC) = 0	Makes program branch to a specified address in the same page if a specified AC bit is reset to 0. Note that immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> is used to specify addresses and another immediate data 110 used to specify the desired bit.		The mnemonic will change from BNA0 to BNA3 depending on the value of immediate data t10.
	BMI addr	Branch on M bit	0 1 1 1	0 1 1 1 0 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	2	2	PC <sub>7:10</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if (MDP, t10) = 1	Makes program branch to a specified address in the same page if a specified M(DP) bit is set to 1. Note that immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> is used to specify addresses and another immediate data 110 used to specify the desired bit.		The mnemonic will change from BM0 to BM3 depending on the value of immediate data t10.
	BNMI addr	Branch on no M bit	0 0 1 1	0 1 1 1 0 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	2	2	PC <sub>7:10</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if (MDP, t10) = 0	Makes program branch to a specified address in the same page if a specified M(DP) bit is reset to 0. Note that immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> is used to specify addresses and another immediate data 110 used to specify the desired bit.		The mnemonic will change from BNMI0 to BNMI3 depending on the value of immediate data t10.
	BPi addr	Branch on Port bit	0 1 1 1	1 0 1 1 0 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	2	2	PC <sub>7:10</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if ((DPL, t10) = 1 or ((DP, t10) = 1	Makes program branch to a specified address in the same page if a specified port (DP) or pseudo port (DPL) bit is set to 1. Note that immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> is used to specify addresses and another immediate data 110 used to specify the desired bit.		The mnemonic will change from BP0 to BP3 depending on the value of immediate data t10.
	BNPi addr	Branch on no Port bit	0 0 1 1	1 0 1 1 0 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	2	2	PC <sub>7:10</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if ((DPL, t10) = 0 or ((DP, t10) = 0	Makes program branch to a specified address in the same page if a specified port (DP) or pseudo port (DPL) bit is reset to 0. Note that immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> is used to specify addresses and another immediate data 110 used to specify the desired bit.		The mnemonic will change from BNPI0 to BNPI3 depending on the value of immediate data t10.

Instruction group type	Mnemonic	Operation Code		Bytes	Cycles	Operations	Operating Description	Affected STS flag(s)	Remarks	
		D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub>	D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>							
Branch instructions	BC addr	Branch on CF	0 0 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 1 0 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7100</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> If CF = 1	Makes program branch to a specified address in the same page if CF is set. Note that immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> is used to specify addresses.		
	BNC addr	Branch on no CF	0 0 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 1 1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7100</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> If CF = 0	Makes program branch to a specified address in the same page if CF is reset. Note that immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> is used to specify addresses.		
	BZ addr	Branch on ZF	0 1 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 1 0 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7100</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> If ZF = 1	Makes program branch to a specified address in the same page if ZF is set. Note that immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> is used to specify addresses.		
	BNZ addr	Branch on no ZF	0 0 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 1 0 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7100</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> If ZF = 0	Makes program branch to a specified address in the same page if ZF is reset. Note that immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> is used to specify addresses.		
	BFn addr	Branch on flag bit	1 1 0 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7100</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> If bFn = 1	Makes program branch to a specified address in the same page if a specified flag bit (one of the 16 flag bits) in register bank b (already selected) is set. Note that immediate data n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub> is used to specify the desired flag bit and another immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> is used to specify the desired address.		The mnemonic changes from BFO to BF15 according to the values of n.
	BNZ addr	Branch on no flag bit	1 1 0 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7100</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> If bFn = 0	Makes program branch to a specified address in the same page if a specified flag bit (one of the 16 flag bits) in register bank b (already selected) is reset. Note that immediate data n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub> is used to specify the desired flag bit and another immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> is used to specify the desired address.		The mnemonic changes from BFO to BF15 according to the values of n.
Input/output instructions	IP	Input port to AC	0 0 0 0	1 1 0 0	1	1	AC ← [P(DPL)] or [GP(DP)]	Inputs data to AC from the port P(DPL) or pseudo port GP(DP).	ZF	
	OP	Output AC to port	0 1 1 0	0 0 0 1	1	1	P(DPL) or --(AC) GP(DP)	Outputs data to the port P(DPL) or pseudo port GP(DP) from AC.		
	SPB bit	Set port bit	0 0 0 0	0 1 B <sub>1</sub> B <sub>0</sub>	1	2	P(DPL,B1B0) ← 1 or GP(DP, B1B0)	Sets a specified bit of the port P(DPL) or pseudo port GP(DP). Note that immediate data B1B0 is used to specify the desired port bit.		If executed, the content of the E register will be destroyed.
	RPB bit	Reset port bit	0 0 1 0	0 1 B <sub>1</sub> B <sub>0</sub>	1	2	P(DPL,B1B0) ← 0 or GP(DP, B1B0)	Resets a specified bit of the port P(DPL) or pseudo port GP(DP). Note that immediate data B1B0 is used to specify the desired port bit.	ZF	If executed, the content of the E register will be destroyed.
Other instructions	SCTL bit	Set control register bit	0 0 1 0 1 0 0 0	1 1 0 0 B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>	2	2	CTL, B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> ← 1 or MSTEN ← 1	Sets a specified bit of the control register (individual interrupt enable flag) or the master interrupt enable flag. Note that immediate data B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> is used to specify the desired bit.		* 2
	RCTL bit	Reset control register bit	0 0 1 0 1 0 0 1	1 1 0 0 B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>	2	2	CTL, B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> ← 0 or MSTEN ← 0	Resets a specified bit of the control register (individual interrupt enable flag) or the master interrupt enable flag. Note that immediate data B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> is used to specify the desired bit.	ZF	* 2
	HALT	Halt	1 1 1 1	0 1 1 0	1	1	Hold	Places the chip in the standby mode.		
	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	The CPU runs idle for one machine cycle.		

\*1: If two or more LI or CLA instructions are executed continuously, only the first instruction will be executed normally. However, the instructions following the first will be handled as the NOP instructions.

\*2: B3B2B1B0 = 0000B to 1000B

On the LC65404A user mask option code specification

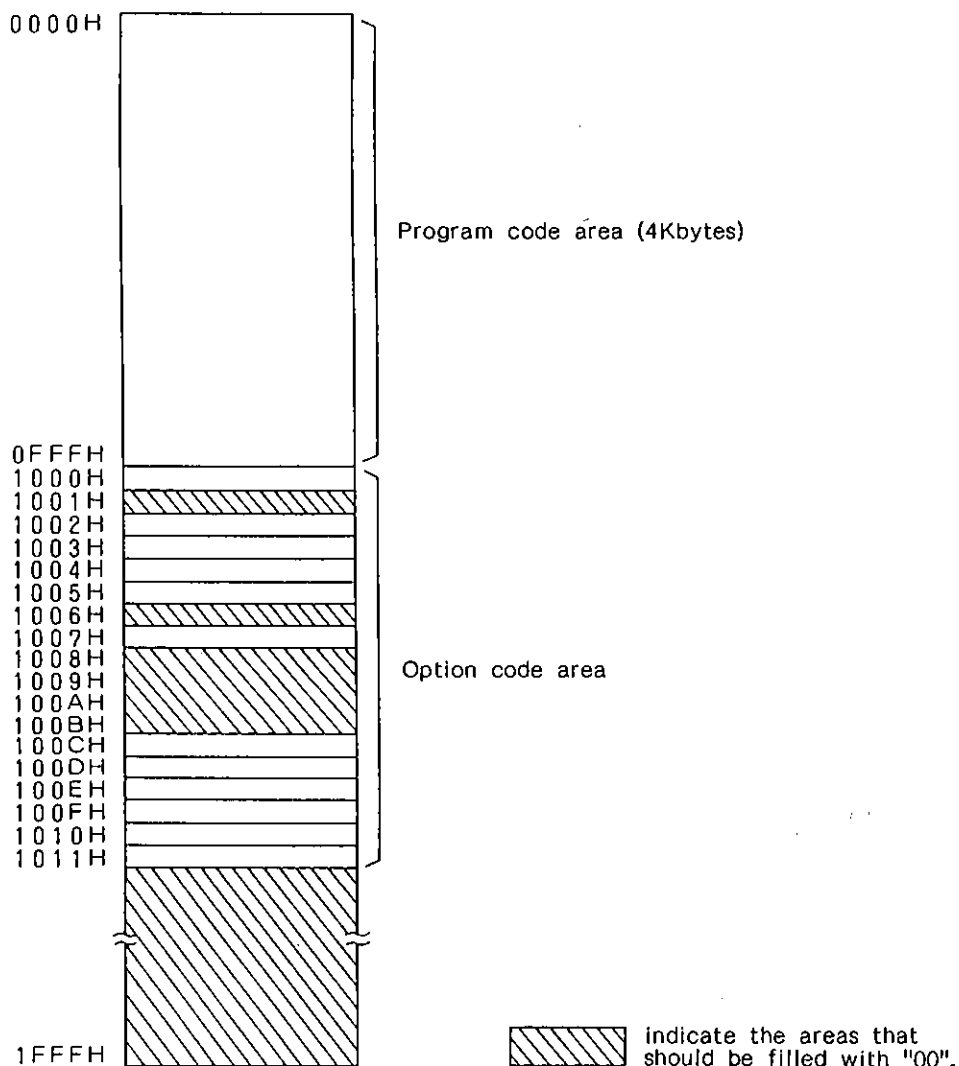
Overview

The user mask option data for the LC65404A should be stored to an EPROM as well as program code and then sent to Sanyo.

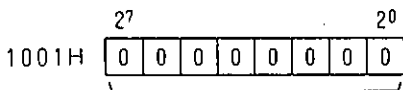
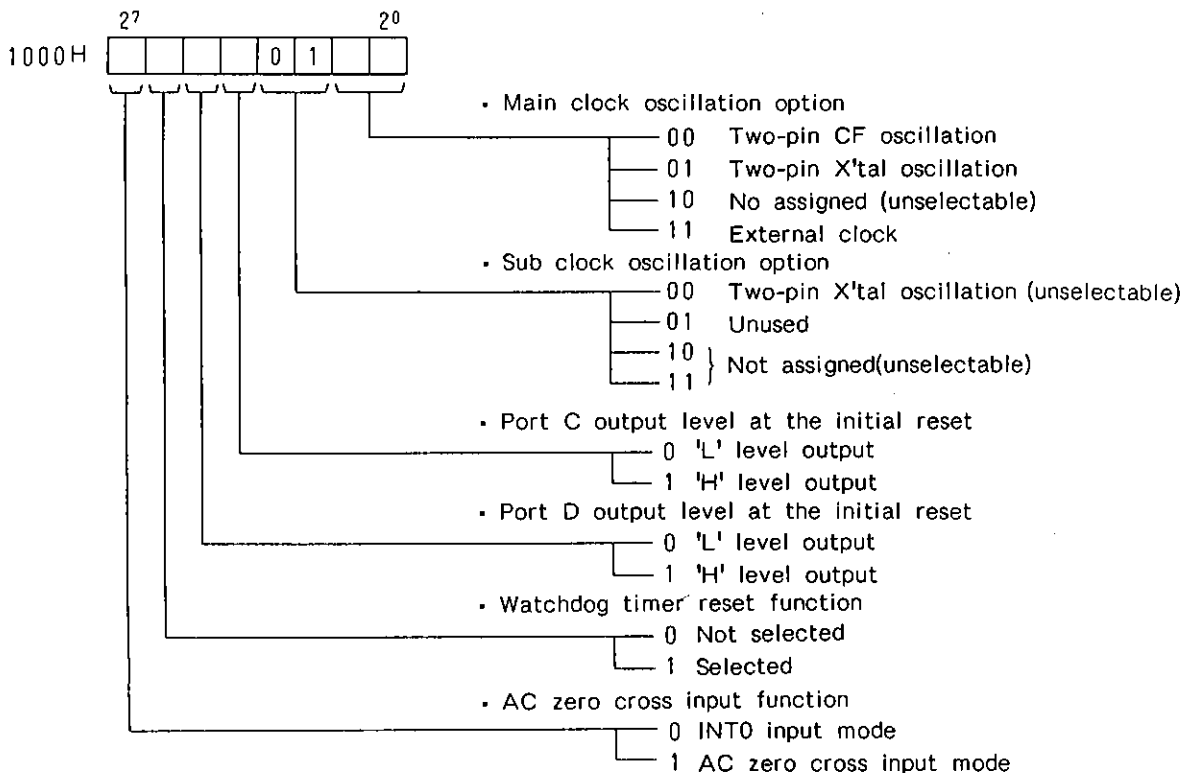
With the Sanyo cross assembler for the LC65404A, the user is allowed to specify option codes in the conversation mode and the user option data can be set in an EPROM properly with ease.

If the Sanyo cross assembler is not used, the option code should be specified in the following manner (this corresponds to the format of the cross assembler):

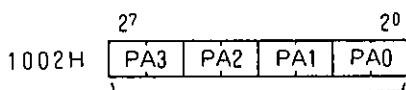
EPROM address map



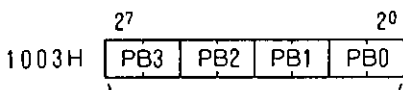
Contents of User option codes



These bits should always be set to '0'.



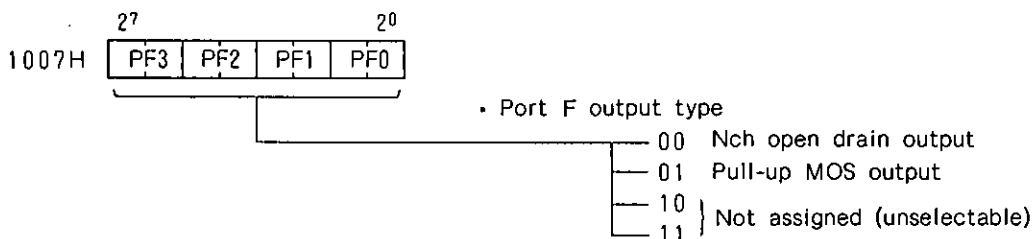
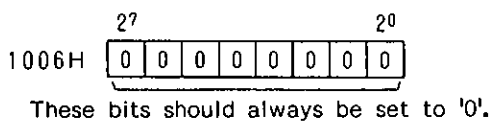
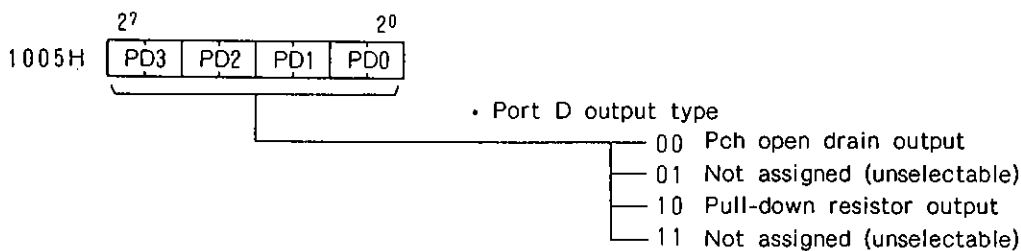
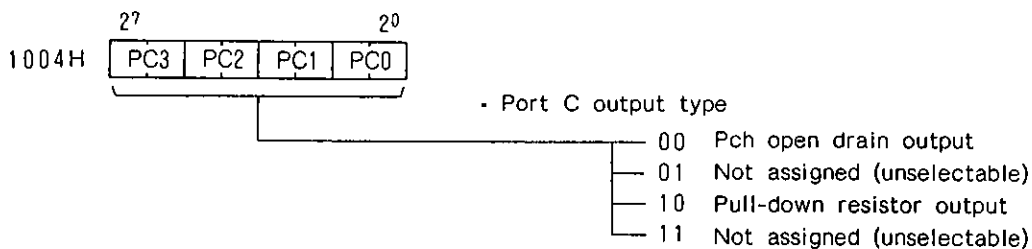
- Port A output type
  - 00 Nch open drain output
  - 01 Pull-up MOS output
  - 10 } No assigned (unselectable)
  - 11 }



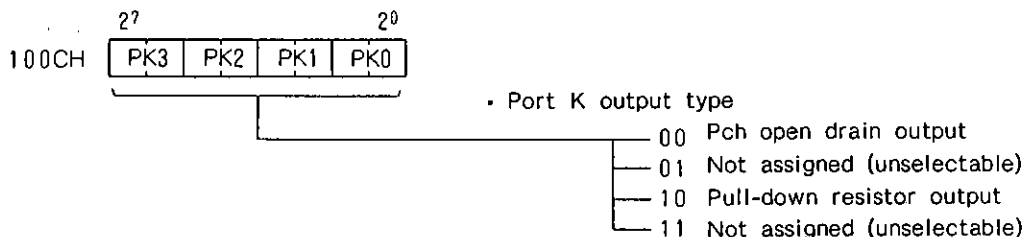
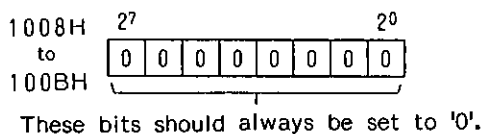
- Port B output type
  - 00 Nch open drain output
  - 01 Pull-up MOS output
  - 10 } Not assigned (unselectable)
  - 11 }

To be continued on the next page.

Continued from the preceding page.

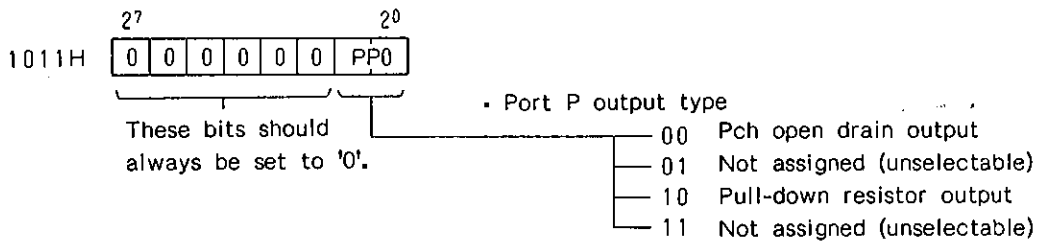
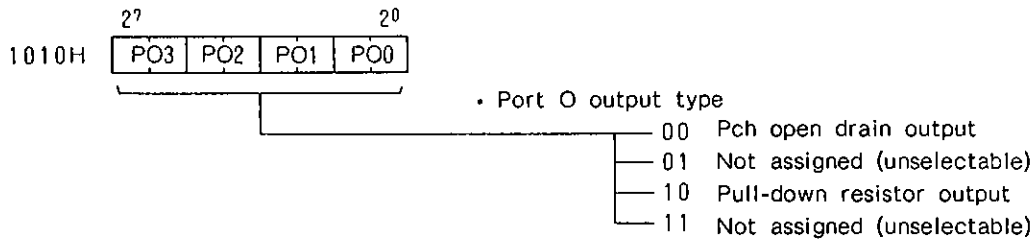
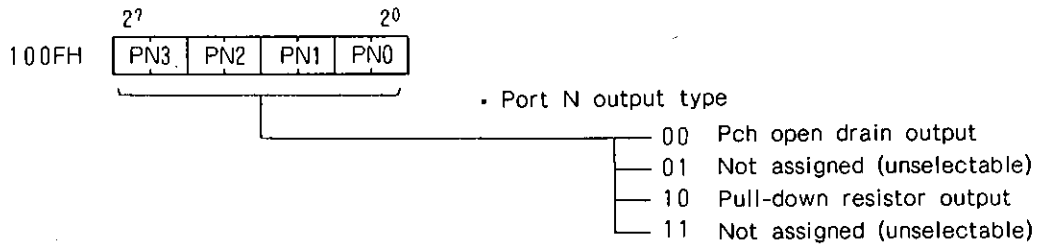
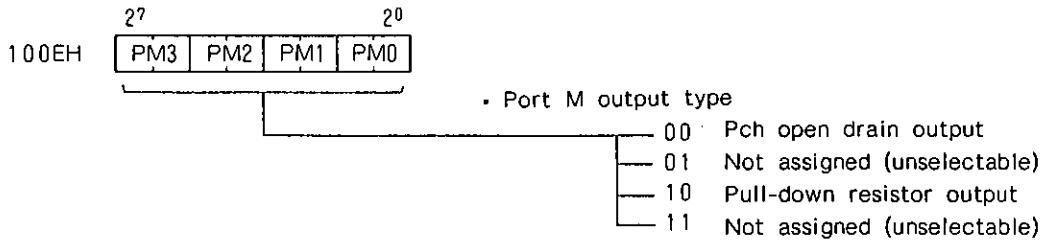
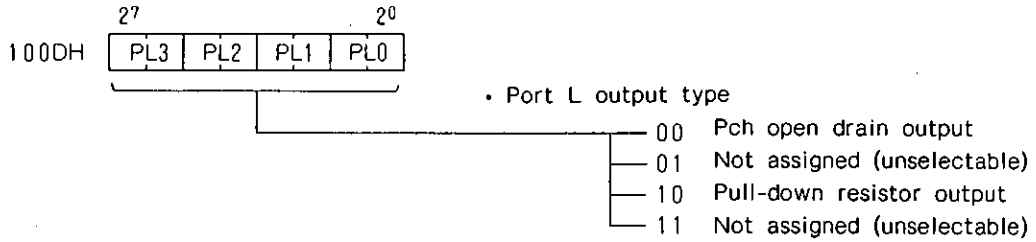


(Note) Be sure to set the output type of the PF3 port pin to OD if the AC zero cross input mode has been selected with the AC zero cross input option.



To be continued on the next page.

Continued from the preceding page.



# LC65404A

## Programming Considerations

- The user application programs for the LC65404A should be developed with the following considerations in mind.

	Item	Functions	Consideration										
System Clock Function	System clock mode	<p>The LC65404A allows the user to select the desired system clock source from the following three by software.</p> <p>① Main clock 1/1 mode (TCYC= 0.95 <math>\mu</math>s)                      ② Main clock 1/2 mode (TCYC = 1.90 <math>\mu</math>s)                      ③ Main clock 1/32 mode (TCYC = 30.6 <math>\mu</math>s)</p> <p>(Note) Main clock = 4.19MHz</p>	<ul style="list-style-type: none"> <li>The main clock oscillation is always required at the system start-up.</li> </ul>										
	System clock switching	<p>The desired system clock mode can be selected by writing data to the clock mode flag (CMF: 2 bits) of the system clock control register as shown below:</p> <table border="1" style="margin: 10px auto; border-collapse: collapse;"> <thead> <tr> <th style="width: 5%;">CMF</th> <th style="width: 95%;">System clock mode</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Main clock 1/32 mode (at the reset)</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Main clock 1/1 mode</td> </tr> <tr> <td style="text-align: center;">2</td> <td>Main clock 1/2 mode</td> </tr> <tr> <td style="text-align: center;">3</td> <td>Unusable</td> </tr> </tbody> </table>	CMF	System clock mode	0	Main clock 1/32 mode (at the reset)	1	Main clock 1/1 mode	2	Main clock 1/2 mode	3	Unusable	<ul style="list-style-type: none"> <li>When the current system clock mode needs to be changed, the user should confirm that the main clock oscillation has become stabilized or that the MCSTP flag has been set to '0' in the external clock input mode.</li> <li>The current system clock mode will be switched to the desired mode in 64 cycles (64/fMOSC, Max.) after the CMF flag is set properly. If the user wants the LC65404A to enter a standby mode after the system clock switching, the above switching time period should be kept in mind. That is, the user should execute the HALT instruction after the switching time elapses.</li> </ul>
	CMF	System clock mode											
0	Main clock 1/32 mode (at the reset)												
1	Main clock 1/1 mode												
2	Main clock 1/2 mode												
3	Unusable												
Main clock control (oscillation stop/start)	<p>The main clock oscillation should be started by setting the MCSTP flag of the system clock control register to "0" (at the reset).</p>	<ul style="list-style-type: none"> <li>Be sure not to set the MCSTP to '1'. If it is set to '1', the main clock oscillation will stop. As a result, the microcomputer will operate abnormally.</li> </ul>											
Standby Function	HALT mode start/release	<p>&lt;Start&gt;                      The HALT mode will be started if the HALT instruction is executed with the SLPF flag of the standby control register set to '0'. Note that the instruction will be processed as the NOP instruction if one of the following conditions is satisfied.</p> <p>-----</p> <p>&lt;Release&gt;                      (1) Reset                      (2) The PB3/START pin is set to 'H' with the WG2 = 1.                      (3) The interrupt release signal becomes active with the WG3 = 1.                      (4) Time base overflow</p>	<ul style="list-style-type: none"> <li>If the HALT mode needs to be released based on the PB3/START pin level ('H') or the interrupt release signal, the WG2 or WG3 flag must be set prior to the execution of the HALT instruction.</li> </ul>										
	HOLD mode start/release	<p>&lt;Start&gt;                      The HOLD mode will be started if the HALT instruction is executed with the SLPF = 1.</p> <p>-----</p> <p>&lt;Release&gt;                      (1) Reset                      (2) The PB3/START pin is set to 'H' with the WG1 = 1.</p>	<ul style="list-style-type: none"> <li>Execute one NOP instruction before issuing the HALT instruction to place the microcomputer in the HOLD mode.</li> <li>If the HOLD mode needs to be released based on the PB3/START pin level, it should be confirmed that the WG1 flag is set and the active oscillation clock (either main clock x 1/128) is used as the time base source clock prior to the execution of the HALT instruction.</li> </ul>										

To be continued on the next page.



Continued from the preceding page.

Item	Functions	Consideration
Watchdog reset (only in case when the optional watchdog function has been selected)	The watchdog reset function uses the time base timer to allow program upset and watchdog reset.	<ul style="list-style-type: none"> <li>• The routine must be included in the user application program in order to reset the TBF flag within a certain fixed time (maximum time base timer overflow cycle). In this case, be sure not to overlap the time base interrupt request signal timing with the TBF flag reset timing.</li> <li>• The active oscillation clock should be used as the time base clock source.</li> <li>• If the time base interrupt request flag (TBF) is set to '1' prior to the HALT mode activation, the HALT mode will be released due to the time base overflow signal and at the same time the watchdog reset signal becomes active. In order to prevent the watchdog reset at the HALT mode release, ① reset the TBF immediately before executing the HALT instruction or ② set the time base interrupt enable flag (TBEN) and the HALT release enable flag (WG3: release due to the interrupt) before executing the HALT instruction.</li> </ul>
Interrupt Enable flag (control register: 5 bits)	<ul style="list-style-type: none"> <li>• Five flags are provided to control the five interrupt sources on one-to-one basis. To enable a certain interrupt request, its corresponding interrupt enable flag must be set. (For this purpose, the SCTL0 to SCTL7 instructions can be used. Note that multiple flag bits cannot be accessed at the same time.)</li> <li>• All the interrupt enable flags are reset at the system reset.</li> </ul>	<ul style="list-style-type: none"> <li>• No flag is reset after interrupt processing terminates. In resetting a certain flag, issue the RCTL instruction to that flag.</li> <li>• All the flags are reset at the HOLD mode start. Set the desired flag after the HOLD mode is released.</li> </ul>
Interrupt request flag	<ul style="list-style-type: none"> <li>• Five interrupt request flags are provided to the five interrupt sources on an one-to-one basis. These flags are assigned to a pseudo port. To reset the flag bits, data is loaded to the AC (Accumulator) by the 'BANK + IP' instructions and then output to the port by the 'BANK + OP' instructions. Note that any bit cannot be set. The data bit that corresponds to the flag bit to be reset should be set to '0' and the remaining data bits should be set to '1'. This data should be first set in the AC and then output to the interrupt request register by the 'BANK + OP' instructions.</li> <li>• At the reset, all the flags except for the timer 1 interrupt request flag (TMIF) are set to all '0'.</li> <li>• The SIOF is reset the moment when the serial data transfer is started.</li> </ul>	<ul style="list-style-type: none"> <li>• No flag is reset after interrupt processing terminates. Every time when a certain interrupt processing is performed, be sure to reset the flag that corresponds to the interrupt source. Note that if the interrupt request flag needs to be reset, it should be confirmed that the master interrupt enable flag, and at the same time the individual interrupt enable flag that corresponds to that interrupt source are both reset or either one is reset.</li> <li>• All the flags are reset at the HOLD mode start-up.</li> <li>• Be sure not to issue the 'BANK + SPB/RPB' instructions to the interrupt request register.</li> </ul>

LC65404A

Considerations on Program Evaluation

- The application programs for the LC65404A should be evaluated on the evaluation chip (LC65999 or LC65PG20X/40X) with the following considerations in mind.

Item type	Item	Function		Consideration
		Production chip	EVA chip	
Function Settings	RAM capacity	RAM capacity of 256 x 4 bits	The desired RAM capacity can be selected by using the RC and RC2 pins.	Set the RC and RC2 pins properly in accordance with the production chip RAM capacity.
	Stack levels	8 levels	The desired stack level can be set by the STC pin.	Set the STC pin properly in accordance with the production chip setting.
	Output type of ports C and D	Pch high-voltage withstand input/output	The circuit type of ports C and D can be set to the Pch high-voltage withstand input/output or the Nch medium-voltage withstand input/output by the C/FLSEL pin.	Set the C/FLSEL pin properly in accordance with the production chip circuit type.
Optional functions	Oscillation circuit	Connect the desired oscillator with pins OSC1 and OSC2.	If the EVA chip board is used for program evaluation, the desired oscillator can be selected by using the jump switch on the board. The simulation chip has the same optional selection as the production chip.	[EVA chip board] Set the jumper switch properly in accordance with the production chip option setting. [simulation chip] Connect the same oscillation as that of the production chip to pins OSC1, OSC2.
	Output level of ports C and D at the reset	4-bit simultaneous select. The output level of all the four bits of the port C or D can be set to the 'H' or 'L' at the same time.	Port C can set to the 'H' or 'L' by the CHL pin while port D by the DHL pin.	Set the CHL and DHL pins properly in accordance with the production chip option setting.
	Watchdog reset function	The watchdog reset function based on the time base timer can be selected.	The watchdog function can be activated or inactivated by using the WDC pin.	Set the WDC pin properly in accordance with the production chip option setting.
	AC zero cross detection circuit	The AC zero cross detection circuit can be internally added to the PF3/INT0 pin.	The AC zero cross detection circuit can be internally activated by the ACZ/INT0 pin.	Set the ACZ/INT0 pin properly in accordance with the production chip option setting.
	Port output type: PU and OD	The output type of each port pin can be set to the PU or OD (on a single-bit manipulation basis).	No pull-up resistor output can be selected. All the port pins are set to the Nch OD output type.	[EVA chip board] Connect the 10kohm of external resistor to the target port. [Simulation chip] Connect a resistor to the target port of the user application board.
	PU resistor	This resistor is used with the port pin that enters the high impedance state (HI-Z OFF) at the 'L'-level output.	Since this is a resistor externally added, the impedance level remains unchanged at the 'L' level output.	On the production chip, only the leakage current flows into the Pch Tr. at the 'L' output. However, please note that the current flow continues through the pull-up resistor on the EVA chip.
	Port output type: PD and OD	The output type of each port pin can be set to the OD or PD (on a single-bit manipulation basis).	No pull-down resistor can be selected. All the port pins are set to the Pch OD output type.	[EVA chip board] Connect the 100kohm of external resistor to the target port. [Simulation chip] Connect the external resistor to the target port of the user application board. Note that the user application board should have its own load power supply.

To be continued on the next page.

Continued from the preceding page.

Item type	Item	Function		Consideration
		Production Chip	EVA Chip	
Oscillation	Main clock oscillation constant	[Crystal oscillation] and [Ceramic oscillation] If the guaranteed constant listed in this catalog is used, the standard oscillation frequency is produced.	[Crystal oscillation] and [Ceramic oscillation] The EVA chip differs from the production chip in oscillation circuit design and characteristics. In addition, the oscillation may be unstable due to wire capacitance.	[Crystal oscillation] and [Ceramic oscillation] External constants should be fine-adjusted according to the evaluation environment.
	Oscillation frequencies of main clock	The oscillation frequency characteristics are shown in this catalog.	The EVA chip differs from the production chip in circuit design and characteristics.	The detailed evaluation should be performed on the ES and CS.
Electrical Characteristics	Operation current and Standby current	The current characteristics are shown in this catalog.	The EVA chip differs from the production chip in circuit design and characteristics.	The standby current cannot be evaluated in detail. However, the standby function can be confirmed in the manner as shown in the manual. Be sure to check the standby function in that way. The characteristics should be evaluated in detail on the EC and CS.
	Operating power supply voltage	The operating power supply voltage range is shown in this catalog.	The power supply voltage range is limited to the range for the EPROM and other LSIs.	The EVA chip should operate in the operating power supply voltage range of $V_{DD}=5V \pm 5\%$ . The operating voltage range of the EPROM and other LSIs should not be exceeded. This means that the functions in the entire operating range of the production chip cannot be evaluated.
	Operating ambient temperature	The operating ambient temperature is shown in this catalog.	Guaranteed temperature range: 10 °C to 40 °C	The operating temperature range of the EVA chip and the simulation chip should be from 10 °C to 40 °C.
Function	ROM capacity	The LC65404A has the 4Kbyte ROM. This means that the JMP and BANK + JMP instructions allow program to jump to the entire ROM area. Note that the SB + JMP instructions cannot be used.	Up to 8Kbytes of ROM can be externally added to the chip. The SB + JMP, BANK + JMP and JMP instructions allow program to jump to the entire ROM area.	It should be confirmed that the application program size is less than 4K bytes.

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
  - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
  - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.