HD155017T

Built-in 1.9 GHz / 650 MHz High Speed Prescaler Dual PLL Frequency Synthesizer IC

HITACHI

ADE-207-240 (Z)
Preliminary
1st. Edition
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Description

The HD155017T is a dual PLL frequency synthesizer IC that was developed for mobile telecommunication systems. The HD155017T includes built-in two channels prescaler up to 1.9 GHz and 650 MHz, which can form a dual PLL system when VCOs and external loop filters are added.

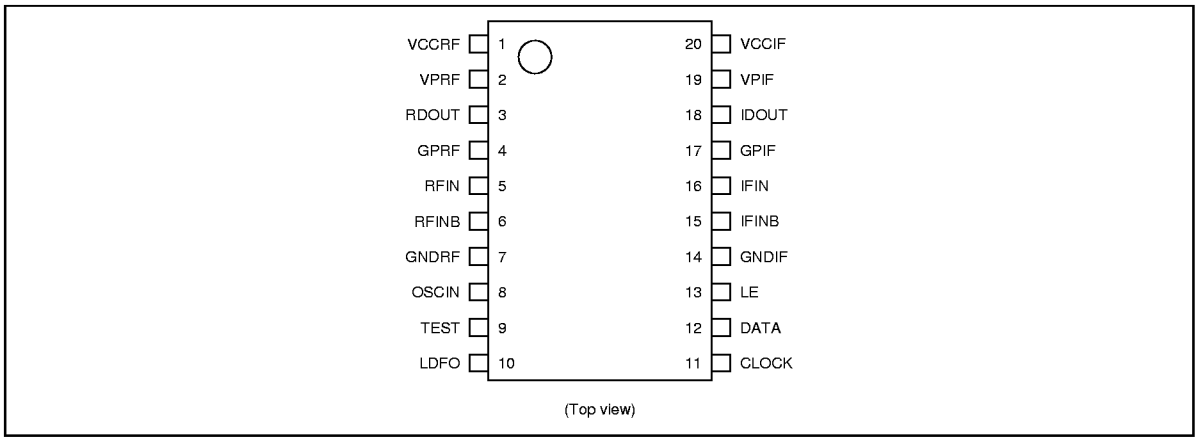
Functions

- Dual-modulus pulse swallow type PLL frequency synthesizer
- RF and IF dual PLL (1.9 GHz / 650 MHz)
- Power saving mode (synchronized for phase detect timing)
- Devision ratios and mode of operation set by a serial command interface
- Built-in constant current type charge pump circuit
- Alternative (High & Low) charge pump current
- Built-in MOS switch for fast lock-up

Features

- High speed prescaler (RFIN Max = 1.9 GHz, IFIN Max = 650 MHz)
- Prescaler input sensitivity
  - RFIN : –15 dBm (@1700 MHz)
  - IFIN : –15 dBm (@400 MHz)
- Charge pump current (4 mA / 9 mA Typ)
- TSSOP-20 (Thin Shrink Small Outline Package) miniature package

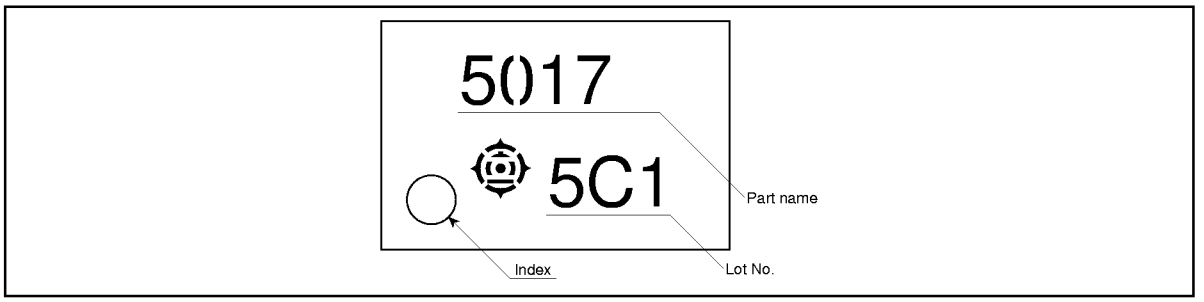
Pin Arrangement



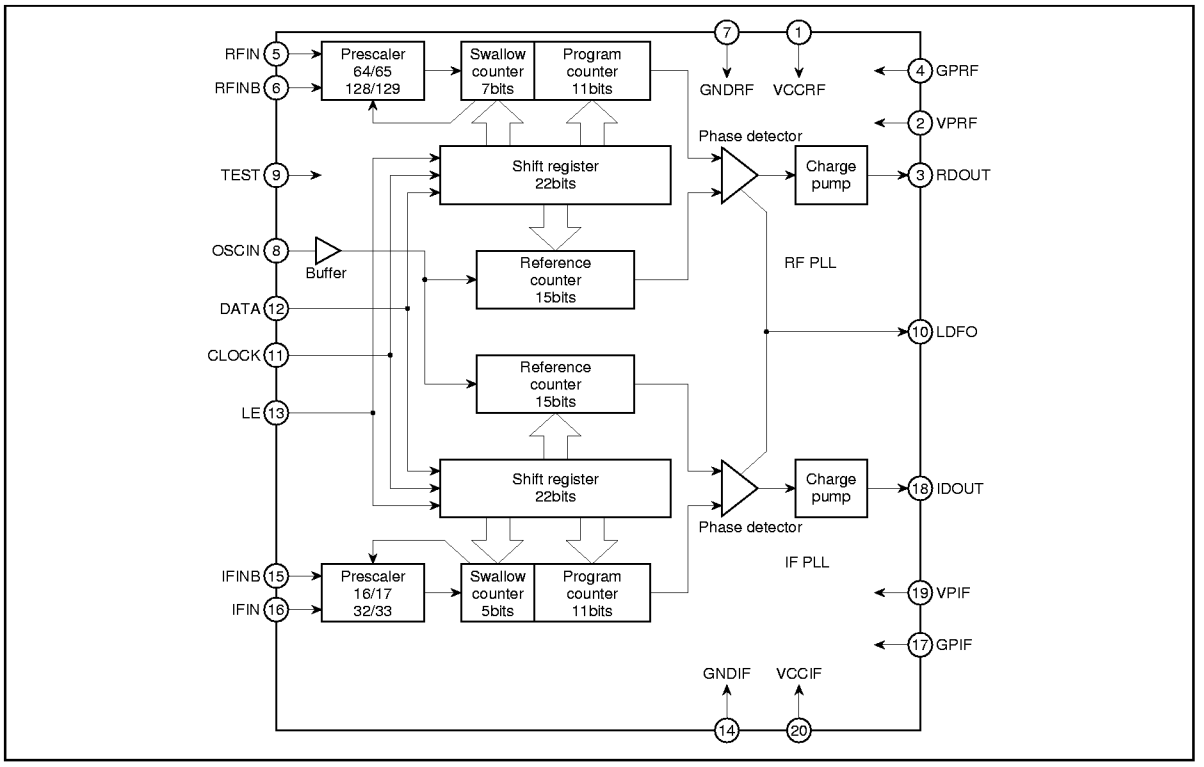
Pin Functions

Pin No.	Pin Name	I/O	Function	Pin Characteristics
1	VCCRF		RF power supply	
2	VPRF		RF charge pump power supply	
3	RDOUT	Output	RF charge pump output	Analog
4	GPRF		RF charge pump ground	
5	RFIN	Input	RF prescaler input	Analog
6	RFINB	Input	RF prescaler differential input	Analog
7	GNDRF		RF ground	
8	OSCIN	Input	Reference oscillator input	Analog
9	TEST	Input	Test pin (normally not connected)	Pull down
10	LDFO	Output	Lock detection/counter monitor output	Open drain
11	CLOCK	Input	Command synchronous clock input	CMOS
12	DATA	Input	Command data input	CMOS
13	LE	Input	Command enable input	CMOS
14	GNDIF		IF ground	
15	IFINB	Input	IF prescaler differential input	Analog
16	IFIN	Input	IF prescaler input	Analog
17	GPIF		IF charge pump ground	
18	IDOUT	Output	IF charge pump output	Analog
19	VPIF		IF charge pump power supply	
20	VCCIF		IF power supply	

Marking Specification



Block Diagram



Functional Description

Genaral Description of the PLL Frequency Synthesizer Operation

The HD155017T is a dual modulus pulse swallow type PLL frequency synthesizer IC. The following is a brief, general description of a PLL synthesizer's operation. In a PLL system, the phase detector compares the phase of a reference oscillator signal with the phase of a Voltage Controlled Oscillator (VCO). The output of the phase detector is fed back to the VCO through the loop filter. Thus the PLL synthesizes the desired frequency.

The following equation shows the relationship between the OSCIN frequency and VCO frequency when the PLL is locked.

$$f_{OSCIN} / N = f_{FIN} / M$$

where f_{OSCIN}: reference oscillator frequency, f_{FIN}: prescaler input frequency, N: division ratio for OSCIN signal, M: division ratio for prescaler input.

In order to obtain the desired frequency from this PLL, counters are needed, which are used to set the division ratio. Usually, a high frequency counter is realized by using bipolar ECL cells. It is very difficult, however, to realize such complicated logic with only ECL cells. To overcome this difficulty, dual modulus pulse swallow architecture as shown in figure 1 is adopted. The prescaler which has a division ratio of K+1 or K is implemented with ECL since it has to handle the high frequency signals. The rest of the circuit including the control circuit which selects prescaler division ratio accordingly is constituted of CMOS logic.

The explanation of the operation of this counter, based on figure 1, is as follows. The high frequency VCO output is fed into the prescaler. The output signal of the prescaler is the input for both the swallow and program counters. The initial values of the counters are loaded from the corresponding data registers by the overflow signal of the program counter. The prescaler immediately starts dividing the input signal with the division ratio, K+1, until it receives the overflow signal from the swallow counter. On receipt of the swallow counter's overflow signal, the prescaler switches its division ratio from K+1 to K. The program counter continues its operation until it overflows, which reloads both the swallow and program counters. The counters repeat above described operation.

Consequently, the overall division ratio of this program counter is :

$$M = (K + 1) \times SWL + K \times (PRG - SWL) = (K \times PRG) + SWL$$

where SWL: Swallow counter register value, PRG: Program counter register value.

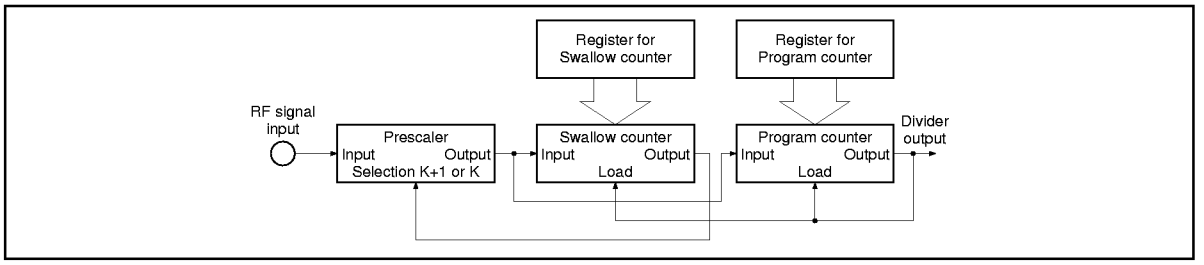


Figure 1 Counter Structure of Dual Modulus Pulse Swallow PLL Frequency Synthesizer

Setting the Register Values

The HD155017T includes a pair of dual modulus pulse swallow type PLL frequency synthesizers. The register settings can be derived from the following formulas.

1. RF PLL
   a) When the RF prescaler division ratio is 128/129 :
      $f_{RFIN} = f_{OSCIN} \times (PRG \times 128 + SWL) / REF$
   b) When the RF prescaler division ratio is 64/65 :
      $f_{RFIN} = f_{OSCIN} \times (PRG \times 64 + SWL) / REF$
2. IF PLL
   a) When the IF prescaler division ratio is 32/33 :
      $f_{IFIN} = f_{OSCIN} \times (PRG \times 32 + SWL) / REF$
   b) When the IF prescaler division ratio is 16/17 :
      $f_{IFIN} = f_{OSCIN} \times (PRG \times 16 + SWL) / REF$

Each RF PLL and IF PLL cases, f_{RFIN}, f_{IFIN} and f_{OSCIN} indicate the RF and the IF VCO frequencies and the reference oscillator frequency, respectively. PRG, SWL and REF are the division ratios of the program, swallow and the reference counters, respectively. Note that PRG must be larger than SWL, and that if the prescaler division ratio is 64, SWL must be less than 64. If the prescaler division ratio is 32, SWL must be less than 32. Similarly, if the prescaler division ratio is 16, SWL must be less than 16.

Setting the Operating Mode

The operating modes of the HD155017T, as shown in table 1, are set by the register bits which are not used to set the division ratios. In other words, the serial data through the 'DATA' pin determines the operating mode as well as division ratio. Each operating mode is described below.

Table 1 Setting the HD155017T Operating Mode

Setting Bit	Operating Mode
RC = H	Charge pump output is High impedance
RC = L	Charge pump Normal mode
IC = H	Charge pump current = ±9.0mA
IC = L	Charge pump current = ±4.0mA
FC = H	POS (VCO is positive polarity)
FC = L	NEG (VCO is negative polarity)
PS = H	Power saving mode
PS = L	Active mode
PR = H	Prescaler division ratio setting (RF : 128/129, IF : 32/33)
PR = L	Prescaler division ratio setting (RF : 64/65, IF : 16/17)

a) FO, LD

These bits determine the output function of LDFO as shown in table 2.

Table 2 Setting the LDFO Pin

FO of RF	FO of IF	LD of RF	LD of IF	LDFO Pin Output Signal
FO = L	FO = L	LD = L	LD = L	No output (GND level output)
FO = L	FO = L	LD = L	LD = H	IF lock detection output
FO = L	FO = L	LD = H	LD = L	RF lock detection output
FO = L	FO = L	LD = H	LD = H	RF and IF lock detection output (Logical AND)
FO = L	FO = H	—	LD = L	IF reference counter overflow pulse output
FO = L	FO = H	—	LD = H	IF program counter overflow pulse output
FO = H	FO = L	—	LD = L	RF reference counter overflow pulse output
FO = H	FO = L	—	LD = H	RF program counter overflow pulse output
FO = H	FO = H	LD = L	LD = L	Fast lock mode selection
FO = H	FO = H	LD = L	LD = H	(Not users application)
FO = H	FO = H	LD = H	LD = L	(Not users application)
FO = H	FO = H	LD = H	LD = H	(Not users application)

b) RC

This bit sets the state of RDOUT and IDOUT, which are the charge pump outputs. If RC is set 'H', RDOUT and IDOUT become high impedance. If this mode is chosen after lock detection, it is possible to modulate the VCO signal with a low frequency signal without reducing the bandwidth of the loop filters.

However, careful consideration with regard to the stability of the oscillation frequency of the VCO is necessary, since no phase lock loop is available in this mode.

c) IC

This bit selects the charge pump output current capability. When "high current mode" is selected, the charge pump can supply 2.25 times greater current than in "low current mode". Usually the high current mode is selected during lock-up to speed up the process. Once the loop is locked, the mode should be switched to "low current mode" to suppress the spurious. In applying this mode, the stability of the phase lock loop should be closely examined because of the closed loop gain difference between high and low current modes. The HD155017T has a MOS switch connected to LDFO to be used for fast lock up mode of RF PLL. This MOS switch is also controlled by the IC bit. Please refer to "Fast Lock-up Mode" for more detailed description.

d) FC

This bit sets the polarity of the phase detector. If the control characteristics of the VCO is such that the oscillation frequency increases as control voltage increases, then this bit must be 'H'. If it is vice-versa, then FC must be 'L'. (See figure 2)

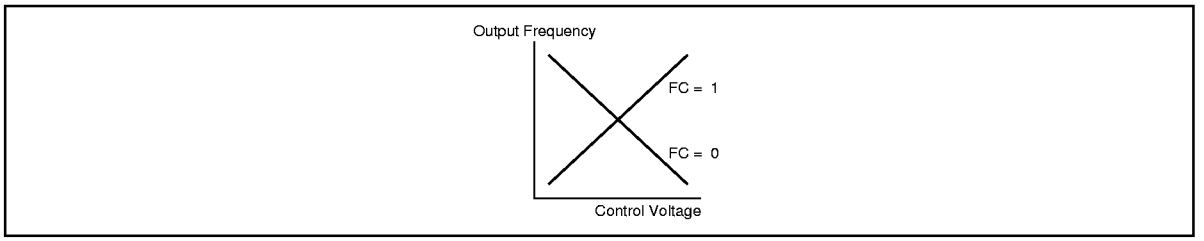


Figure 2 Relationship between VCO Characteristics and FC Setting

e) PS

The PS bit controls the power saving mode. If both the RF and IF synthesizers are set to power saving mode, OSCIN is shut down, and the HD155017T stops operating completely. Please refer to 'Power Saving Mode' for a more detailed explanation.

f) PR

The PR bit selects the division ratio for RF and IF prescalers.

Setting the Registers

Each PLL of the HD155017T has four registers which are used to set the division ratio of the reference , program, swallow counter and the prescaler. These registers, as well as the above mentioned operating modes, are set by the CLOCK, DATA and LE signals from the microprocessor. Figure 3 shows the data sequence of the serial commands. In order to set the RF or IF reference counter register, the bit sequence is FO, LD, RC, IC, FC, reference counter register value, register selection bit2, register selection bit1.

To set the RF or IF program and swallow counter registers, the PS bit comes first followed by PR, program counter register value, swallow counter register value, register selection bit2, register selection bit1. Note that the serial data bits for setting each counter's register value must be preceded by an MSB. The number of bits used by the RF and IF reference counters are 15, and their values are from 8 to 32767. The RF and IF program counters have 11 bits, and their programmable values are from 8 to 2047. As for the RF swallow counter, it has 7 bits, the programmable value of which is from 0 to 127. Note, however, that the division ratio of the RF prescaler must be taken into account when setting the value of RF swallow counter. The value of the RF swallow counter is from 0 to 63, if the prescaler division ratio is 64/65.

Similarly, the IF swallow counter has 5 bits, with a value from 0 to 31. Again, the value is limited by the division ratio of the IF prescaler. If it is 16/17, the swallow counter value must be 0 to 15. The IF swallow counter value must be preceded by two consecutive zeros in the serial data stream.

The combination of register selection bits 1 and 2 chooses which registers are to be written to by the serial data. Table 3 shows which register is chosen according to the combination of the register selection bits.

Figure 4 is a block diagram of the serial data interface and registers. The timing chart is shown in figure 5. Each loading of data through the DATA pin to the shift registers is synchronized to the positive edge of the CLOCK signal.

The serial data is followed by the LE pulse which transfers the loaded data to the registers specified by the register selection bits 1 and 2.

Note that the length of each register is 22 bits. Therefore the command length should also be 22 bits. A longer or shorter command would result in the wrong division ratio or mode of operation being selected.

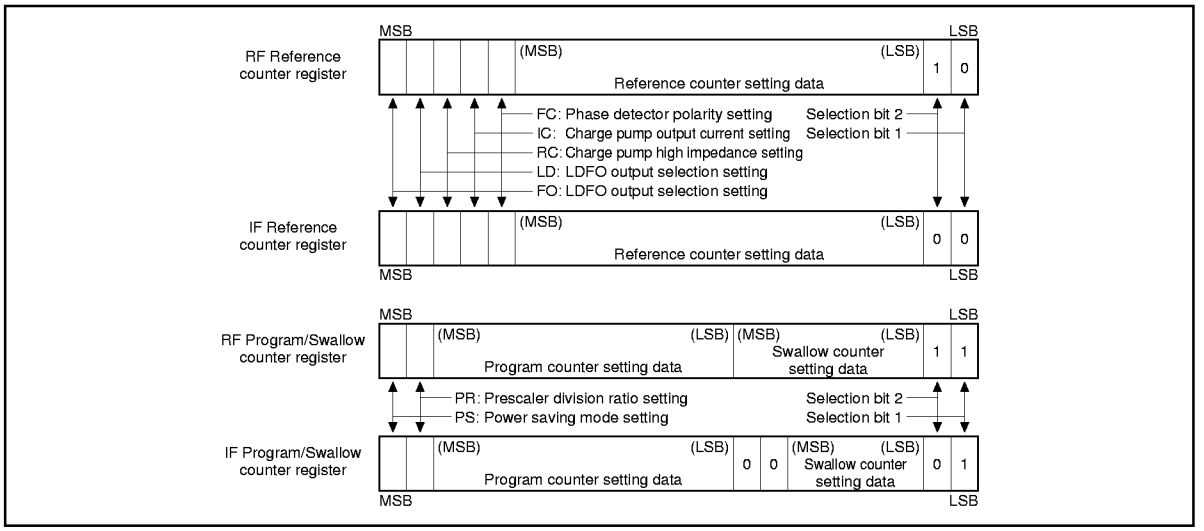


Figure 3 Operating Mode Setting

Table 3 Setting the HD155017T Register

Selection Bit 2	Selection Bit 1	Register
H	L	RF Reference counter
L	L	IF Reference counter
H	H	RF Program/Swallow counter
L	H	IF Program/Swallow counter

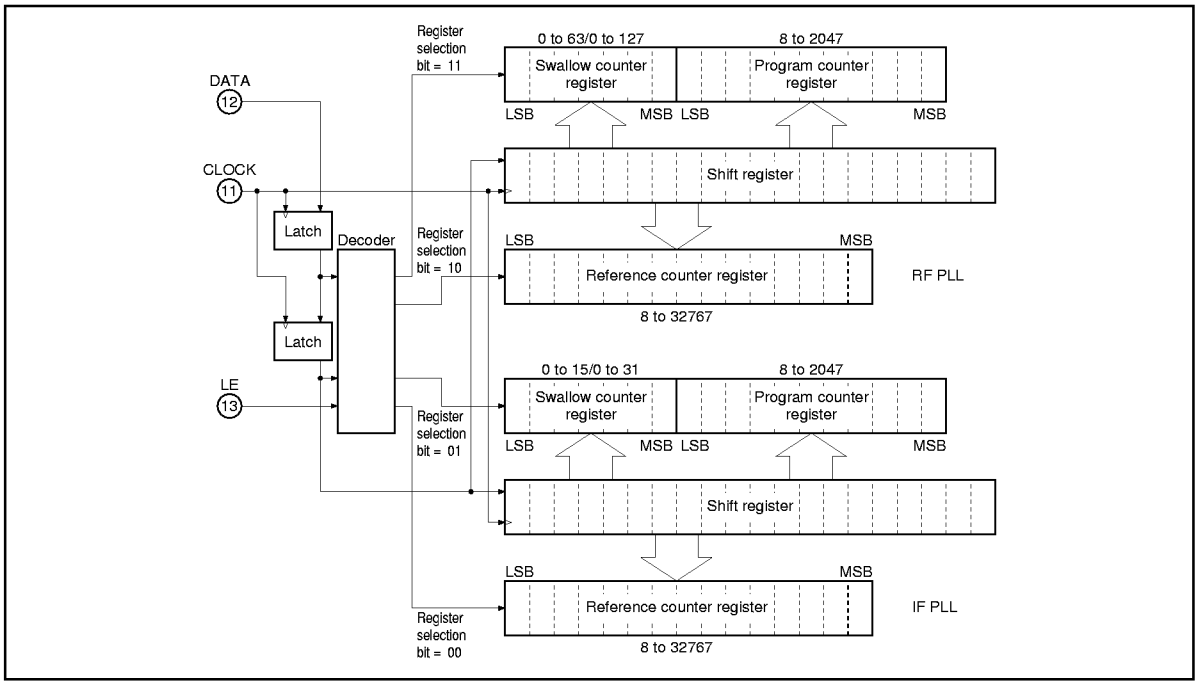


Figure 4 Structure of HD155017T Internal Register

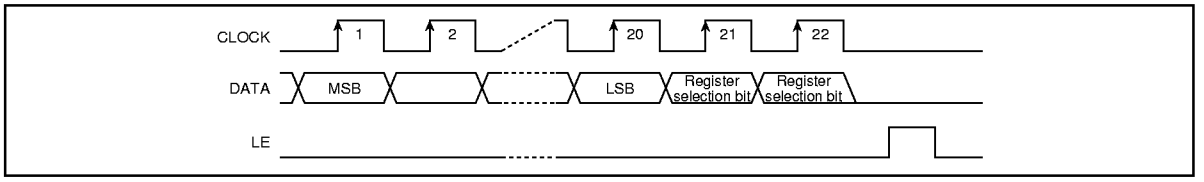


Figure 5 Setting the Registers

Power Saving Mode

In power saving mode, the ECL prescaler of the HD155017T is disabled to reduce power consumption.

As for the CMOS blocks, they consume essentially no power when there is no clock. Therefore the clock input to the CMOS blocks is stopped when power saving is activated. Furthermore, the charge pump output goes to a high impedance state in order for the loop filter to hold the preceding VCO control voltage.

The initialization of power saving is internally controlled in order to avoid starting this mode while the charge pump is active (i.e. phase comparison is in process). Figure 6 shows this timing relationship. The power saving mode starts from the last negative edge of the OSCIN clock, which is before the positive edge of the reference counter output.

Similarly, the phase error between the reference counter output and the program counter output is minimized when recovering the HD155017T from the power saving mode. Figure 7 shows the timing chart. When PS goes 'L', the reference counter and the prescaler start operating. Then the first overflow pulse from the reference counter wakes up the program and swallow counters. As a result the phase error of both the program and swallow counters are minimized.

This is due to the fact that CMOS circuits can retain their states even if the clock signal is removed whereas ECL circuits can not.

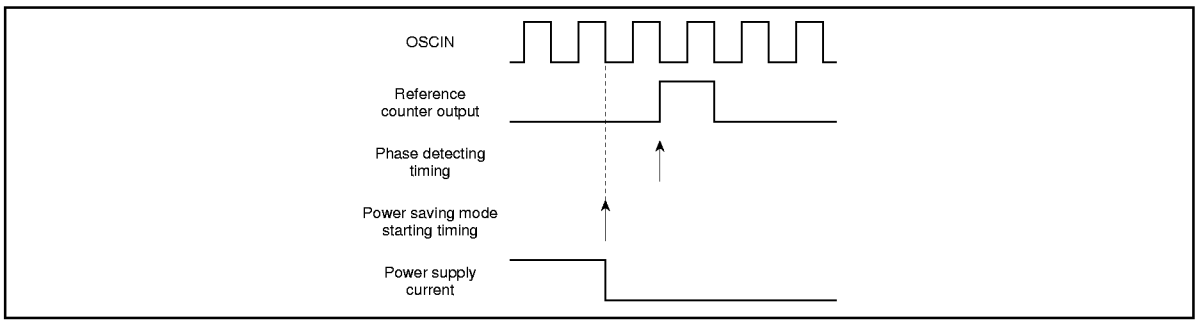


Figure 6 Power Saving Mode Starting Timing

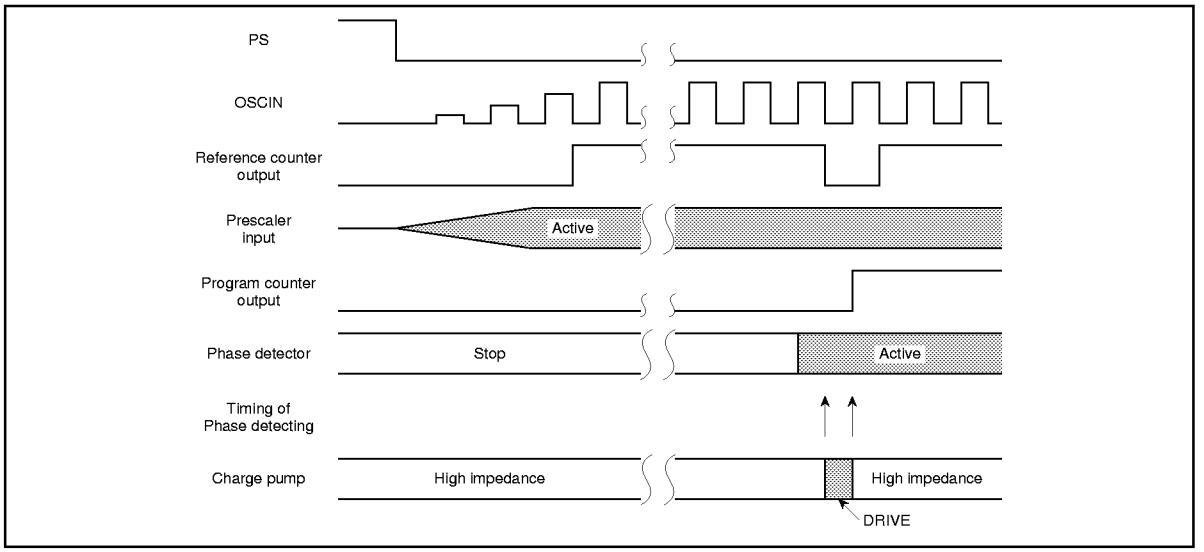


Figure 7 Recover Timing of Power Saving Mode

Fast Lock-up Mode

As explained above, the HD155017T has a circuit which minimizes the phase error when recovering from the power saving mode. Yet this circuit can not provide any recovery ability outside of the set time constant of the loop filter since it can only be used to improve only the initial phase error. Thus, for further improvement of the fast lock-up characteristics, the HD155017T has a fast lock-up mode in which the time constant of the loop filter is changed. LD and FO are used to set this mode. It is also important to check the stability of the loop as the frequency response of the loop is changed in fast lock-up mode. When fast lock-up mode is selected, the MOS switch connected to LDFO is controlled by the IC bit. In other words, when the IC bit of RF reference counter resister is set 'H' the charge pump current becomes 2.25 times greater, and LDFO is connected to the ground through the MOS switch. Thus R2 is connected to the ground to achieve fast lock-up characteristics. The IC bit needs to be set 'L' after the acquisition to obtain better spurious.

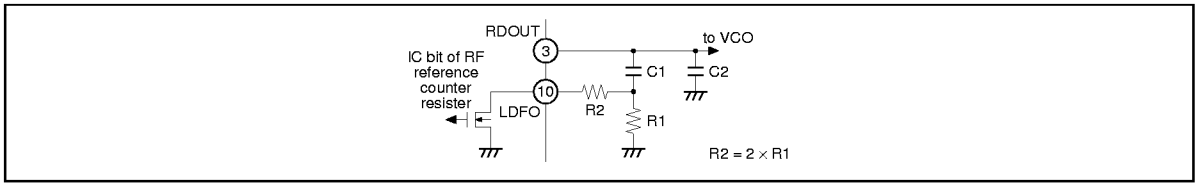


Figure 8 External Circuit on Fast Lock-up Mode (RF PLL)

Table 4 Operation of LDFO Pin at Fast Lock-up Mode

IC Bit of RF Reference Counter Resister	Operation of LDFO Pin
IC (RF) = L	Open (Switch = OFF)
IC (RF) = H	Ground (Switch = ON)

Internal State Monitoring

The overflow signal of each counter and lock detection signal of the HD155017T are observable at the LDFO pin. The LD and FO bits of the serial command specifies the signal to be monitored.

a) Counters

Overflow pulse of counters are monitored.

b) Lock detection signals

The lock detection signals are equivalent to the output of the phase detector's driving signals. If simultaneous monitoring of RF and IF is selected, the output is an 'AND' function of both the RF and IF lock detection signals.

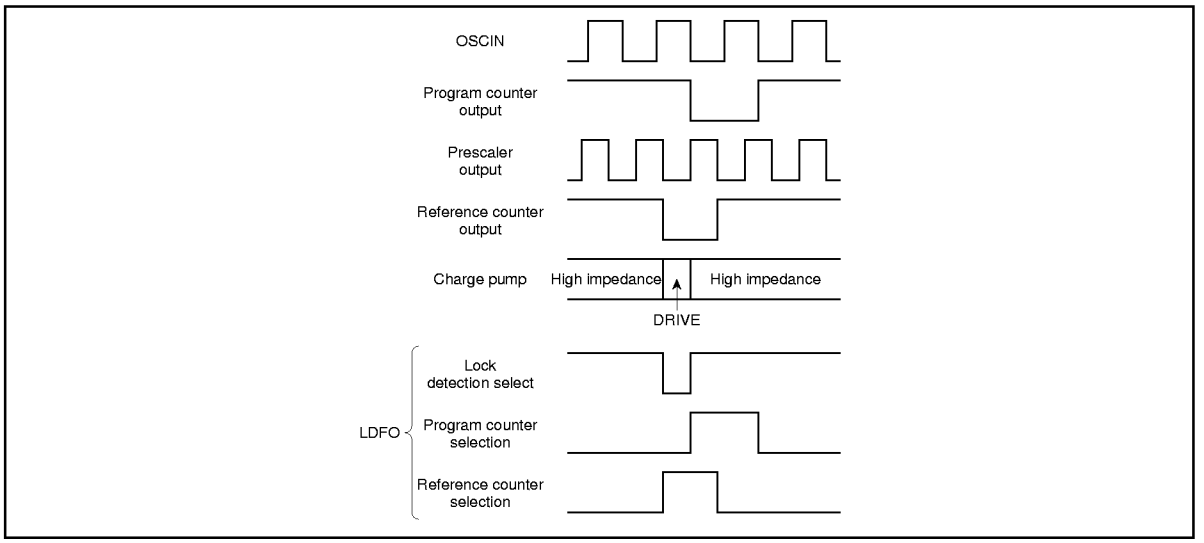


Figure 9 Monitor Output Timing

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage (VCC)	Vcc	–0.3 to +6.0	V
Power supply voltage (VP)	Vp	Vcc to +6.0	V
Voltage difference between Vcc and Vp	ΔV	±0.3	V
Pin voltage	Vt	–0.3 to Vcc+0.3 (6.0 Max)	V
Power dissipation	P_T	400	mW
Operating temperature	Topr	–30 to +85	°C
Storage temperature	Tstg	–55 to +125	°C

Electrical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins
Power supply voltage	V_{CC}	2.7	3.0	3.6	V		1, 20
Power supply voltage	V_P	V_{CC}–0.3	—	V_{CC}+0.3	V		2, 19
Power supply current	I_{CC}	—	14.0	17.5	mA	V_{CC}, V_P = 3.0V	1, 2, 19, 20
Power saving mode current	I_{PS}	–10	—	10	µA	V_{CC}, V_P = 3.0V	1, 2, 19, 20
RFIN operating frequency	f_{RFIN}	400	—	1900	MHz	V_{RFIN} = 0dBm	5
IFIN operating frequency	f_{IFIN16}	80	—	500	MHz	V_{IFIN} = 0dBm, PR of IF = "L"	16
	f_{IFIN32}	80	—	650	MHz	V_{IFIN} = 0dBm PR of IF = "H"	
OSCIN operating frequency	f_{OSCIN}	1	—	20	MHz	V_{OSCIN} = 0.6Vpp	8
RFIN input sensitivity	V_{RFIN}	–15	—	2	dBm	f_{RFIN} = 1700MHz	5
IFIN input sensitivity	V_{IFIN}	–15	—	2	dBm	f_{IFIN} = 400MHz	16
OSCIN input sensitivity	V_{OSCIN}	0.5	—	V_{CC}	Vpp	f_{OSCIN} = 10MHz	8
Input voltage	V_{IH}	0.7V_{CC}	—	V_{CC}	V		11, 12, 13
	V_{IL}	0	—	0.2V_{CC}	V		
Input leakage current	I_L	–1	—	1	µA	0 < V_{IL} < V_{CC}	11, 12, 13
Pull-up resistance	R_{PU}	—	50	—	kΩ		9
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 0.4mA	10
DOUT output current	I_{DOH}	—	–9.0	—	mA	V_{DOH} = 1/2V_{CC}	3, 18
(IC = "H")	I_{DOL}	—	9.0	—	mA	V_{DOL} = 1/2V_{CC}	3, 18
DOUT output current	I_{DOH}	—	–4.0	—	mA	V_{DOH} = 1/2V_{CC}	3, 18
(IC = "L")	I_{DOL}	—	4.0	—	mA	V_{DOL} = 1/2V_{CC}	3, 18
Cycle time	tcyc	(100)	—	—	ns	V_{CC} = 3.0V	11
Setup time	tstup	(10)	—	—	ns	V_{CC} = 3.0V	12
Hold time	thld	(10)	—	—	ns	V_{CC} = 3.0V	12
LE setup time	tsule	(50)	—	—	ns	V_{CC} = 3.0V	13
LE width	twle	(50)	—	—	ns	V_{CC} = 3.0V	13

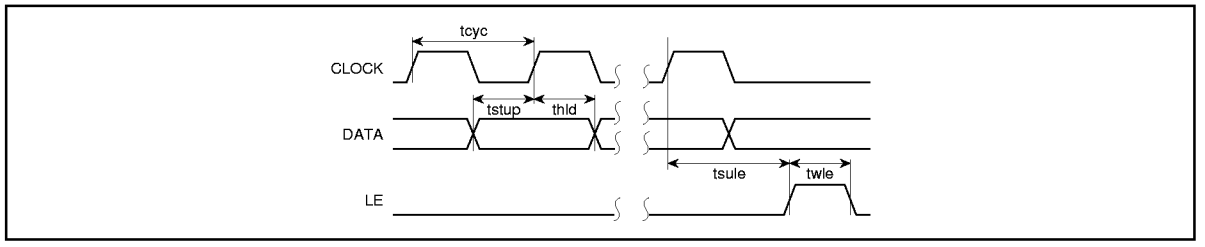
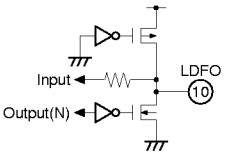
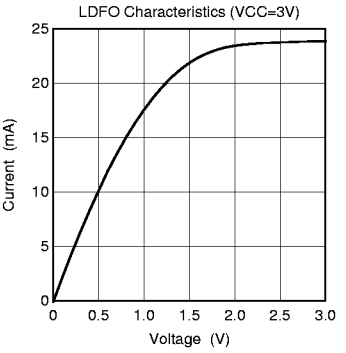


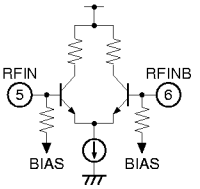
Figure 10 Serial Command Transmit Timing

Standard Characteristics of Pin (Ta = 25°C)

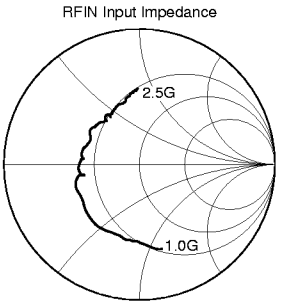


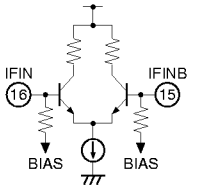
LDFO Equivalent Circuit





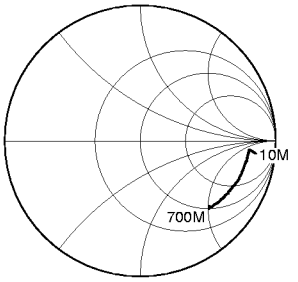
RFIN, RFINB Equivalent Circuit

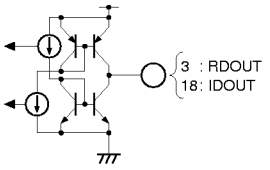




IFIN, IFINB Equivalent Circuit

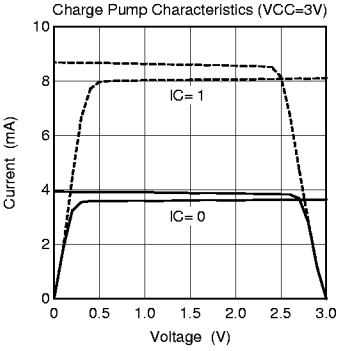
IFIN Input Impedance



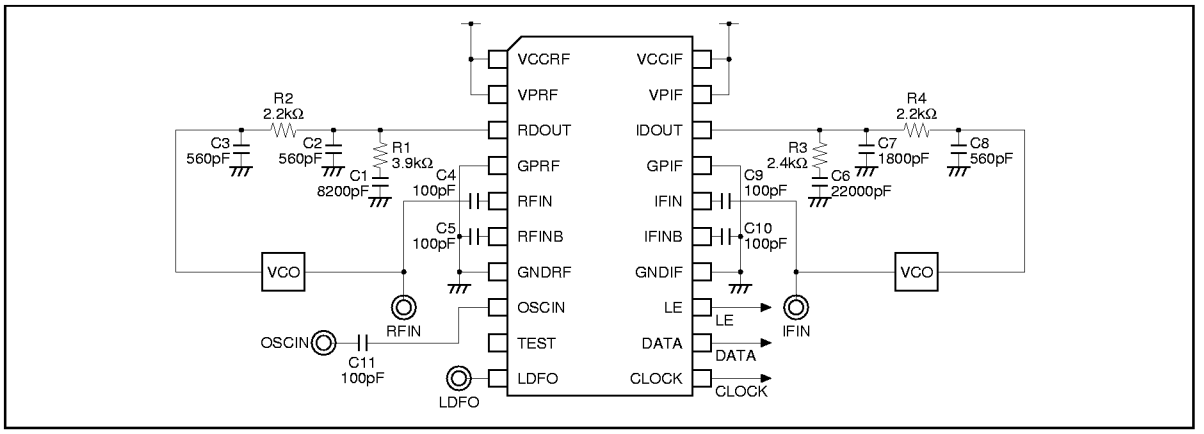


Charge Pump Equivalent Circuit

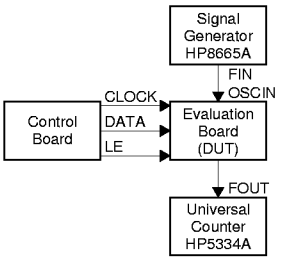
Charge Pump Characteristics (VCC=3V)



Example of External Circuit

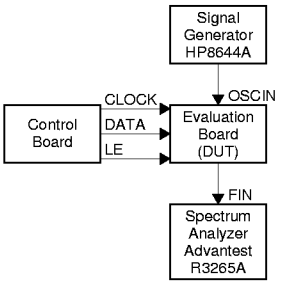


Test Conditions (Ta = 25°C)



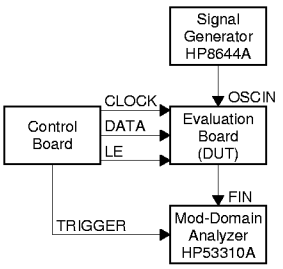
Item	Value
Toleranse	100p.p.m.

Condition of Input Sensitivity Characteristics



Item	Value (Long span)	(Short span)
Power supply voltage	3.0V	
OSCIN condition	19.2MHz 0dBm	
RF Phase detect frequency	200kHz	
IF Phase detect frequency	200kHz	
RF Lock frequency	1172MHz	
IF Lock frequency	540MHz	
RBW	3kHz	100Hz
VBW	300Hz	100Hz
Sweep time	2.3sec	2sec

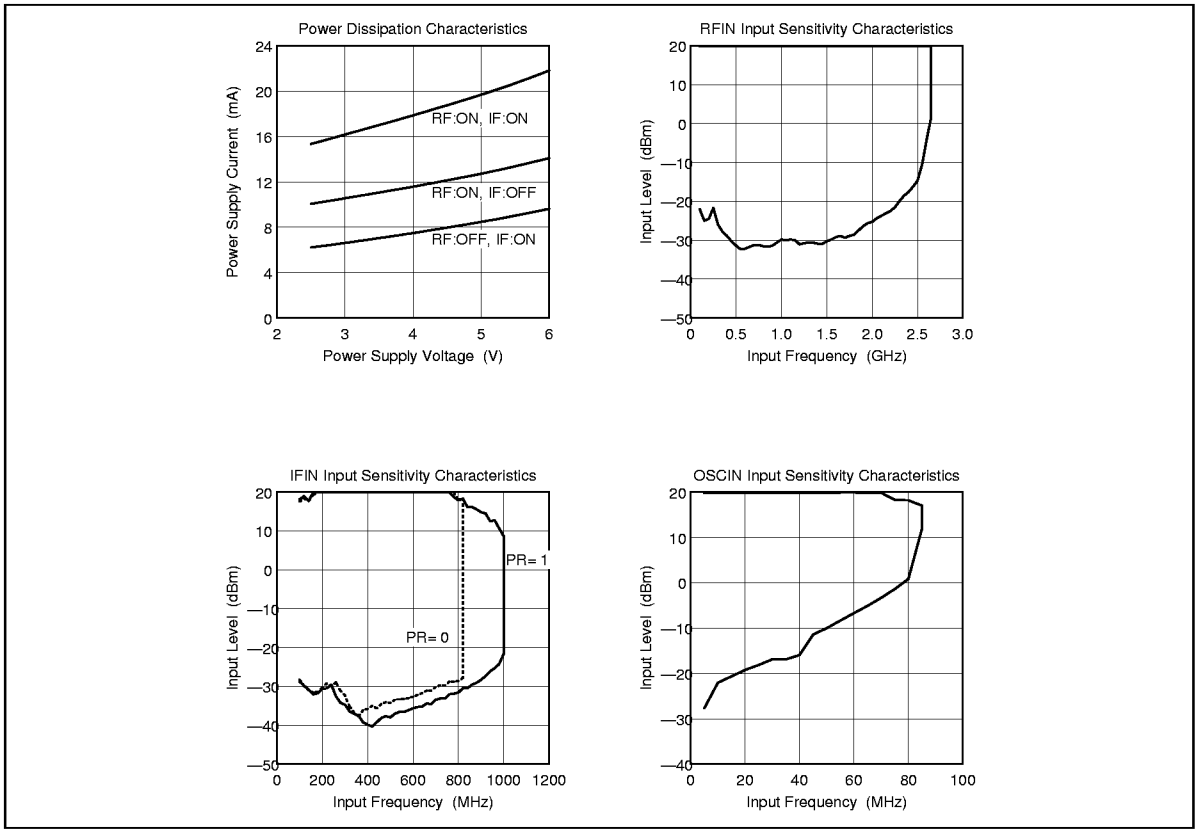
Condition of Spurious Characteristics

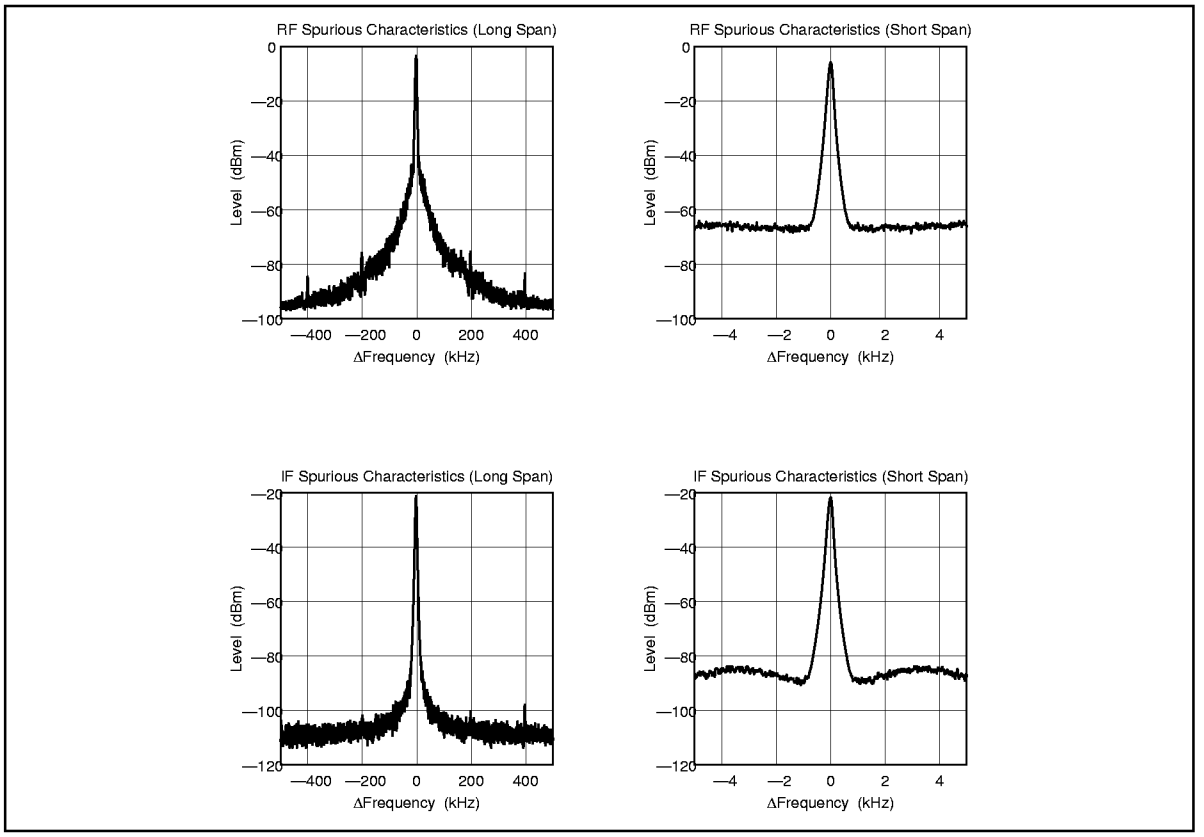


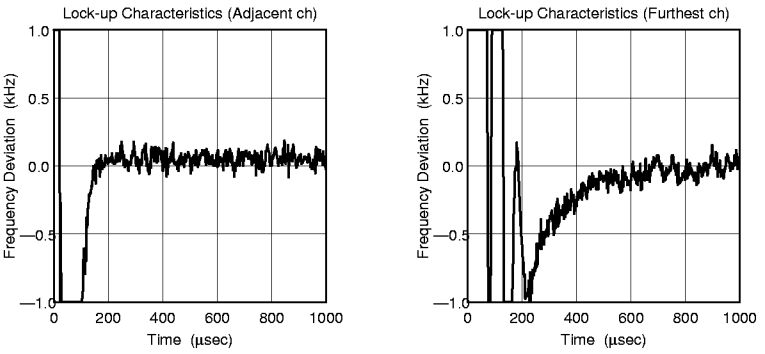
Item	Value
Power supply voltage	3.0V
OSCIN condition	19.2MHz 0dBm
Phase detect frequency	200kHz
Frequency deviation (adjacent ch)	1172.0MHz to 1172.2MHz
Frequency deviation (furthest ch)	1150MHz to 1185MHz

Condition of Measuring Lock-up Time

Standard Characteristics (Ta = 25°C)

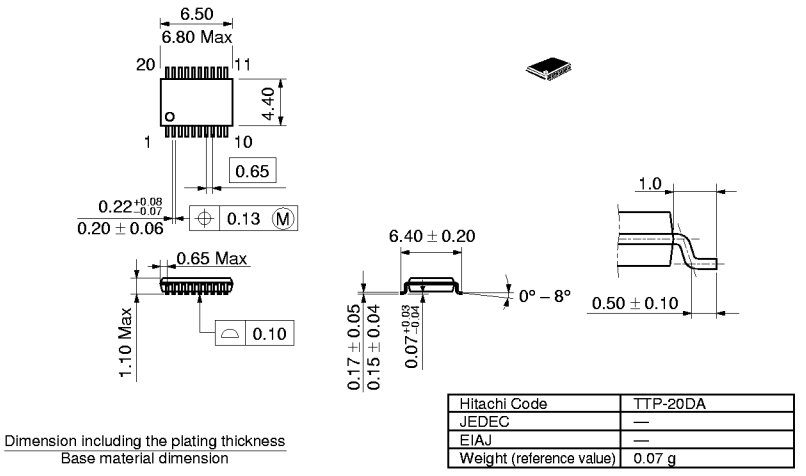



RF Spurious Characteristics (Long Span)
Level (dBm)
0
—20
—40
—60
—80
—100
—400 —200 0 200 400
ΔFrequency (kHz)
RF Spurious Characteristics (Short Span)
Level (dBm)
0
—20
—40
—60
—80
—100
—4 —2 0 2 4
ΔFrequency (kHz)
IF Spurious Characteristics (Long Span)
Level (dBm)
—20
—40
—60
—80
—100
—120
—400 —200 0 200 400
ΔFrequency (kHz)
IF Spurious Characteristics (Short Span)
Level (dBm)
—20
—40
—60
—80
—100
—120
—4 —2 0 2 4
ΔFrequency (kHz)


Lock-up Characteristics (Adjacent ch)
Frequency Deviation (kHz)
1.0
0.5
0.0
—0.5
—1.0
0
200
400
600
800
1000
Time (µsec)
Lock-up Characteristics (Furthest ch)
Frequency Deviation (kHz)
1.0
0.5
0.0
—0.5
—1.0
0
200
400
600
800
1000
Time (µsec)

Package Dimensions

Unit: mm



Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-20DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.07 g