

OKI Semiconductor

MSC23V47257TD-xxBS18

4,194,304-Word x 72-Bit DYNAMIC RAM MODULE : FAST PAGE MODE TYPE WITH EDO

DESCRIPTION

The MSC23V47257TD-xxBS18 is a 4,194,304-word x 72-bit CMOS dynamic random access memory module which is composed of eighteen 16Mb(4Mx4) DRAMs in TSOP packages mounted with eighteen decoupling capacitors. This is an 168-pin dual in-line memory module. This module supports any application where high density and large capacity of storage memory are required.

FEATURES

- 4,194,304-word x 72-bit organization
- 168-pin Dual In-line Memory Module
- Gold tab
- Single 3.3V power supply, $\pm 0.3V$ tolerance
- Input : LVTTTL compatible
- Output : LVTTTL compatible, 3-state
- Refresh : 2048cycles/ 32ms
- /CAS before /RAS refresh, hidden refresh, /RAS only refresh capability
- Fast page mode with EDO, read modify write capability
- Multi-bit test mode capability
- Serial Presence Detect

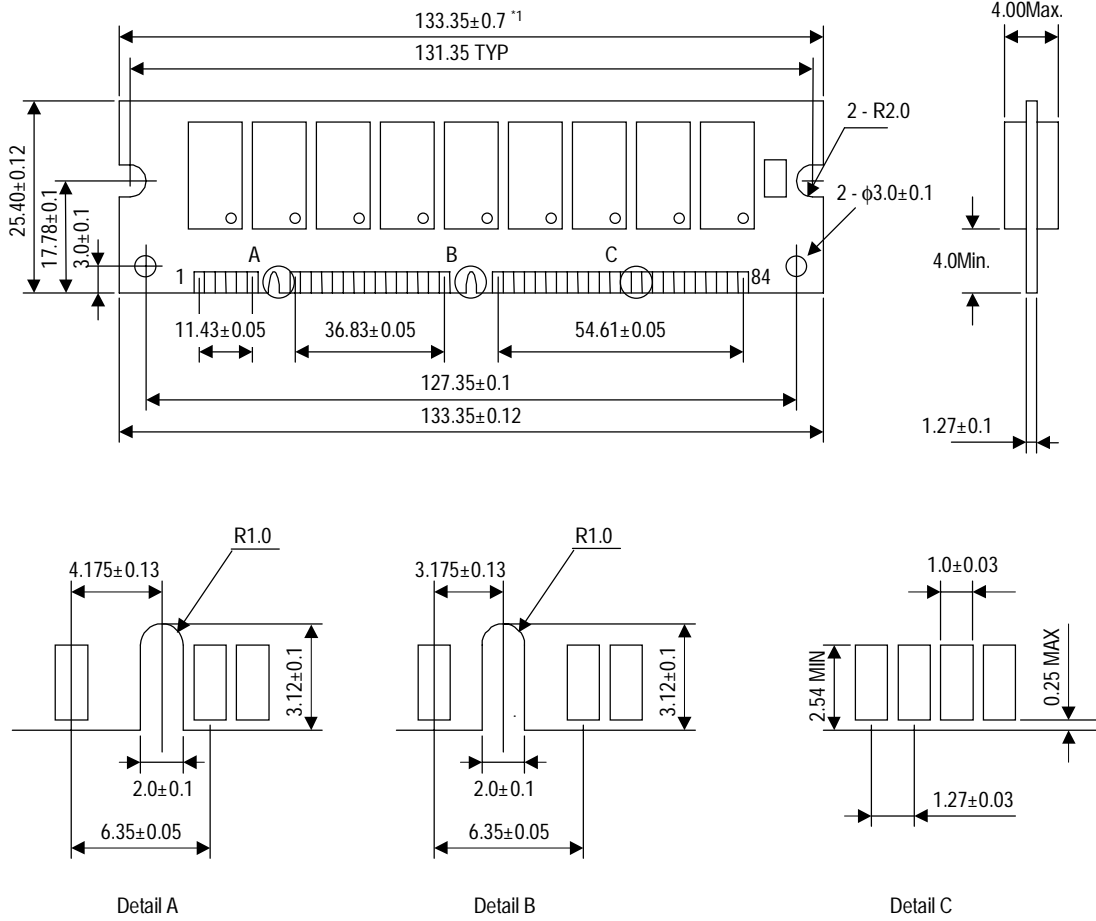
PRODUCT FAMILY

| Family | Access Time (Max.) | | | | Cycle Time (Min.) | Power Dissipation (Max.) | |
|----------------------|--------------------|-----------------|------------------|------------------|-------------------|--------------------------|---------|
| | t _{RAC} | t _{AA} | t _{CAC} | t _{OEA} | | Operating | Standby |
| MSC23V47257TD-50BS18 | 50ns | 25ns | 13ns | 13ns | 84ns | 6480mW | 32.4mW |
| MSC23V47257TD-60BS18 | 60ns | 30ns | 15ns | 15ns | 104ns | 5832mW | |
| MSC23V47257TD-70BS18 | 70ns | 35ns | 20ns | 20ns | 124ns | 5184mW | |

MODULE OUTLINE

MSC23V47257TD-xxBS18

(Unit : mm)



Note:
 1. Tolerance over 19.78mm from bottom edge is ±0.7.

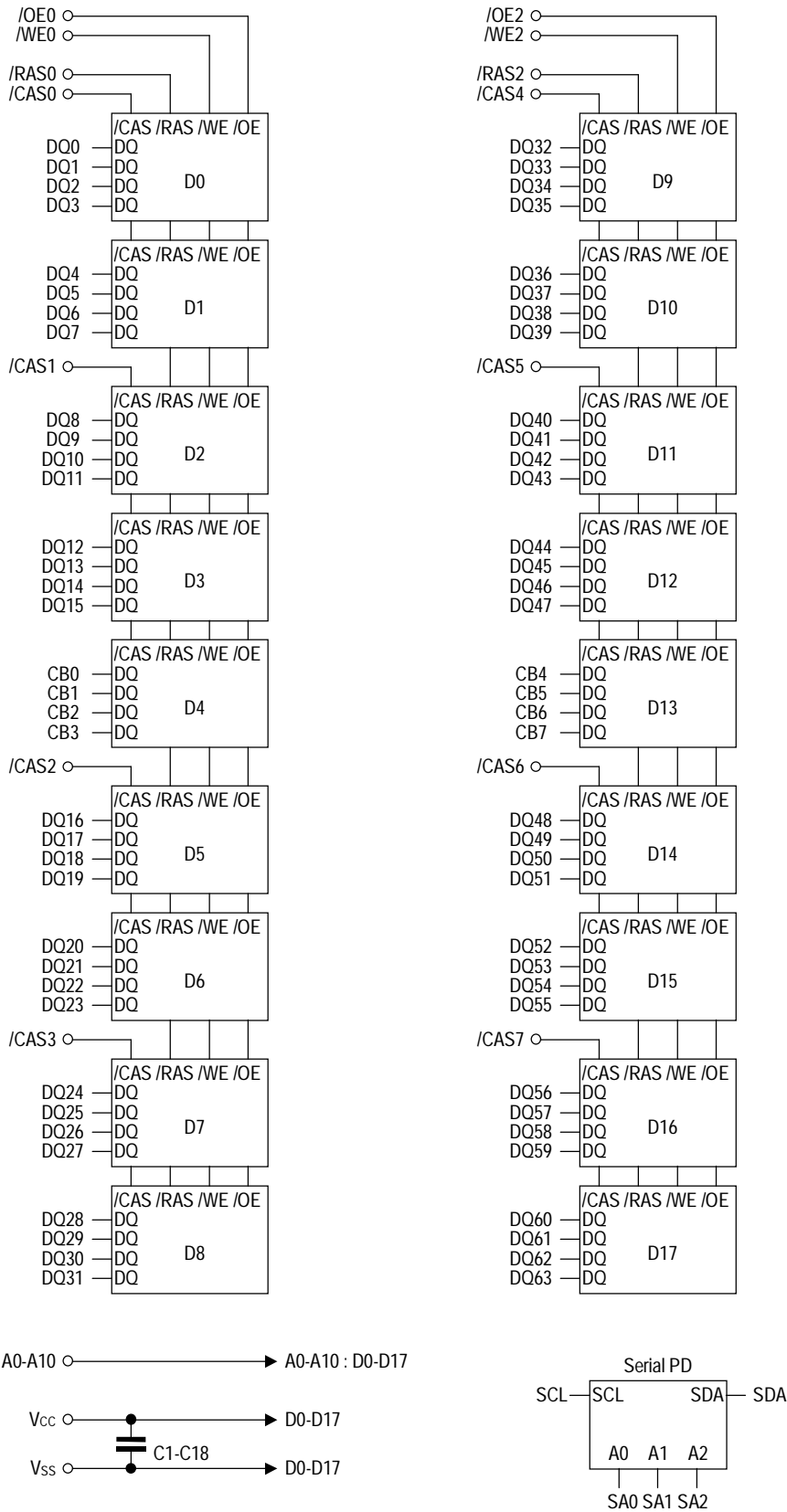
PIN CONFIGURATION

| Front Side | | Back Side | | Front Side | | Back Side | |
|------------|-----------------|-----------|-----------------|------------|-----------------|-----------|-----------------|
| Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name |
| 1 | V _{SS} | 85 | V _{SS} | 43 | V _{SS} | 127 | V _{SS} |
| 2 | DQ0 | 86 | DQ32 | 44 | /OE2 | 128 | NC |
| 3 | DQ1 | 87 | DQ33 | 45 | /RAS2 | 129 | NC |
| 4 | DQ2 | 88 | DQ34 | 46 | /CAS2 | 130 | /CAS6 |
| 5 | DQ3 | 89 | DQ35 | 47 | /CAS3 | 131 | /CAS7 |
| 6 | V _{CC} | 90 | V _{CC} | 48 | /WE2 | 132 | NC |
| 7 | DQ4 | 91 | DQ36 | 49 | V _{CC} | 133 | V _{CC} |
| 8 | DQ5 | 92 | DQ37 | 50 | NC | 134 | NC |
| 9 | DQ6 | 93 | DQ38 | 51 | NC | 135 | NC |
| 10 | DQ7 | 94 | DQ39 | 52 | CB2 | 136 | CB6 |
| 11 | DQ8 | 95 | DQ40 | 53 | CB3 | 137 | CB7 |
| 12 | V _{SS} | 96 | V _{SS} | 54 | V _{SS} | 138 | V _{SS} |
| 13 | DQ9 | 97 | DQ41 | 55 | DQ16 | 139 | DQ48 |
| 14 | DQ10 | 98 | DQ42 | 56 | DQ17 | 140 | DQ49 |
| 15 | DQ11 | 99 | DQ43 | 57 | DQ18 | 141 | DQ50 |
| 16 | DQ12 | 100 | DQ44 | 58 | DQ19 | 142 | DQ51 |
| 17 | DQ13 | 101 | DQ45 | 59 | V _{CC} | 143 | V _{CC} |
| 18 | V _{CC} | 102 | V _{CC} | 60 | DQ20 | 144 | DQ52 |
| 19 | DQ14 | 103 | DQ46 | 61 | NC | 145 | NC |
| 20 | DQ15 | 104 | DQ47 | 62 | NC | 146 | NC |
| 21 | CB0 | 105 | CB4 | 63 | NC | 147 | NC |
| 22 | CB1 | 106 | CB5 | 64 | V _{SS} | 148 | V _{SS} |
| 23 | V _{SS} | 107 | V _{SS} | 65 | DQ21 | 149 | DQ53 |
| 24 | NC | 108 | NC | 66 | DQ22 | 150 | DQ54 |
| 25 | NC | 109 | NC | 67 | DQ23 | 151 | DQ55 |
| 26 | V _{CC} | 110 | V _{CC} | 68 | V _{SS} | 152 | V _{SS} |
| 27 | /WE0 | 111 | NC | 69 | DQ24 | 153 | DQ56 |
| 28 | /CAS0 | 112 | /CAS4 | 70 | DQ25 | 154 | DQ57 |
| 29 | /CAS1 | 113 | /CAS5 | 71 | DQ26 | 155 | DQ58 |
| 30 | /RAS0 | 114 | NC | 72 | DQ27 | 156 | DQ59 |
| 31 | /OE0 | 115 | NC | 73 | V _{CC} | 157 | V _{CC} |
| 32 | V _{SS} | 116 | V _{SS} | 74 | DQ28 | 158 | DQ60 |
| 33 | A0 | 117 | A1 | 75 | DQ29 | 159 | DQ61 |
| 34 | A2 | 118 | A3 | 76 | DQ30 | 160 | DQ62 |
| 35 | A4 | 119 | A5 | 77 | DQ31 | 161 | DQ63 |
| 36 | A6 | 120 | A7 | 78 | V _{SS} | 162 | V _{SS} |
| 37 | A8 | 121 | A9 | 79 | NC | 163 | NC |
| 38 | A10 | 122 | NC | 80 | NC | 164 | NC |
| 39 | NC | 123 | NC | 81 | NC | 165 | SA0 |
| 40 | V _{CC} | 124 | V _{CC} | 82 | SDA | 166 | SA1 |
| 41 | V _{CC} | 125 | NC | 83 | SCL | 167 | SA2 |
| 42 | NC | 126 | NC | 84 | V _{CC} | 168 | V _{CC} |

Serial PD Matrix

| Byte No. | Function described | SPD Value (Hex) | Note | |
|----------|------------------------------------|-----------------|----------------|------|
| 0 | Number of Byte used | 80 | 128 Bytes | |
| 1 | Total SPD Memory size | 08 | 256 Bytes | |
| 2 | Memory type | 02 | EDO | |
| 3 | Number of Rows | 0B | 11 | |
| 4 | Number of Columns | 0B | 11 | |
| 5 | Number of Banks | 01 | 1 | |
| 6 | Module Data Width | 48 | 72 | |
| 7 | Module Data Width Continued | 00 | 0 | |
| 8 | Supply Voltage | 01 | LVTTL | |
| 9 | /RAS Access Time | -50 | 32 | 50ns |
| | | -60 | 3C | 60ns |
| | | -70 | 46 | 70ns |
| 10 | /CAS Access Time | -50 | 0D | 13ns |
| | | -60 | 0F | 15ns |
| | | -70 | 14 | 20ns |
| 11 | DIMM Configuration type | 02 | ECC | |
| 12 | Refresh Rate/Type | 00 | Normal Refresh | |
| 13 | Primary DRAM Width | 04 | x4 | |
| 14 | Error Checking DRAM Width | 04 | x4 | |
| 15-61 | Superset Information | 00 | Reserved | |
| 62 | SPD Data Revision Code | 01 | 1 | |
| 63 | Checksum for Byte 0-62 | -50 | 34 | |
| | | -60 | 40 | |
| | | -70 | 4F | |
| 64-127 | Reserved | 00 | | |
| 128-255 | Unused Storage Location (Reserved) | FF | | |

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|---|-------------------|-------------|------|
| Voltage on Any Pin Relative to V_{SS} | V_{IN}, V_{OUT} | -0.5 to 4.6 | V |
| Voltage on V_{CC} Supply Relative to V_{SS} | V_{CC} | -0.5 to 4.6 | V |
| Short Circuit Output Current | I_{OS} | 50 | mA |
| Power Dissipation | P_D^* | 18 | W |
| Operating Temperature | T_{OPR} | 0 to 70 | °C |
| Storage Temperature | T_{STG} | -40 to 125 | °C |

* $T_a = 25^\circ\text{C}$

Recommended Operating Conditions

($T_a = 0^\circ\text{C}$ to 70°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|----------------------|----------|------|------|--------------|------|
| Power Supply Voltage | V_{CC} | 3.0 | 3.3 | 3.6 | V |
| | V_{SS} | 0 | 0 | 0 | V |
| Input High Voltage | V_{IH} | 2.0 | - | $V_{CC}+0.3$ | V |
| Input Low Voltage | V_{IL} | -0.3 | - | 0.8 | V |

Capacitance

($V_{CC} = 3.3V \pm 0.3V$, $T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

| Parameter | Symbol | Typ. | Max. | Unit |
|--|-----------|------|------|------|
| Input Capacitance (A0 - A10) | C_{IN1} | - | 122 | pF |
| Input Capacitance (/RAS0, /RAS2, /WE0, /WE2, /OE0, /OE2) | C_{IN2} | - | 73 | pF |
| Input Capacitance (/CAS0 - /CAS7) | C_{IN3} | - | 28 | pF |
| I/O Capacitance (DQ0 - DQ63, CB0 - CB7) | $C_{I/O}$ | - | 16 | pF |

DC Characteristics

 $(V_{CC} = 3.3V \pm 0.3V, T_a = 0^\circ C \text{ to } 70^\circ C)$

| Parameter | Symbol | Condition | -50 | | -60 | | -70 | | Unit | Note |
|---|-----------|---|------|----------|------|----------|------|----------|---------|------|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Output High Voltage | V_{OH} | $I_{OH} = -2.0mA$ | 2.4 | V_{CC} | 2.4 | V_{CC} | 2.4 | V_{CC} | V | |
| Output Low Voltage | V_{OL} | $I_{OL} = 2.0mA$ | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | V | |
| Input Leakage Current | I_{LI} | $0V \leq V_{IN} \leq V_{CC} + 0.3V$; All other pins not under test = 0V | -180 | 180 | -180 | 180 | -180 | 180 | μA | |
| Output Leakage Current | I_{LO} | DQ disable $0V \leq V_{OUT} \leq V_{CC}$ | -10 | 10 | -10 | 10 | -10 | 10 | μA | |
| Average Power Supply Current (Operating) | I_{CC1} | /RAS, /CAS cycling, $t_{RC} = \text{Min.}$ | - | 1800 | - | 1620 | - | 1440 | mA | 1, 2 |
| Power Supply Current (Standby) | I_{CC2} | /RAS, /CAS = V_{IH} | - | 36 | - | 36 | - | 36 | mA | 1 |
| | | /RAS, /CAS $\geq V_{CC} - 0.2V$ | - | 9 | - | 9 | - | 9 | mA | |
| Average Power Supply Current (/RAS only refresh) | I_{CC3} | /RAS cycling, /CAS = V_{IH} , $t_{RC} = \text{Min.}$ | - | 1800 | - | 1620 | - | 1440 | mA | 1, 2 |
| Average Power Supply Current (/CAS before /RAS refresh) | I_{CC6} | /RAS cycling, /CAS before /RAS | - | 1800 | - | 1620 | - | 1440 | mA | 1, 2 |
| Average Power Supply Current (Fast Page Mode) | I_{CC7} | /RAS = V_{IL} , /CAS cycling, $t_{HPC} = \text{Min.}$ | - | 1800 | - | 1620 | - | 1440 | mA | 1, 3 |

- Notes: 1. I_{CC} Max. is specified as I_{CC} for output open condition.
2. The address can be changed once or less while /RAS = V_{IL} .
3. The address can be changed once or less while /CAS = V_{IH} .

AC Characteristics (1/2)

(V_{CC} = 3.3V ±0.3V, T_a = 0°C to 70°C) Note: 1, 2, 3, 12, 13

| Parameter | Symbol | -50 | | -60 | | -70 | | Unit | Note |
|--|--------------------|------|------|------|------|------|------|------|---------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Random Read or Write Cycle Time | t _{RC} | 84 | - | 104 | - | 124 | - | ns | |
| Read Modify Write Cycle Time | t _{RWC} | 110 | - | 135 | - | 160 | - | ns | |
| Fast Page Mode Cycle Time | t _{HPC} | 20 | - | 25 | - | 30 | - | ns | |
| Fast Page Mode Read Modify Write Cycle Time | t _{HPRWC} | 58 | - | 68 | - | 78 | - | ns | |
| Access Time from /RAS | t _{RAC} | - | 50 | - | 60 | - | 70 | ns | 4, 5, 6 |
| Access Time from /CAS | t _{CAC} | - | 13 | - | 15 | - | 20 | ns | 4, 5 |
| Access Time from Column Address | t _{AA} | - | 25 | - | 30 | - | 35 | ns | 4, 6 |
| Access Time from /CAS Precharge | t _{CPA} | - | 30 | - | 35 | - | 40 | ns | 4 |
| Access Time from /OE | t _{OEa} | - | 13 | - | 15 | - | 20 | ns | 4 |
| Output Low Impedance Time from /CAS | t _{CLZ} | 0 | - | 0 | - | 0 | - | ns | 4 |
| Data Output Hold After /CAS Low | t _{DOH} | 5 | - | 5 | - | 5 | - | ns | |
| /CAS to Data Output Buffer Turn-off Delay Time | t _{CEZ} | 0 | 13 | 0 | 15 | 0 | 20 | ns | 7, 8 |
| /RAS to Data Output Buffer Turn-off Delay Time | t _{REZ} | 0 | 13 | 0 | 15 | 0 | 20 | ns | 7, 8 |
| /OE to Data Output Buffer Turn-off Delay Time | t _{OEZ} | 0 | 13 | 0 | 15 | 0 | 20 | ns | 7 |
| /WE to Data Output Buffer Turn-off Delay Time | t _{WEZ} | 0 | 13 | 0 | 15 | 0 | 20 | ns | 7 |
| Transition Time | t _T | 1 | 50 | 1 | 50 | 1 | 50 | ns | 3 |
| Refresh Period | t _{REF} | - | 32 | - | 32 | - | 32 | ms | |
| /RAS Precharge Time | t _{RP} | 30 | - | 40 | - | 50 | - | ns | |
| /RAS Pulse Width | t _{RAS} | 50 | 10K | 60 | 10K | 70 | 10K | ns | |
| /RAS Pulse Width (Fast Page Mode with EDO) | t _{RASP} | 50 | 100K | 60 | 100K | 70 | 100K | ns | |
| /RAS Hold Time | t _{RSH} | 7 | - | 10 | - | 13 | - | ns | |
| /RAS Hold Time referenced to /OE | t _{ROH} | 7 | - | 10 | - | 13 | - | ns | |
| /CAS Precharge Time (Fast Page Mode with EDO) | t _{CP} | 7 | - | 10 | - | 10 | - | ns | |
| /CAS Pulse Width | t _{CAS} | 7 | 10K | 10 | 10K | 13 | 10K | ns | |
| /CAS Hold Time | t _{CSH} | 35 | - | 40 | - | 45 | - | ns | |
| /CAS to /RAS Precharge Time | t _{CRP} | 5 | - | 5 | - | 5 | - | ns | |
| /RAS Hold Time from /CAS Precharge | t _{RHCP} | 30 | - | 35 | - | 40 | - | ns | |
| /OE Hold Time from /CAS (DQ Disable) | t _{CHO} | 5 | - | 5 | - | 5 | - | ns | |
| /RAS to /CAS Delay Time | t _{RCD} | 11 | 37 | 14 | 45 | 14 | 50 | ns | 5 |
| /RAS to Column Address Delay Time | t _{RAD} | 9 | 25 | 12 | 30 | 12 | 35 | ns | 6 |
| Row Address Set-up Time | t _{ASR} | 0 | - | 0 | - | 0 | - | ns | |
| Row Address Hold Time | t _{RAH} | 7 | - | 10 | - | 10 | - | ns | |
| Column Address Set-up Time | t _{ASC} | 0 | - | 0 | - | 0 | - | ns | |
| Column Address Hold Time | t _{CAH} | 7 | - | 10 | - | 13 | - | ns | |
| Column Address to /RAS Lead Time | t _{RAL} | 25 | - | 30 | - | 35 | - | ns | |

AC Characteristics (2/2)

(V_{CC} = 3.3V ±0.3V, T_a = 0°C to 70°C) Note: 1, 2, 3, 12, 13

| Parameter | Symbol | -50 | | -60 | | -70 | | Unit | Note |
|---|-------------------|------|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Read Command Set-up Time | t _{RCS} | 0 | - | 0 | - | 0 | - | ns | |
| Read Command Hold Time | t _{RCH} | 0 | - | 0 | - | 0 | - | ns | 9 |
| Read Command Hold Time referenced to /RAS | t _{RRH} | 0 | - | 0 | - | 0 | - | ns | 9 |
| Write Command Set-up Time | t _{WCS} | 0 | - | 0 | - | 0 | - | ns | 10 |
| Write Command Hold Time | t _{WCH} | 7 | - | 10 | - | 13 | - | ns | |
| Write Command Pulse Width | t _{WP} | 7 | - | 10 | - | 10 | - | ns | |
| /WE Pulse Width (DQ Disable) | t _{WPE} | 7 | - | 10 | - | 10 | - | ns | |
| /OE Command Hold Time | t _{OEH} | 7 | - | 10 | - | 13 | - | ns | |
| /OE Precharge Time | t _{OEP} | 7 | - | 10 | - | 10 | - | ns | |
| /OE Command Hold Time | t _{OCH} | 7 | - | 10 | - | 10 | - | ns | |
| Write Command to /RAS Lead Time | t _{RWL} | 7 | - | 10 | - | 13 | - | ns | |
| Write Command to /CAS Lead Time | t _{CWL} | 7 | - | 10 | - | 13 | - | ns | |
| Data-in Set-up Time | t _{DS} | 0 | - | 0 | - | 0 | - | ns | 11 |
| Data-in Hold Time | t _{DH} | 7 | - | 10 | - | 13 | - | ns | 11 |
| /OE to Data-in Delay Time | t _{OED} | 13 | - | 15 | - | 20 | - | ns | |
| /CAS to /WE Delay Time | t _{CWD} | 30 | - | 34 | - | 44 | - | ns | 10 |
| Column Address to /WE Delay Time | t _{AWD} | 42 | - | 49 | - | 59 | - | ns | 10 |
| /RAS to /WE Delay Time | t _{RWD} | 67 | - | 79 | - | 94 | - | ns | 10 |
| /CAS Precharge /WE Delay Time | t _{CPWD} | 47 | - | 54 | - | 64 | - | ns | 10 |
| /CAS Active Delay Time from /RAS Precharge | t _{RPC} | 5 | - | 5 | - | 5 | - | ns | |
| /RAS to /CAS Set-up Time (/CAS before /RAS) | t _{CSR} | 5 | - | 5 | - | 5 | - | ns | |
| /RAS to /CAS Hold Time (/CAS before /RAS) | t _{CHR} | 10 | - | 10 | - | 10 | - | ns | |
| /WE to /RAS Precharge Time (/CAS before /RAS) | t _{WRP} | 10 | - | 10 | - | 10 | - | ns | |
| /WE Hold Time from /RAS (/CAS before /RAS) | t _{WRH} | 10 | - | 10 | - | 10 | - | ns | |
| /RAS to /WE Set-up Time (Test Mode) | t _{WTS} | 10 | - | 10 | - | 10 | - | ns | |
| /RAS to /WE Hold Time (Test Mode) | t _{WTH} | 10 | - | 10 | - | 10 | - | ns | |

- Notes:
1. A start-up delay of 200 μ s is required after power-up, followed by a minimum of eight initialization cycles (/RAS only refresh or /CAS before /RAS refresh) before proper device operation is achieved.
 2. The AC characteristics assume $t_T = 2$ ns.
 3. $V_{IH}(\text{Min.})$ and $V_{IL}(\text{Max.})$ are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL} .
 4. This parameter is measured with a load circuit equivalent to 1 TTL load and 100pF. The output timing reference levels are $V_{OH} = 2.0$ V and $V_{OL} = 0.8$ V.
 5. Operation within the $t_{RCD}(\text{Max.})$ limit ensures that $t_{RAC}(\text{Max.})$ can be met. $t_{RCD}(\text{Max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{Max.})$ limit, then the access time is controlled by t_{CAC} .
 6. Operation within the $t_{RAD}(\text{Max.})$ limit ensures that $t_{RAC}(\text{Max.})$ can be met. $t_{RAD}(\text{Max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{Max.})$ limit, then the access time is controlled by t_{AA} .
 7. $t_{CEZ}(\text{Max.})$, $t_{REZ}(\text{Max.})$, $t_{WEZ}(\text{Max.})$ and $t_{OEZ}(\text{Max.})$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
 8. t_{CEZ} or t_{REZ} must be satisfied for open circuit condition.
 9. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 10. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{Min.})$, then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}(\text{Min.})$, $t_{RWD} \geq t_{RWD}(\text{Min.})$, $t_{AWD} \geq t_{AWD}(\text{Min.})$ and $t_{CPWD} \geq t_{CPWD}(\text{Min.})$, then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
 11. These parameters are referenced to the /CAS leading edge in an early write cycle, and to the /WE leading edge in an /OE control write cycle, or a read modify write cycle.
 12. The test mode is initiated by performing a /WE and /CAS before /RAS refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. The test mode specified in this data sheet is an 8-bit parallel test function. CA0, CA1 and CA10 are not used. In a read cycle, if all internal bits are equal, the DQ pin will indicate a high level. If any internal bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a /RAS only refresh cycle or a /CAS before /RAS refresh cycle.
 13. In a test mode read cycle, the value of access time parameters is delayed for 5ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.