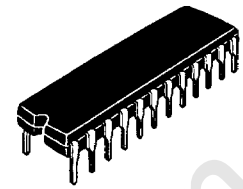
HM53462 Series

65,536-Word x 4-Bit Multiport CMOS Video RAM (with Logic Operation Mode)

■ DESCRIPTION

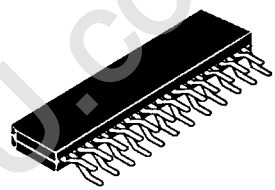
The HM53462 is a 262,144-bit multiport memory equipped with a 64k-word x 4-bit Dynamic RAM port and a 256-word x 4-bit Serial Access Memory (SAM) port. The SAM port is connected to an internal 1,024-bit data register through a 256-word x 4-bit serial read or write access control. In the read transfer cycle, the memory cell data is transferred from a selected word line of the RAM port to the data register. The RAM port has a write mask capability in addition to the conventional operation mode. Write bit selection out of 4 data bit can be achieved. RAM port has another new function, logic operation capability. By this function logic operation between memory data and input data can be done in one cycle. Utilizing the Hitachi 2 μm CMOS process, fast serial access operation and low power dissipation are realized. All inputs and outputs, including clocks, are TTL compatible.

HM53462P Series



(DP-24A)

HM53462ZP Series



(ZP-24)

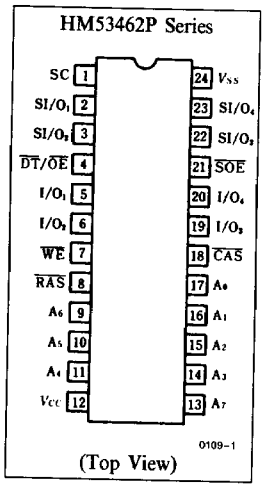
■ FEATURES

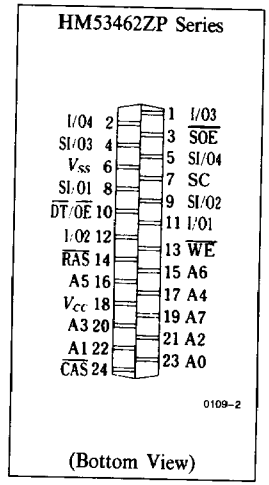
- Multiport Organization
  (RAM; 64k-word x 4-bit and SAM; 256-word x 4-bit)
- Double Layer Polysilicon/Polyicide N-Well CMOS Process
- Single 5V (±10%)
- Low Power
  - Active RAM ..... 380 mW (max)
  - SAM ..... 220 mW (max)
  - Standby ..... 40 mW (max)
- Access Time
  - RAM ..... 100 ns/120 ns/150 ns
  - SAM ..... 40 ns/40 ns/60 ns
- Cycle Time
  - Random Read or Write Cycle Time (RAM) ..... 190 ns/220 ns/260 ns
  - Serial Read or Write Cycle Time (SAM) ..... 40 ns/40 ns/60 ns
- TTL Compatible
- 256 Refresh Cycles ..... 4 ms
- Refresh Function
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Bidirectional Data Transfer Operation (RAM ⟷ SAM)
- Fast Serial Access Operation Asynchronized with RAM Port except Data Transfer Cycle
- Real Time Read Transfer Capability
- Write Mask Mode Capability
- Logic Operation Capability between D_{in} and D_{out}
- SAM Organization Can Be Changed to 1024 x 1

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM53462P-10	100 ns	400 mil 24-pin
HM53462P-12	120 ns	Plastic DIP
HM53462P-15	150 ns	(DP-24A)
HM53462ZP-10	100 ns	24-pin
HM53462ZP-12	120 ns	Plastic DIP
HM53462ZP-15	150 ns	(ZP-24)

■ PIN OUT

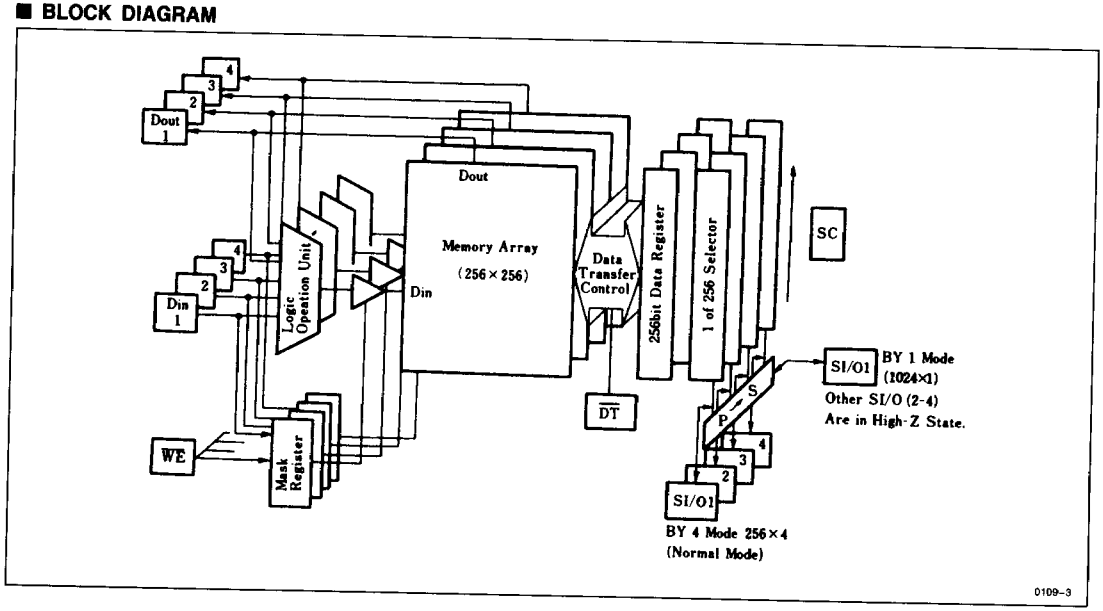




■ PIN DESCRIPTION

Pin Name	Function
A_0–A_7	Address Input
I/O_1–I/O_4	RAM Port Data Input/Output
SI/O_1–SI/O_4	SAM Port Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
SC	Serial Clock
$\overline{WE}$	Write Enable
$\overline{DT/OE}$	Data Transfer/Output Enable
$\overline{SOE}$	SAM Port Enable
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Power Supply Voltage Relative to V_{SS}	V_{CC}	− 0.5 to + 7.0	V
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W

■ INPUT/OUTPUT CAPACITANCE

Parameter	Symbol	Typ	Max	Unit	Note
Address	C_{I1}	—	5	pF	
Clocks	C_{I2}	—	5	pF	
I/O, SI/O	$C_{I/O}$	—	7	pF	

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.4	—	6.5	V	
Input Low Voltage	V_{IL}	− 0.5	—	0.8	V	2

Notes: 1. All voltages referenced to V_{SS}.
2. − 3.0V for pulse width ≤ 10 ns.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

RAM Port	Symbol	SAM Port		HM53462 -10	HM53462 -12	HM53462 -15	Unit	Note
		Standby	Active					
Operating Current $\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = min	I_{CC1}	—	×	70	60	50	mA	
	I_{CC7}	×	—	110	100	80	mA	
Standby Current $\overline{RAS}$, $\overline{CAS}$ = V_{IH}	I_{CC2}	—	×	7	7	7	mA	
	I_{CC8}	×	—	40	40	30	mA	
$\overline{RAS}$ Only Refresh Current $\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling t_{RC} = min	I_{CC3}	—	×	60	50	40	mA	
	I_{CC9}	×	—	100	90	70	mA	
Page Mode Current $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling t_{PC} = min	I_{CC4}	—	×	50	40	35	mA	
	I_{CC10}	×	—	90	80	65	mA	
CBR Refresh Current $\overline{RAS}$ Cycling t_{RC} = min	I_{CC5}	—	X	60	50	40	mA	
	I_{CC11}	×	—	100	90	70	mA	
Data Transfer Current $\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = min	I_{CC6}	—	×	75	65	55	mA	
	I_{CC12}	×	—	115	105	85	mA	

Parameter	Symbol	Min	Max	Unit	Note
Input Leakage	I_{LI}	− 10	10	μA	
Output Leakage	I_{LO}	− 10	10	μA	
Output High Voltage I_{OH} = − 2 mA	V_{OH}	2.4	—	V	
Output Low Voltage I_{OL} = 4.2 mA	V_{OL}	—	0.4	V	

• Electrical Characteristics and Recommended AC Operating Conditions

(T_A = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)[1, 10, 11]

Parameter	Symbol	HM53462-10		HM53462-12		HM53462-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	190	—	220	—	260	—	ns	
Read-Modify-Write Cycle Time	t_{RWC}	260	—	300	—	355	—	ns	
Page Mode Cycle Time	t_{PC}	70	—	85	—	105	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	50	—	60	—	75	ns	3, 4
Outout Buffer Turn-off Delay Referenced to $\overline{CAS}$	t_{OFF1}	0	25	0	30	0	40	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
$\overline{RAS}$ Precharge Time	t_{RP}	80	—	90	—	100	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	50	25	60	30	75	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	50	—	60	—	75	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	—	120	—	150	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	25	—	25	—	30	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	35	—	40	—	45	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	35	—	40	—	45	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	25	—	25	—	30	—	ns	8, 9
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	
$\overline{RAS}$ Pulse Width (Read-Modify-Write Cycle	t_{RWS}	170	10000	200	10000	245	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	85	—	100	—	125	—	ns	8
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CHR}	20	—	25	—	30	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	15	—	20	—	ns	
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	35	—	40	ns	
Output Buffer Turn-off Delay Referenced to $\overline{OE}$	t_{OFF2}	0	25	0	30	0	40	ns	
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	25	—	30	—	40	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	10	—	15	—	20	—	ns	

• Electrical Characteristics and Recommended AC Operating Conditions (continued)

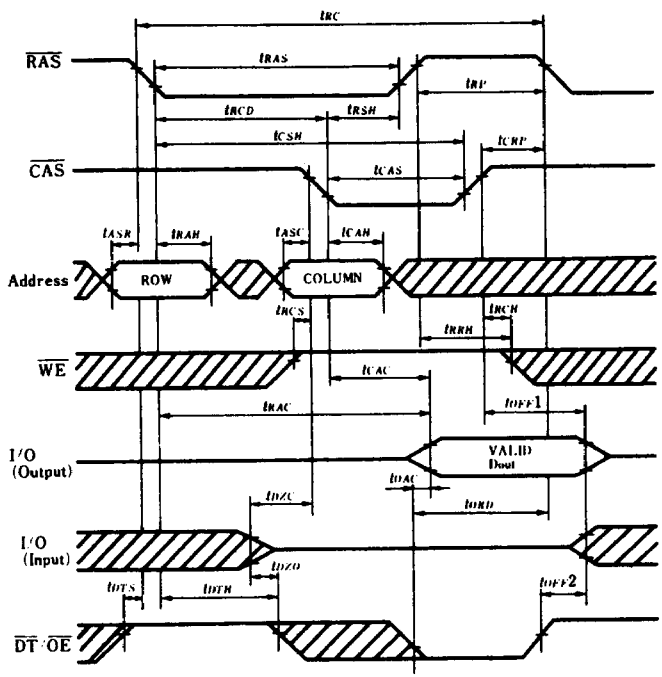
(T_A = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)[1, 10, 11]

Parameter	Symbol	HM53462-10		HM53462-12		HM53462-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Data-in to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	0	—	ns	
Data-in to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{OE}$ to $\overline{RAS}$ Delay Time	t_{ORD}	35	—	40	—	45	—	ns	
Serial Clock Cycle Time	t_{SCC}	40	—	40	—	60	—	ns	
Access Time from SC	t_{SCA}	—	40	—	40	—	60	ns	10
Access Time from $\overline{SOE}$	t_{SEA}	—	25	—	30	—	40	ns	10
SC Pulse Width	t_{SC}	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	ns	
Serial Data-out Hold Time after SC High	t_{SOH}	10	—	10	—	10	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{SOE}$	t_{SEZ}	0	25	0	25	0	30	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	25	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time (Read Transfer Cycle)	t_{RDH}	80	—	90	—	110	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	15	—	15	—	20	—	ns	
$\overline{DT}$ to $\overline{CAS}$ Hold Time	t_{CDH}	20	—	30	—	45	—	ns	
Last SC to $\overline{DT}$ Delay Time	t_{SDD}	5	—	5	—	10	—	ns	
First SC to $\overline{DT}$ Hold Time	t_{SDH}	25	—	25	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Delay Time	t_{DTR}	10	—	10	—	10	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	20	—	ns	
I/O to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	ns	
I/O to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	20	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	75	ns	
SC to $\overline{RAS}$ Setup Time	t_{SRS}	30	—	40	—	45	—	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	—	30	—	35	—	ns	
Serial Data Input Delay Time from $\overline{RAS}$	t_{SID}	50	—	60	—	75	—	ns	
Serial Data Input to $\overline{DT}$ Delay Time	t_{SZD}	0	—	0	—	0	—	ns	
$\overline{SOE}$ to $\overline{RAS}$ Setup Time	t_{ES}	0	—	0	—	0	—	ns	
$\overline{SOE}$ to $\overline{RAS}$ Hold Time	t_{EH}	15	—	15	—	20	—	ns	
Serial Write Enable Setup Time	t_{SWS}	0	—	0	—	0	—	ns	
Serial Write Enable Hold Time	t_{SWH}	35	—	35	—	55	—	ns	
Serial Write Disable Setup Time	t_{SWIS}	0	—	0	—	0	—	ns	
Serial Write Disable Hold Time	t_{SWIH}	35	—	35	—	55	—	ns	
$\overline{DT}$ to Sout in Low-Z Delay Time	t_{DLZ}	5	—	10	—	10	—	ns	

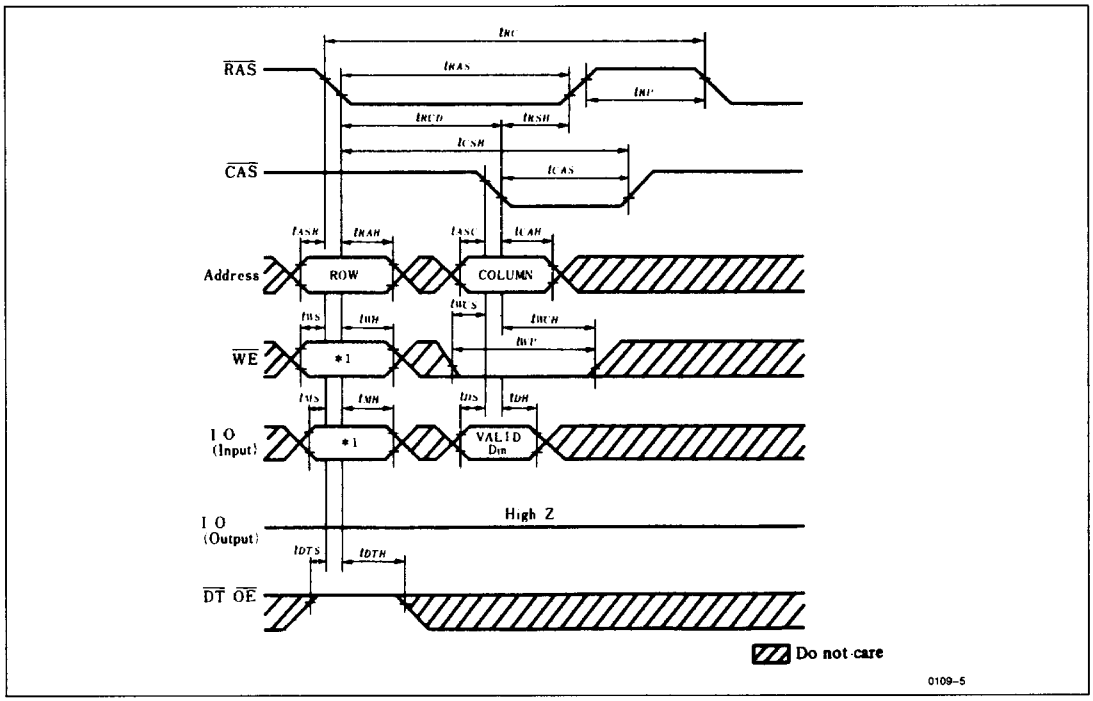
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WC}, and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycle and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. Measured with a load circuit equivalent to 2 TTL and 100 pF.
11. After power-up, pause for more than 100 μs and execute at least 8 initialization cycles. Then execute at least one logic reset cycle including write mask reset (on the falling edge of $\overline{RAS}$, $\overline{WE}$ = "Low" and I/O_I–I/O = "High"), and execute one or more transport cycle for initiation of SAM port.

■ TIMING WAVEFORMS

• Read Cycle

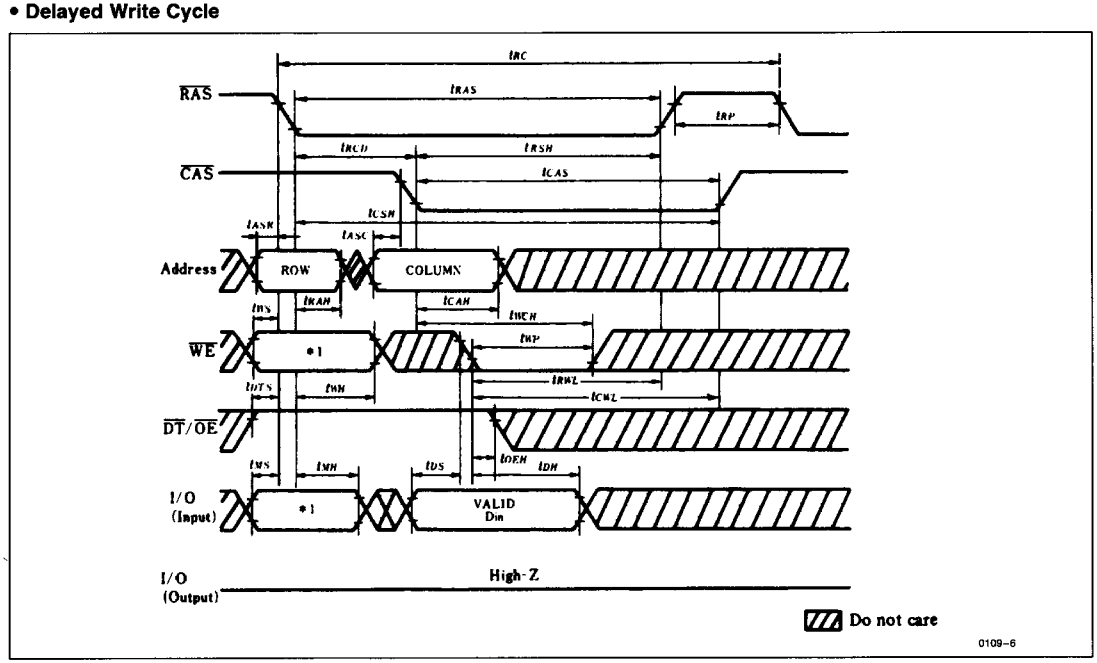


• **Early Write Cycle**



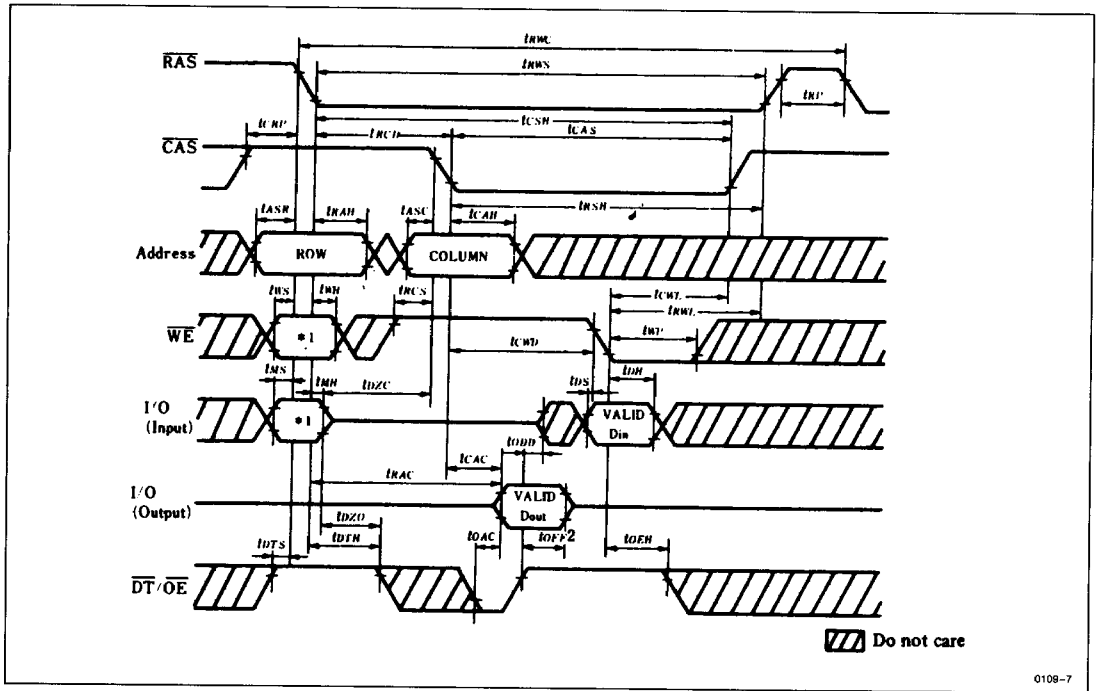
Notes: *1. When $\overline{WE}$ is "H" level, then all data on the I/O can be written into the cell. When $\overline{WE}$ is "L" level, the data on the I/O are not written except for when I/O is "H" level at the falling edge of $\overline{RAS}$.

• **Delayed Write Cycle**



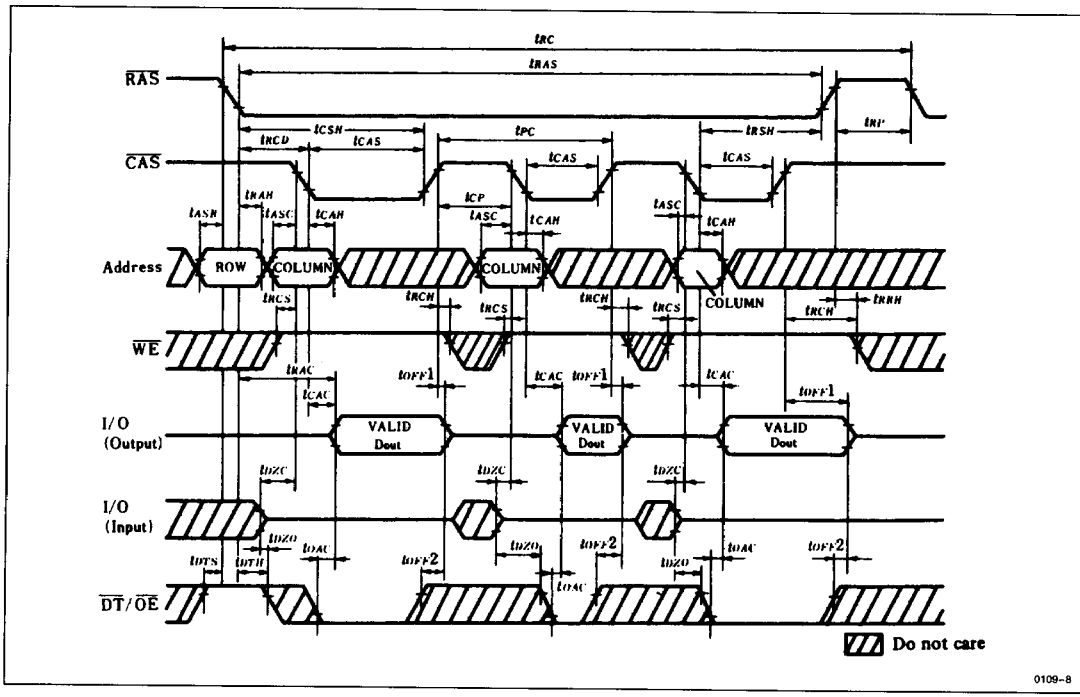
Note: *1. When $\overline{WE}$ is "H" level, all the data on I/O_1–I/O_4 can be written into the memory cell. When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

• **Read-Modify-Write Cycle**

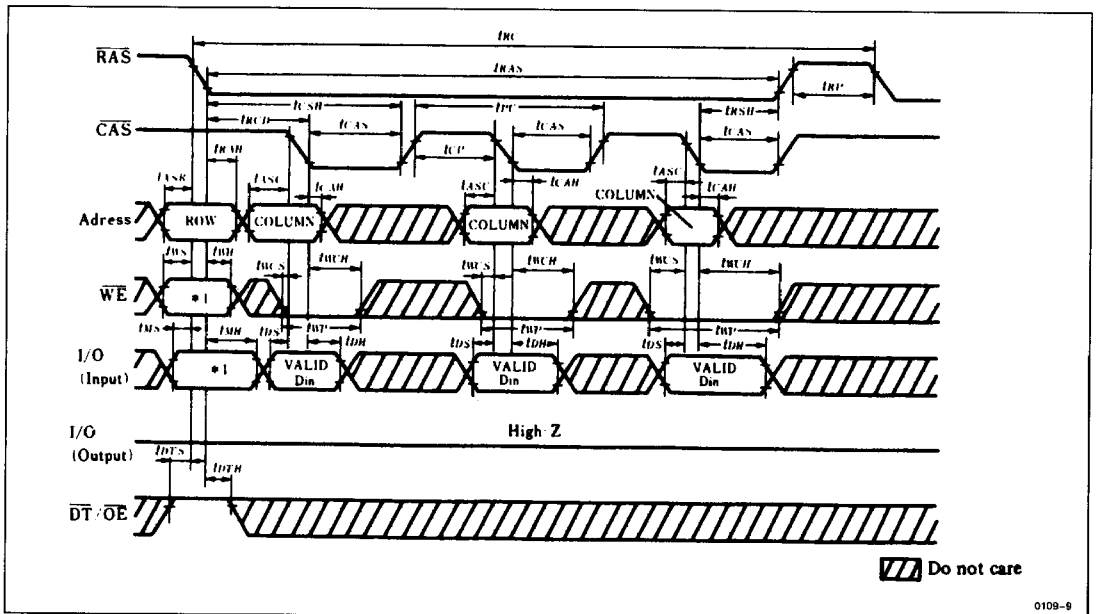


Note: *1. When $\overline{WE}$ is "H" level, all the data on I/O_1–I/O_4 can be written into the memory cell. When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

• **Page Mode Read Cycle**

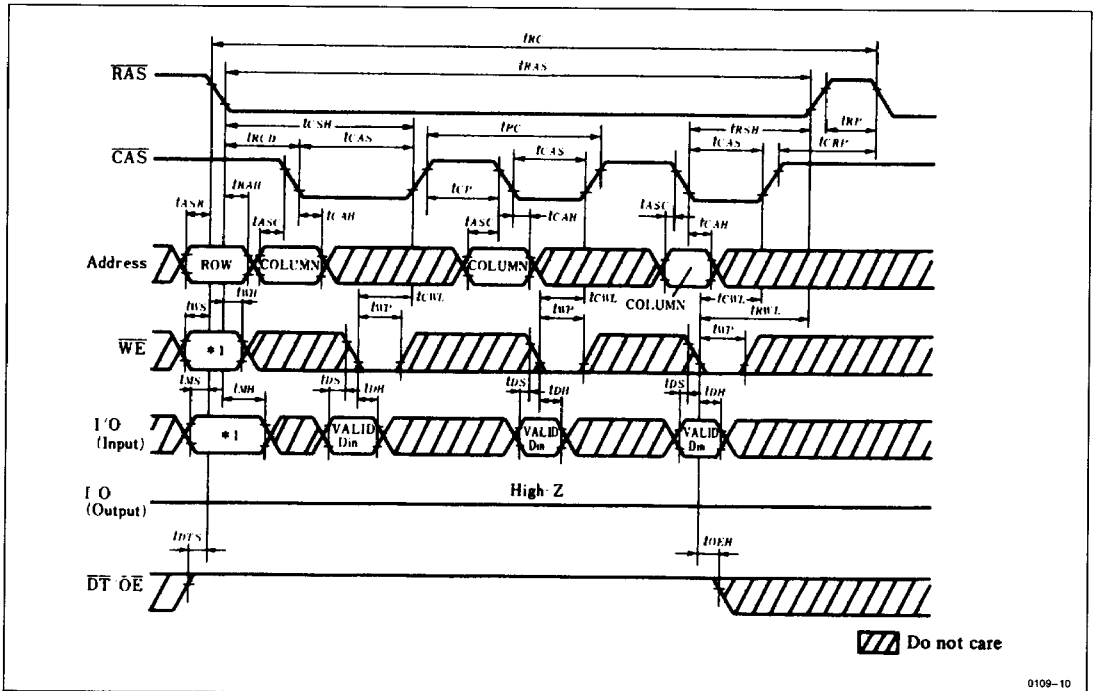


• **Page Mode Write Cycle (Early Write)**



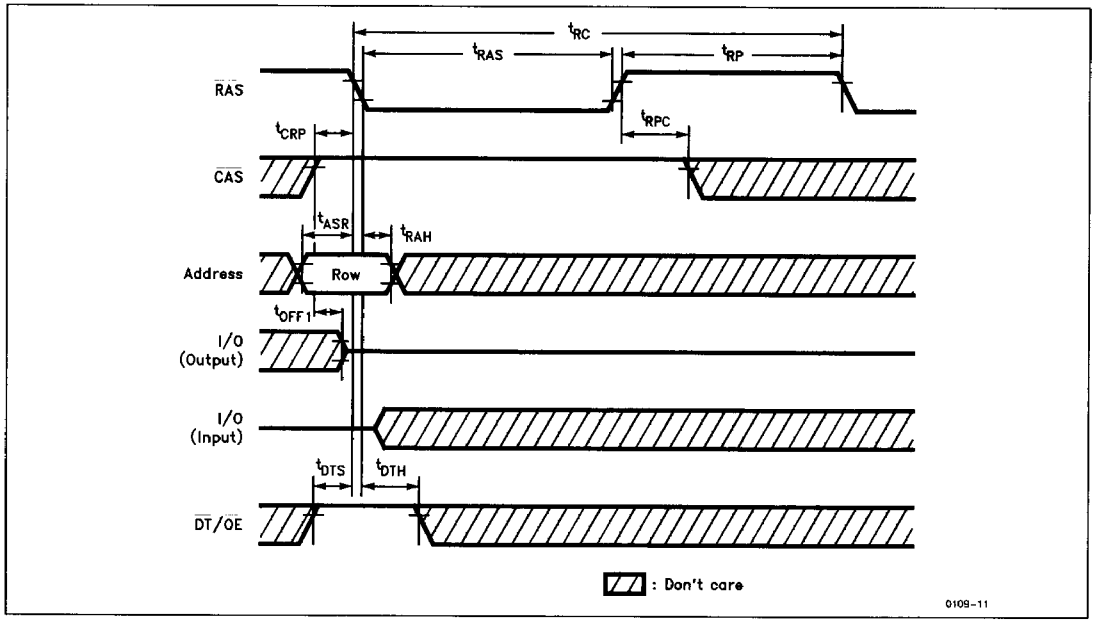
Note: *1. When $\overline{WE}$ is "H" level, all the data on I/O_1–I/O_4 can be written into the memory cell. When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

• **Page Mode Write Cycle (Delayed Write)**

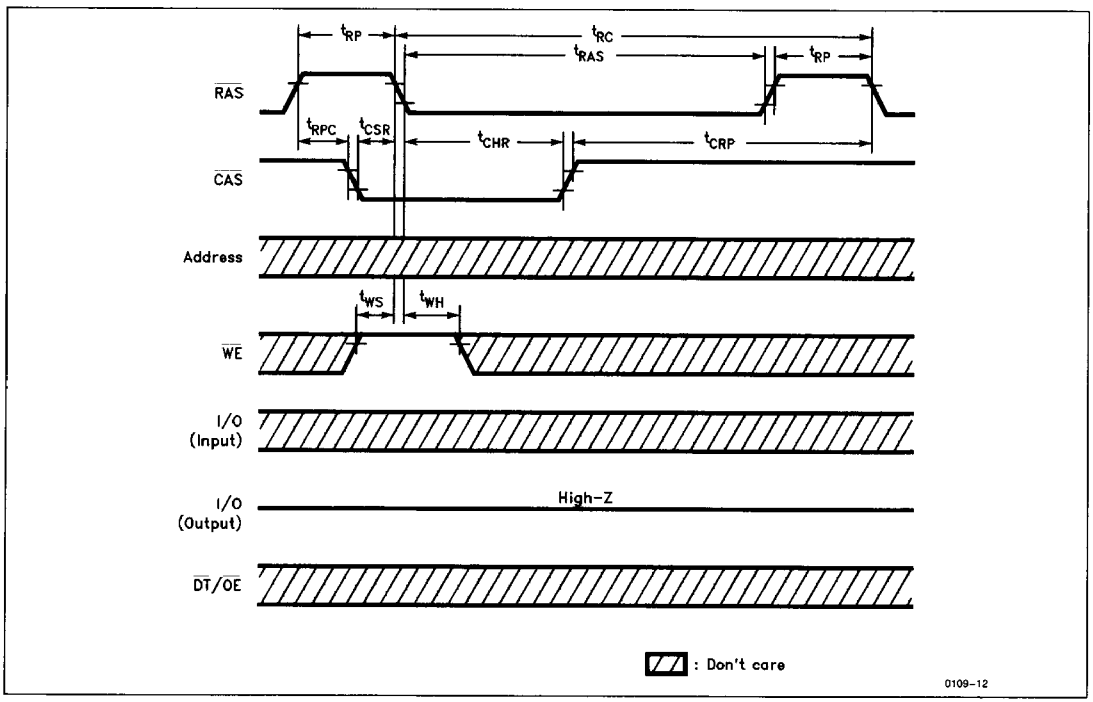


Note: *1. When $\overline{WE}$ is "H" level, all the data on I/O_1–I/O_4 can be written into the memory cell. When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

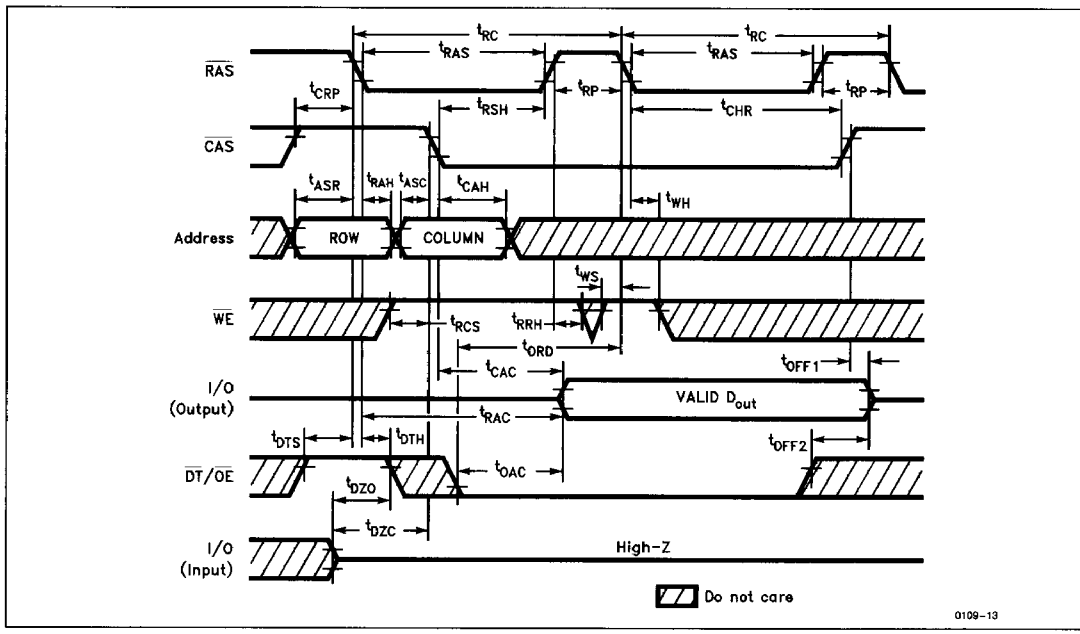
• $\overline{RAS}$ Only Refresh Cycle



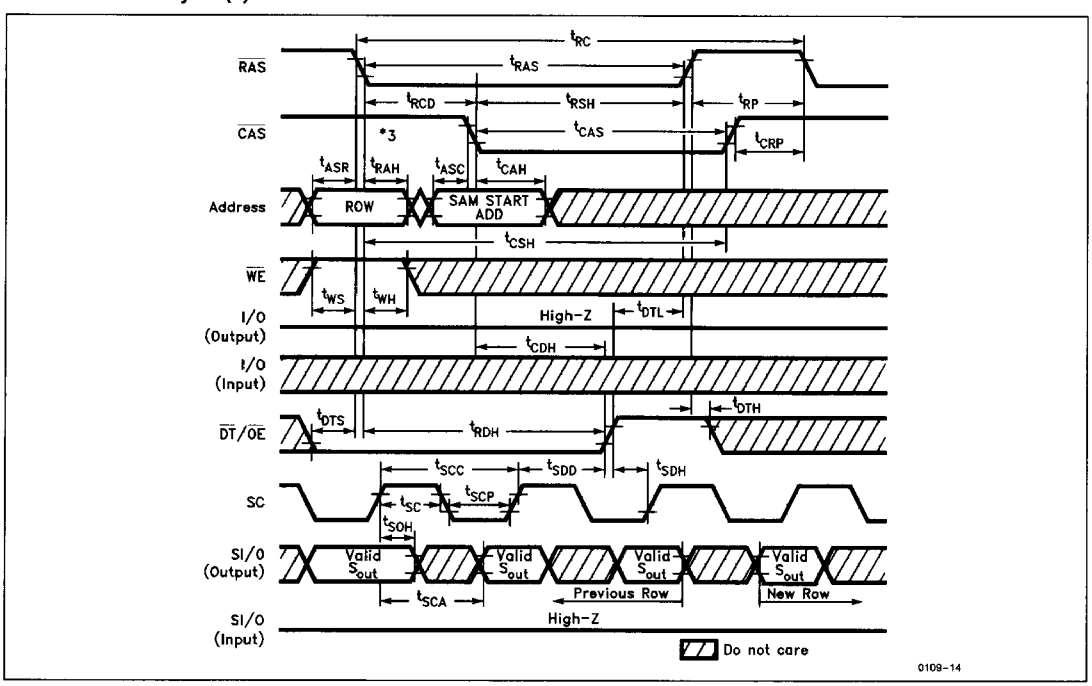
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• **Hidden Refresh Cycle**

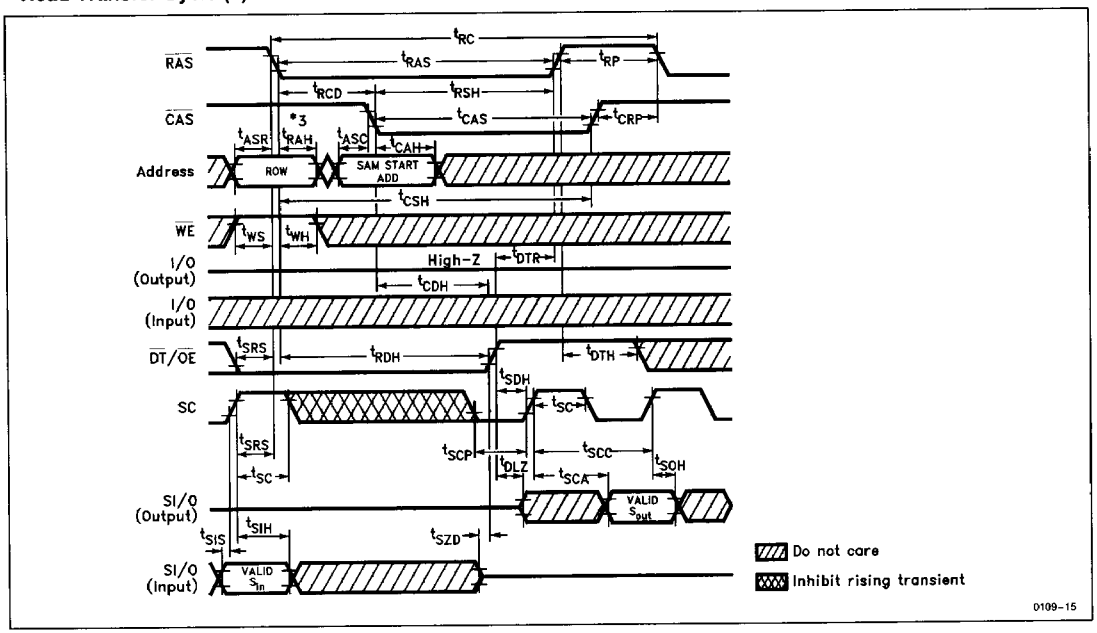


• **Read Transfer Cycle (1)*1, *2**



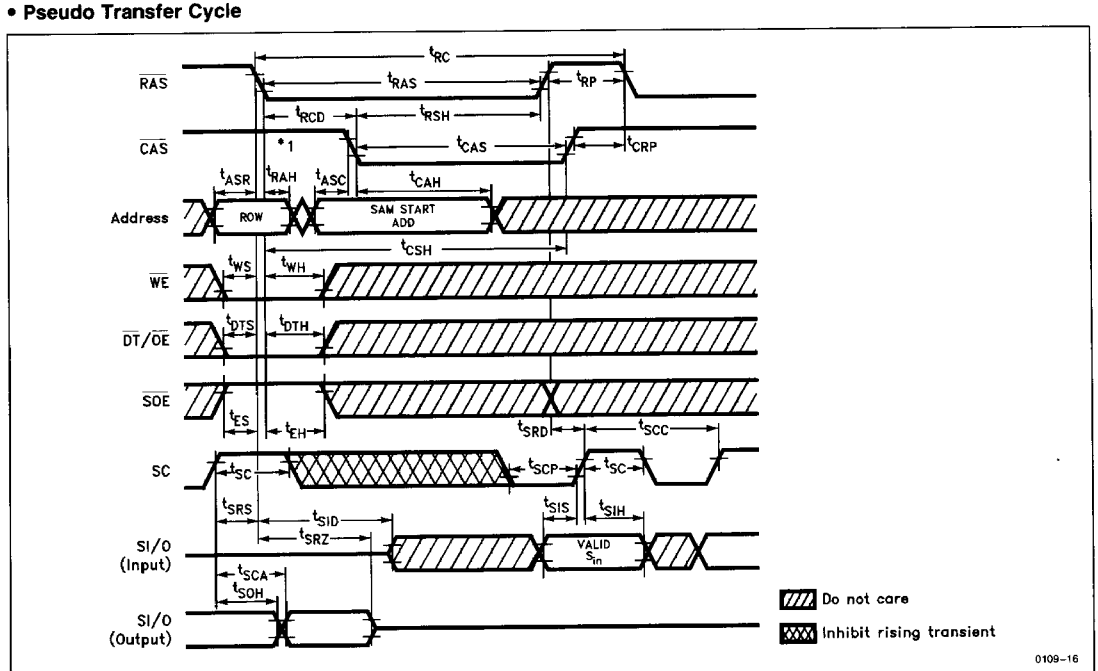
Notes: *1. In the case that the previous data transfer cycle was read transfer.
*2. Assume that $\overline{SOE}$ is "Low".
*3. $\overline{CAS}$ and SAM start Address need not be supplied every cycle, only when it is desired to change to a new SAM start Address.

• **Read Transfer Cycle (2)*1, *2**



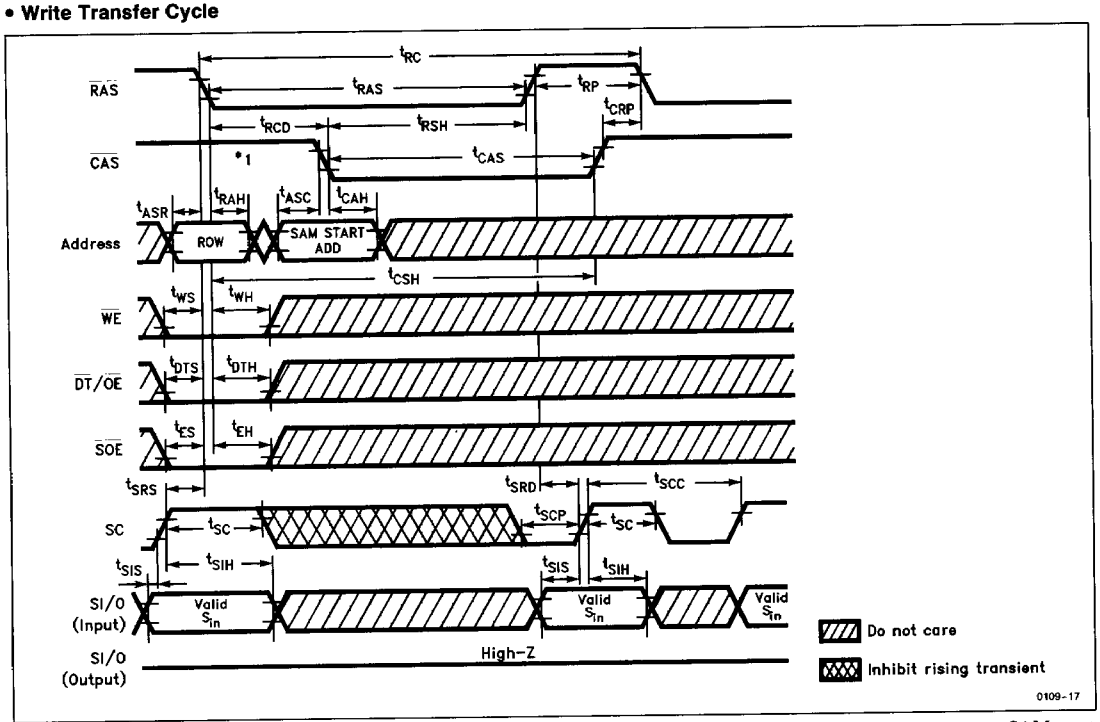
Notes: *1. In the case that the previous data transfer cycle was read transfer.
*2. Assume that $\overline{SOE}$ is "Low".
*3. $\overline{CAS}$ and SAM start Address need not be supplied every cycle, only when it is desired to change to a new $\overline{SAM}$ start Address.

• **Pseudo Transfer Cycle**



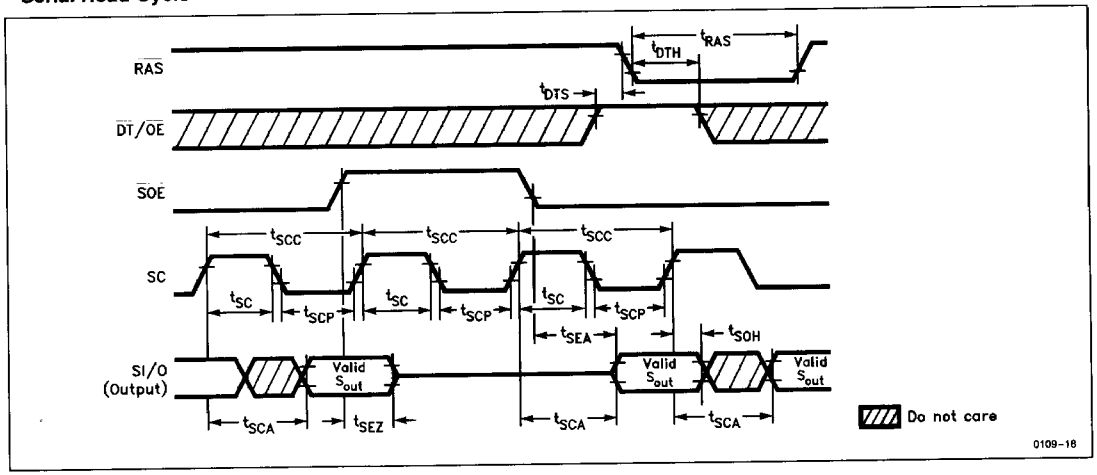
Note: *1. $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• **Write Transfer Cycle**

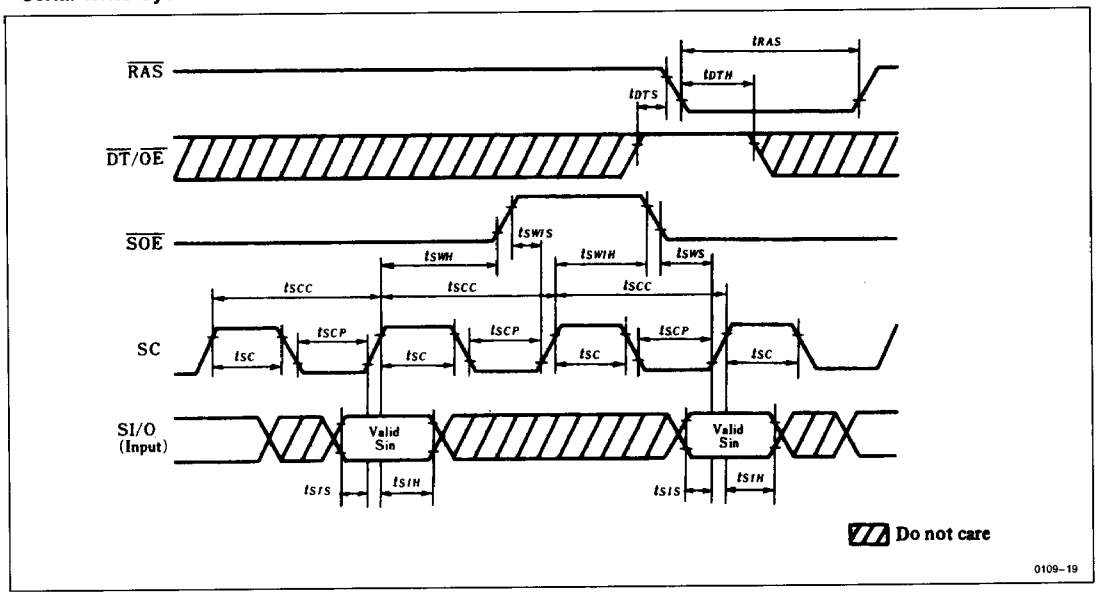


Note: *1. $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• **Serial Read Cycle**



• **Serial Write Cycle**



• **Electrical AC Characteristics** (Logic Operation Mode)

Parameter	Symbol	HM53462-10		HM53462-12		HM53462-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{FRC}	230	—	265	—	310	—	ns	
$\overline{RAS}$ Pulse Width in Write Cycle	t_{RFS}	140	10000	165	10000	200	10000	ns	
$\overline{CAS}$ Pulse Width in Write Cycle	t_{CFS}	80	10000	95	10000	105	10000	ns	
$\overline{CAS}$ Hold Time in Write Cycle	t_{FCSH}	140	—	165	—	200	—	ns	
$\overline{RAS}$ Hold Time in Write Cycle	t_{FRSH}	80	—	95	—	105	—	ns	
Page Mode Cycle Time (Write Cycle)	t_{FPC}	100	—	120	—	135	—	ns	
$\overline{CAS}$ Hold Time (Logic Operation Set/Reset Cycle)	t_{FCHR}	90	—	100	—	120	—	ns	
$\overline{CAS}$ Hold Time from $\overline{RAS}$ Precharge (x4 → x1 Set Cycle)	t_{PSCH}	10	—	10	—	10	—	ns	

• **Logic Code** (FC0–3 are AX0–AX3 in Logic Operation Set Cycle)

FC3	FC2	FC1	FC0	LOGIC	
				Symbol	Write Data
0	0	0	0	0	Zero
0	0	0	1	AND1	Di•Mi
0	0	1	0	AND2	$\overline{Di}$•Mi
0	0	1	1	X4 → X1	—
0	1	0	0	AND3	Di•$\overline{Mi}$
0	1	0	1	THROUGH	Di
0	1	1	0	EOR	$\overline{Di}$•Mi + Di•$\overline{Mi}$
0	1	1	1	OR1	Di + Mi
1	0	0	0	NOR	$\overline{Di}$•$\overline{Mi}$
1	0	0	1	ENOR	Di•Mi + $\overline{Di}$•$\overline{Mi}$
1	0	1	0	INV1	$\overline{Di}$
1	0	1	1	OR2	$\overline{Di}$ + Mi
1	1	0	0	INV2	$\overline{Mi}$
1	1	0	1	OR3	Di + $\overline{Mi}$
1	1	1	0	NAND	$\overline{Di}$ + $\overline{Mi}$
1	1	1	1	1	ONE

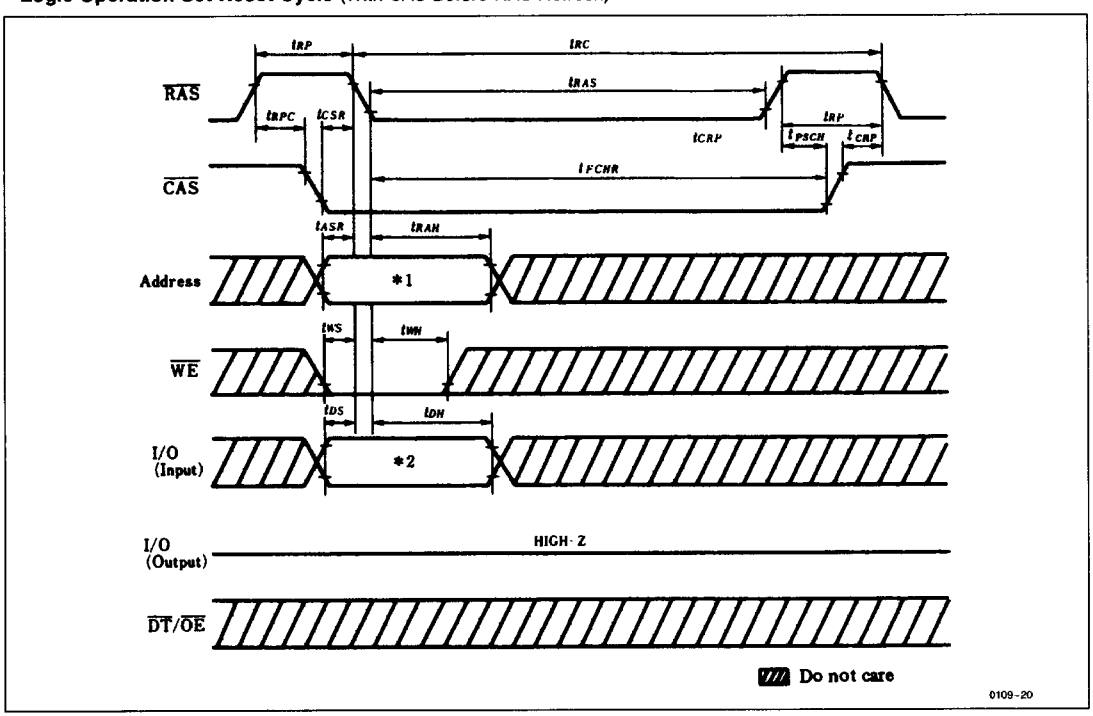
→ SAM Organization Changes to 1024 x 1

→ Logic Operation Mode Reset

Di :External Data-in

Mi :The Data of the Memory Cell

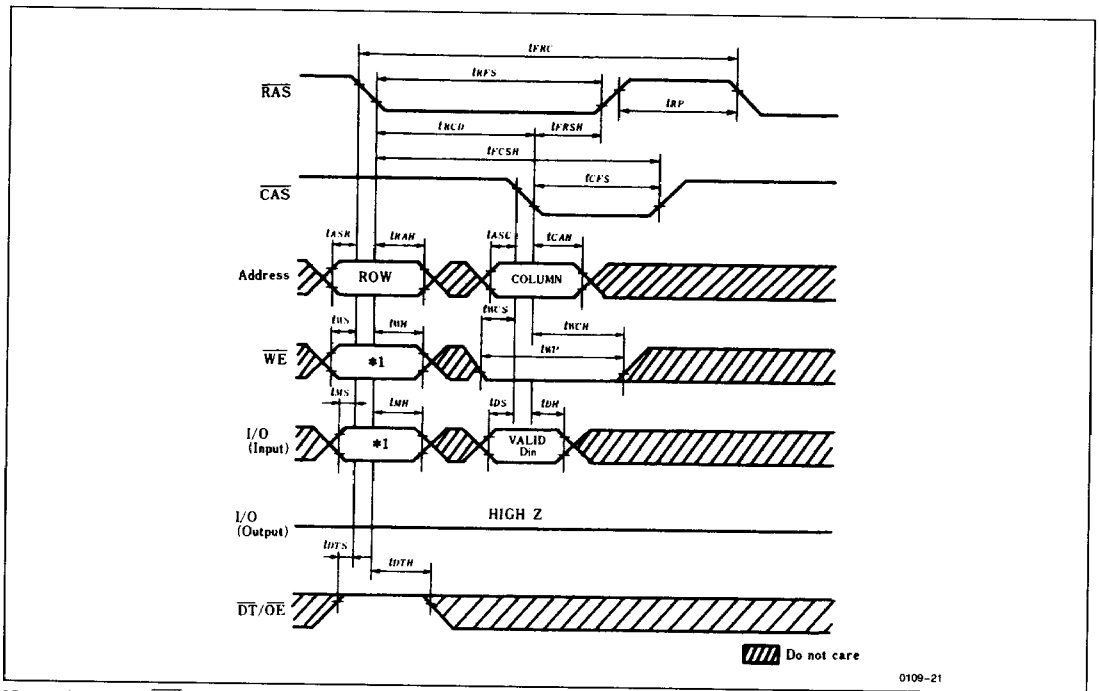
• **Logic Operation Set Reset Cycle** (With $\overline{CAS}$ Before $\overline{RAS}$ Refresh)



Notes: *1. Logic code A_0–A_3 (A_4–A_7: don't care)
*2. Write mask data.

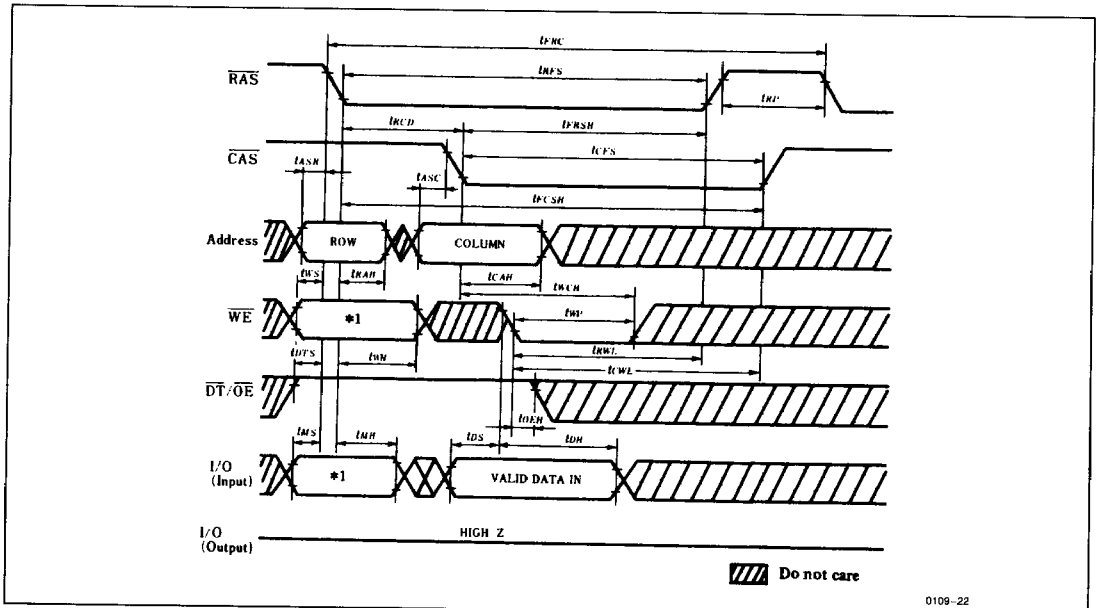
■ LOGIC OPERATION MODE

• Early Write Cycle



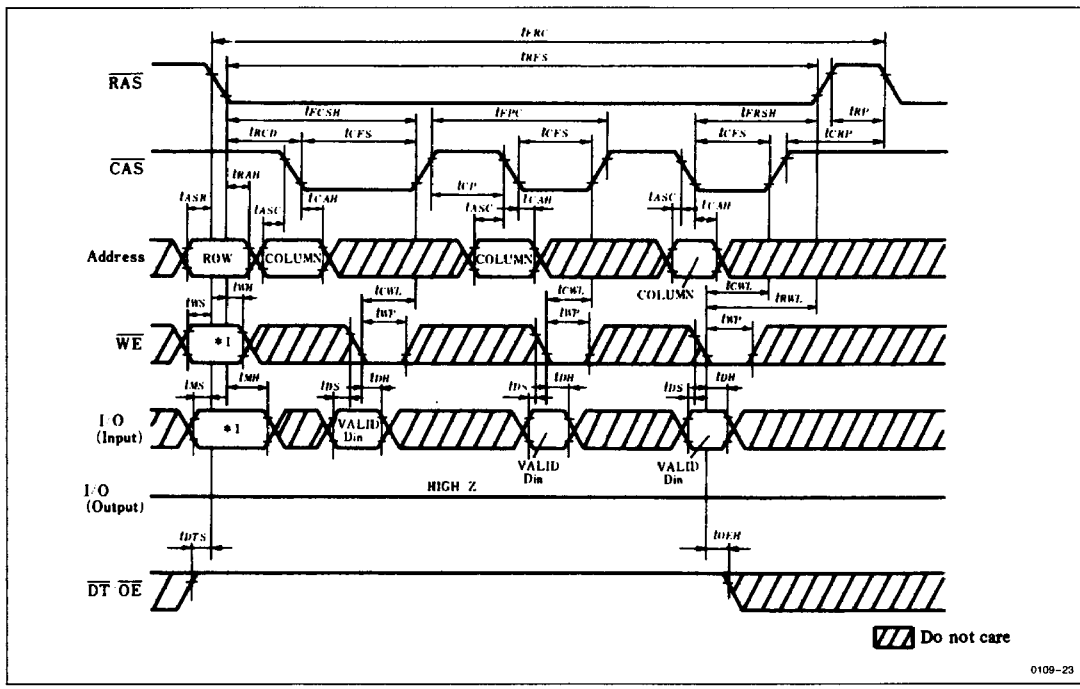
Note: *1. When $\overline{WE}$ is "high", the all data on the I/O can be written into the cell. When $\overline{WE}$ is "low", the data on the I/O are not written except for when I/O is "high" at the falling edge of $\overline{RAS}$.

• Delayed Write Cycle



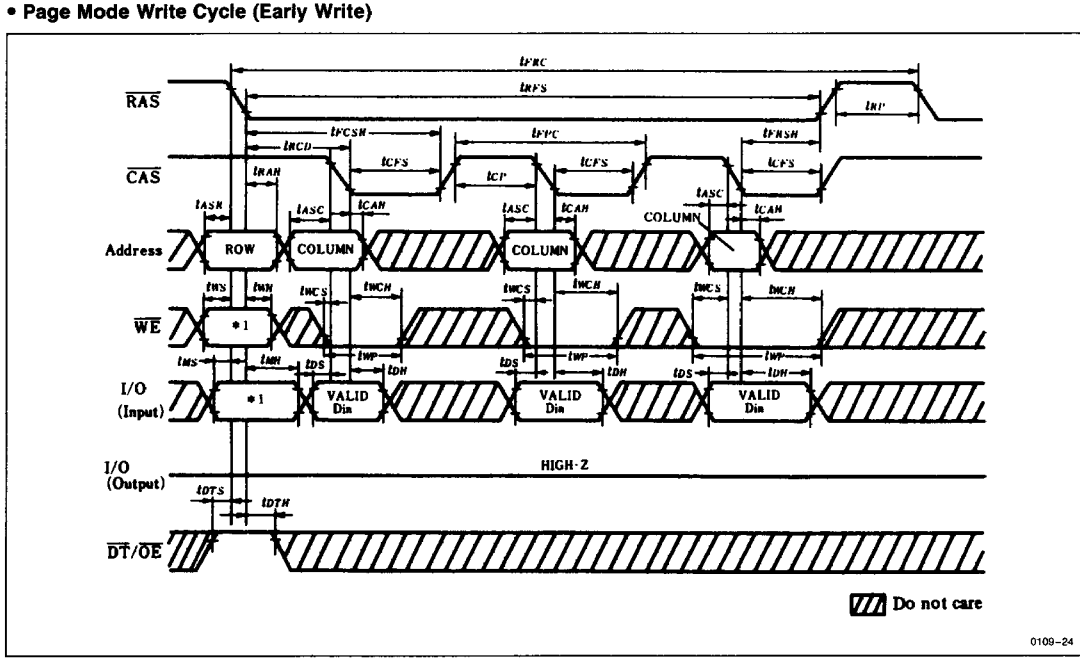
Note: *1. When $\overline{WE}$ is "H" level, all the data on I/O_{1-4} can be written into the memory cell. When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

• **Page Mode Write Cycle** (Delayed Write)



Note: *1. When $\overline{WE}$ is "high", the all data on the I/O can be written into the cell. When $\overline{WE}$ is "low", the data on the I/O are not written except for when I/O is "high" at the falling edge of $\overline{RAS}$.

• **Page Mode Write Cycle (Early Write)**



Note: *1. When $\overline{WE}$ is "high", the all data on the I/O can be written into the cell. When $\overline{WE}$ is "low", the data on the I/O are not written except for when I/O is "high" at the falling edge of $\overline{RAS}$.

■ DESCRIPTION

1. LOGIC OPERATION MODE

HM53462 has an internal logic operation unit which makes a process of graphics simple. The logic is determined in "Logic operation set/reset cycle", and the operation is executed in every write cycle succeeding to the logic operation set/reset cycle. In this mode the internal read-modify-write operation is executed and the cell data is converted into the new data given by the logic operation between D_{in} and the old cell data.

2. LOGIC OPERATION SET/RESET CYCLE

A logic operation set/reset cycle is performed by bringing $\overline{CAS}$ and $\overline{WE}$ low when $\overline{RAS}$ falls (Fig. 1). The logic code and the bits to be masked are determined respectively by AX0–3 state and I/O_{1-4} state at the falling edge of $\overline{RAS}$. Furthermore, in this cycle $\overline{CAS}$ before $\overline{RAS}$ refresh operation is executed, too. In this case of executing the conventional $\overline{CAS}$ before $\overline{RAS}$ refresh operation, $\overline{WE}$ must be high when $\overline{RAS}$ falls.

2.1 Logic Code

The logic code is shown in Table 1. When power is turned on, at least one logic reset cycle including write mask reset is required to initialize logic code. If the logic code is (AX3, AX2, AX1, AX0) = (0, 0, 1, 1), the SAM organization is changed converter (Fig. 2). In the case that the SAM organization is changed to 1024 x 1, one data transfer cycle is needed to initialize the SAM selector.

One the SAM organization is changed to 1024 x 1, this code is maintained unless power is turned off.

2.2 Write Mask

HM53462 has two kinds of mask registers (register 1, 2). The register 1 is set by bringing $\overline{WE}$ low at the falling edge of $\overline{RAS}$ during the write cycle, and the mask data is available only in this cycle. The register 2 is set by level of I/O in the logic operation set/reset cycle, and the mask data is available until the next logic operation set/reset cycle. If the register 1 is set during the current logic operation mode, the mask data of the register 1 is preferred (that of the register 2 is ignored) and the logic becomes "THROUGH" only in this cycle (Fig. 3).

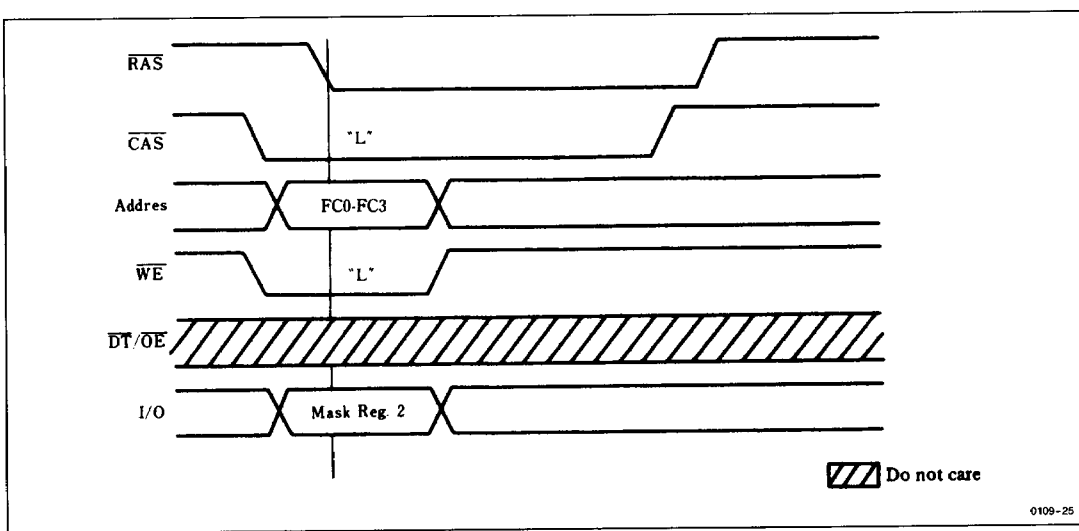


Figure 1. Logic Operation Set/Reset Cycle

• Table 1. Logic Code (FC0–FC3 are AX0–AX3 in Logic Operation Set Cycle)

FC3	FC2	FC1	FC0	LOGIC	
				Symbol	Write Data
0	0	0	0	0	Zero
0	0	0	1	AND1	Di•Mi
0	0	1	0	AND2	$\overline{Di}$•Mi
0	0	1	1	X4 → X1	—
0	1	0	0	AND3	Di•$\overline{Mi}$
0	1	0	1	THROUGH	Di
0	1	1	0	EOR	$\overline{Di}$•Mi + Di•$\overline{Mi}$
0	1	1	1	OR1	Di + Mi
1	0	0	0	NOR	$\overline{Di}$•$\overline{Mi}$
1	0	0	1	ENOR	Di•Mi + $\overline{Di}$•$\overline{Mi}$
1	0	1	0	INV1	$\overline{Di}$
1	0	1	1	OR2	$\overline{Di}$ + Mi
1	1	0	0	INV2	$\overline{Mi}$
1	1	0	1	OR3	Di + $\overline{Mi}$
1	1	1	0	NAND	$\overline{Di}$ + $\overline{Mi}$
1	1	1	1	1	ONE

→ SAM Organization Changes to 1024 x 1

→ Logic Operation Mode Reset

Di :External Data-in

Mi :The Data of the Memory Cell

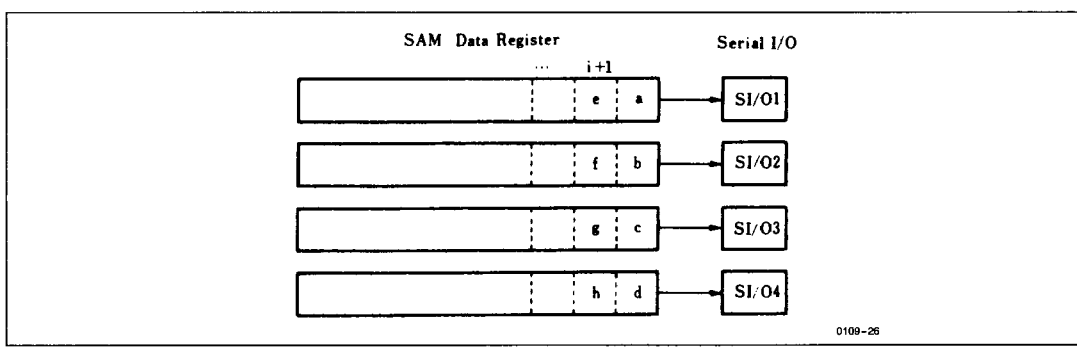
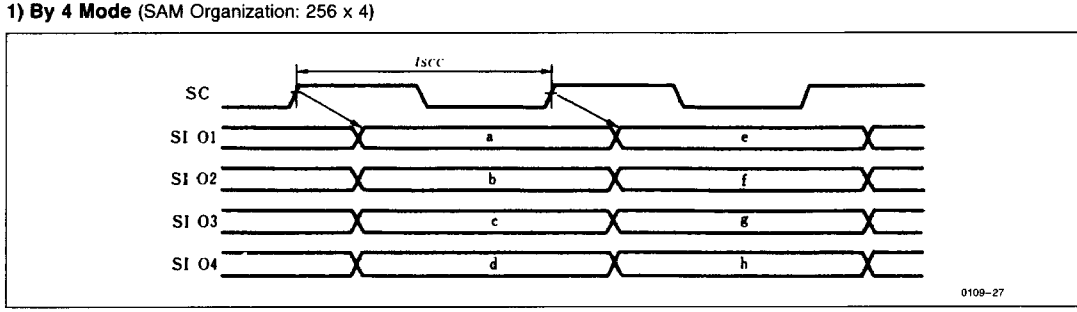
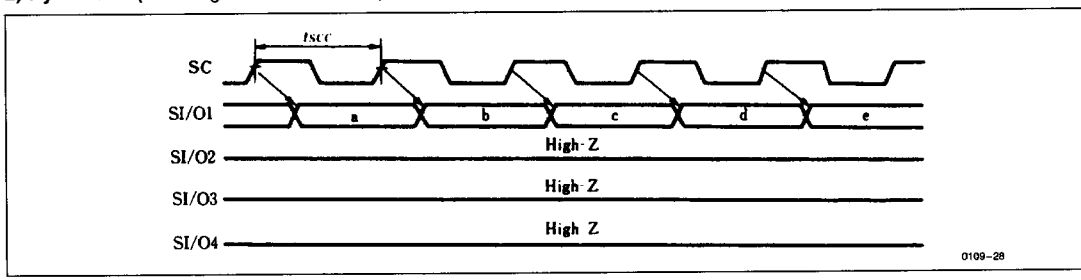


Figure 2. The Shift Way of SAM Data

1) By 4 Mode (SAM Organization: 256 x 4)



2) By 1 Mode (SAM Organization: 1024 x 1)



	Logic operation set/reset cycle	Write cycle	Write cycle	Write cycle	Write cycle
$\overline{RAS}$					
$\overline{CAS}$	"L"	"H"	"H"	"H"	"H"
$\overline{WE}$	"L"	"H"	"L"	"H"	"H"
I/O1		"0" Write	Masked	"1" Write	"0" Write
I/O2		Masked	"1" Write	Masked	Masked
I/O3		Masked	"0" Write	Masked	Masked
I/O4		"1" Write	Masked	"0" Write	"1" Write
Logic	—	AND1	THROUGH	AND1	AND1
	Mask reg.2 is set I O2,3 :Masked Assume that the logic is set to "AND1".		Mask reg.1 is set, and valid only in this cycle. I O1,4:Masked		

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Figure 3. Example of Logic Operation Mode