SONY

CXA1474M/N

Low Current Consumption FM IF Amplifier for Pagers

Description

The CXA1474M/N is a low current consumption FM IF amplifiers which employ the newest bipolar process. It is suitable for such sets as Japan single conversion pagers which require low current consumption.

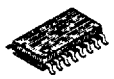
Features

- Low current consumption 920 µA (typ. at Vcc=1.5V)
- Low voltage operation Vcc=1.0 to 4.0V
- Few external parts for needless of IF decoupling capacitor
- Built-in reference power supply for operational amplifier and comparator
- Small package 16-pin VSOP

Functions

- Second IF and limiter amplifiers
- FM detector
- Quaternary LPF operational amplifier
- FSK comparator
- Regulator output for RF amplifier and first mixer
- Power-save function
- Low voltage detection circuit

CXA1474M
16 pin SOP (Plastic)



CXA1474N
16 pin VSOP (Plastic)

Applications

Single super pagers for Japan and overseas

Absolute Maximum Ratings (Ta=25℃)

• Supply voltage	Vcc	12.0	V
• Operating temperature	Topr	–20 to +75	℃
• Storage temperature	Tstg	–65 to +150	℃

Operating Condition

Supply voltage	Vcc	1.0 to 4.0	V

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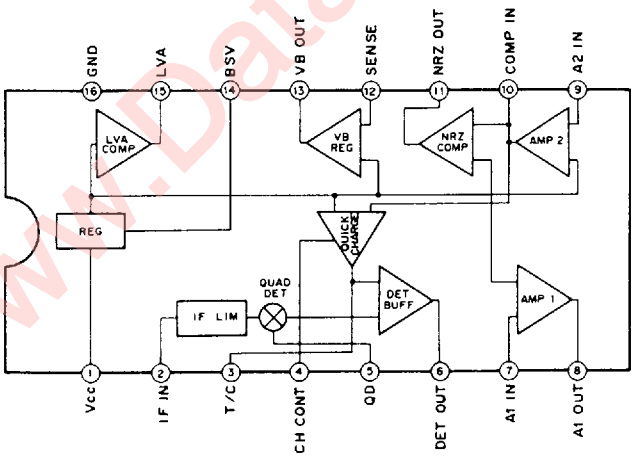
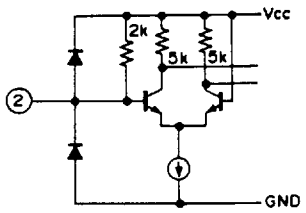
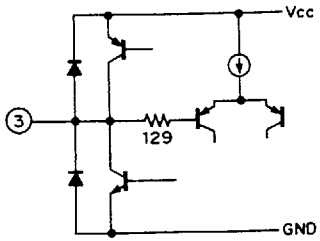
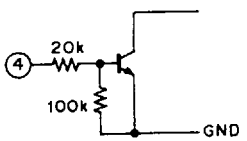
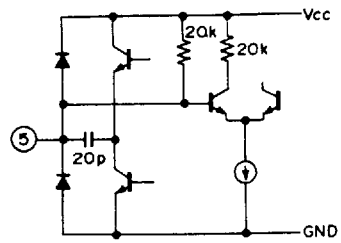
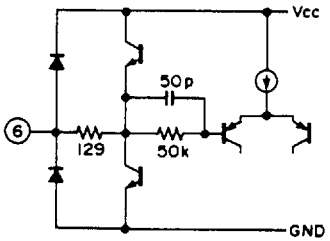
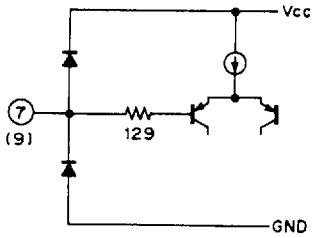
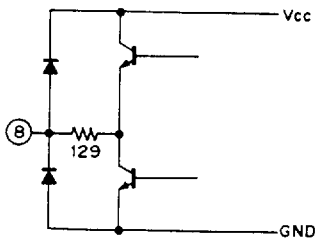
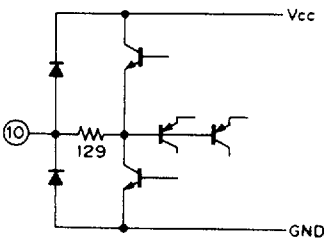
Block Diagram



Pin Description

Pin No	Symbol	Pin voltage	Equivalent circuit	Description
1	Vcc			Vcc
2	IF IN	1.5V		IF limiter amplifier input.
3	T/C	0.2V		Connects a capacitor that determines the low cut-off frequency for the entire system.
4	CH CONT	0V		Controls the ON/OFF operation of the quick-charge circuit. (Input voltage range: −0.5 to +7.0V)
5	QD	1.5V		Connects to the phase shifter of FM detector circuit.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
6	DET OUT	0.2V		FM detector output.
7 9	A1 IN A2 IN	0.2V 0.2V		Input for operational amplifier 1 and 2 (AMP1, AMP2).
8	A1 OUT	0.2V		Output for operational amplifier 1 (AMP1).
10	COMP IN	0.2V		NRZ comparator input. Output for operational amplifier 2 (AMP2) is output.

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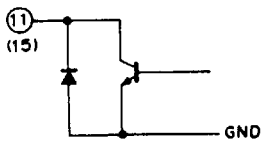
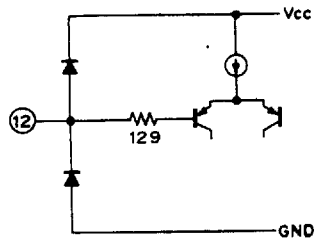
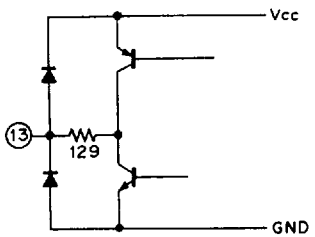
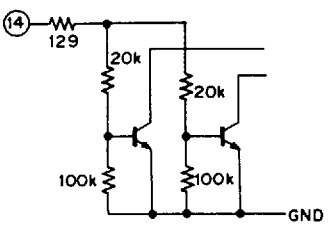
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
11 15	NRZ OUT LVA OUT	— —		NRZ and LVA comparator outputs and are open collectors. (Applied voltage range −0.5 to +7.0V)
12	SENSE	0.2V		Input pin for internal constant-voltage source amplifier. This pin is controlled to maintain 200mV.
13	VB OUT	—		Output pin for internal constant-voltage source amplifier. Connect the base of PNP transistor. (Current capacity: 200 μA)
14	BSV	—		Controls battery saving. Setting this pin low suspends the operation of IC. (Input voltage range: −0.5 to +7.0V)
16	GND	—		GND

Electrical Characteristics

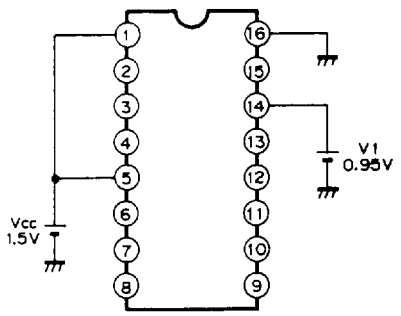
(Vcc=1.5V, Ta=25°C, Fs=455kHz, FMOD=256Hz, FDEV=2.3kHz, AMMOD=30%)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	Icc	Test circuit 1	700	920	1200	μA
Current consumption	Iccs	Test circuit 1, V1=0.3V			20	μA
AM rejection ratio	AMRR	Test circuit 3, VIN=60dBμ	25			dB
Op amp. input bias current	IBIAS	Test circuit 2		40	100	nA
Op amp. open loop gain	Av	Test circuit 4	45	60		dB
Op amp. output voltage amplitude	Vo	Test circuit 5	0.65			Vp-p
NRZ output saturation voltage	VSATNRZ	Test circuit 8			0.4	V
NRZ output leak current	ILNRZ	Test circuit 7			5.0	μA
NRZ hysteresis width	VTWNRZ	Test circuit 6	5	10	17	mV
VB output current	IOUT	—			200	μA
VB output saturation voltage	VSATVB	Test circuit 9			0.4	V
VB SENSE voltage	VSENVB	—	205	215	225	mV
LVA operating voltage	VLVA	Test circuit 10	1.10	1.15	1.20	V
LVA hysteresis	VTHLVA	Test circuit 10	10	50	100	mV
LVA output leak current	ILLVA	Test circuit 10			5.0	μA
LVA output saturation voltage	VSATLVA	Test circuit 8			0.4	V
Detector output voltage	VODET	Test circuit 3	16	20	28	mV
Logic input voltage high level	VTHBSV		0.9			V
Logic input voltage low level	VTLBSV				0.35	V
Limiting sensitivity	VIN (LIM)	Test circuit 3		17	24	dBμ

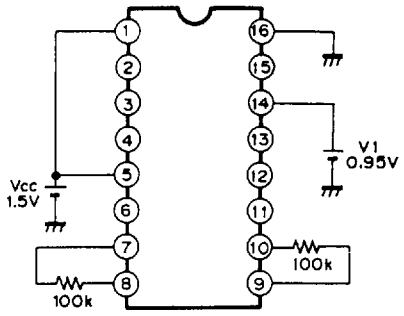
Design Data

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
IF limiter input resistance	RINLIM		1.6	2.0	2.4	kΩ
IF limiter gain stability	GSLIM		−6		+6	dB
DET OUT output resistance	ROUTDET				200	Ω
Op amp. maximum input voltage		Vcc=1.1V	0.39			V
Op amp. minimum input voltage					0.05	V
Comparator maximum input voltage		Vcc=1.1V	0.39			V
Comparator minimum input voltage					0.05	V
Op amp. offset voltage					3.0	mV

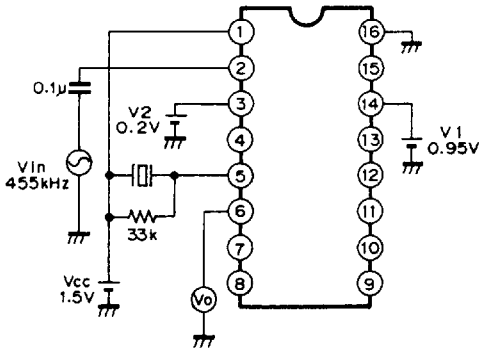
Test Circuit



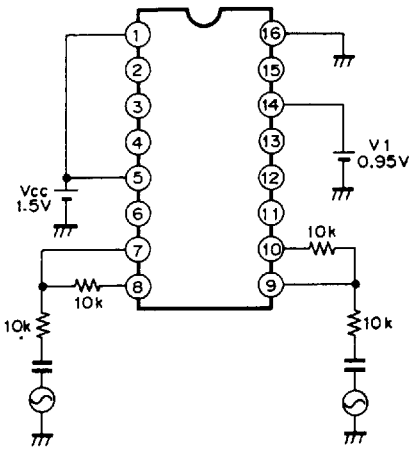
Test circuit 1



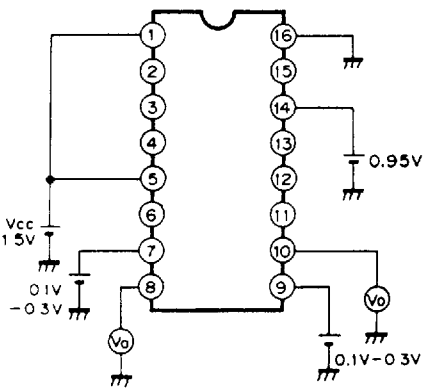
Test circuit 2



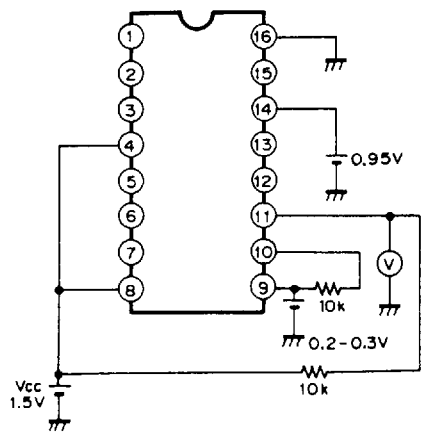
Test circuit 3



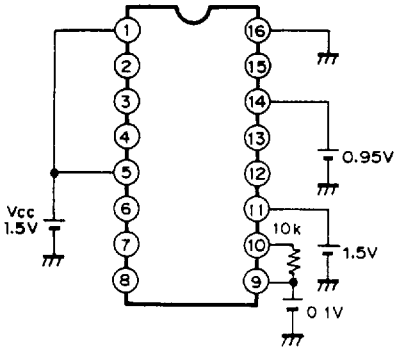
Test circuit 4



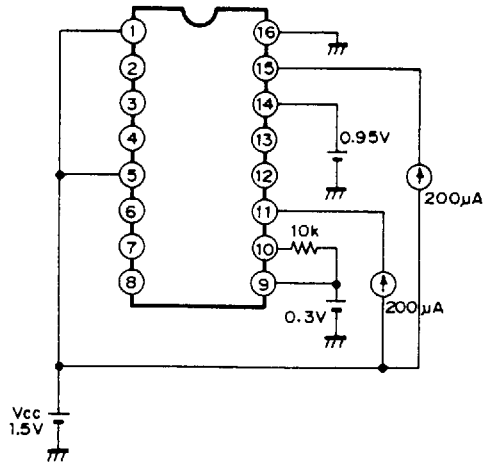
Test circuit 5



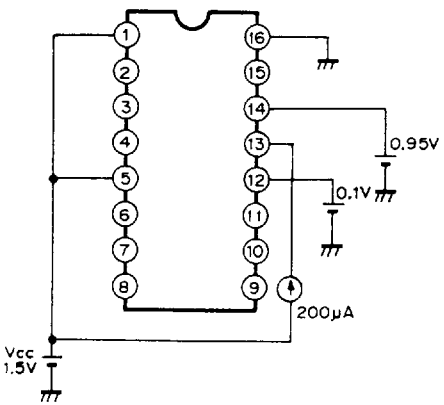
Test circuit 6



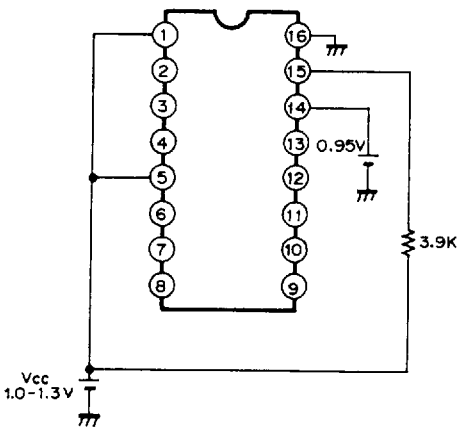
Test circuit 7



Test circuit 8



Test circuit 9



Test circuit 10

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1) Power Supply

The CXA1474M/N, with built-in regulator, is designed to permit stable operation at wide range of supply voltage from 1.0 to 4.0V. Decouple the wiring to Vcc (Pin 1) as close to the pin as possible.

2) IF Filter

The filter to be connected between IF limiters should have the following specifications.

Input impedance : 2.0kΩ ± 10%
Band width : Changes according to applications

3) IF Limiter Amplifier

The gain of this IF limiter amplifier is approximately 100dB so that, note that the following points about wiring to the IF limiter amplifier input pin (Pin 2).

a) Be sure to wire to the IF limiter amplifier input (Pin 2) as short as possible.

b) As the IF limiter amplifier output appears at QD (Pin 5), be sure to wire to the RLC and ceramic discriminator connected to QD as short as possible and reduce the interference on the mixer output and IF limiter amp input.

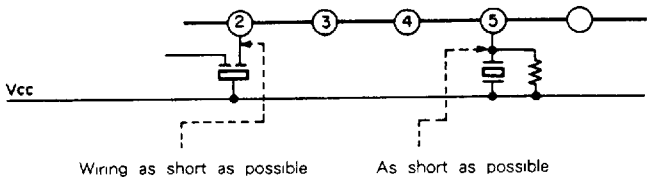
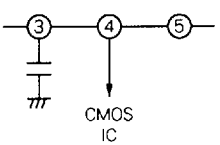


Fig. 1

4) Quick Charge

In order to hasten the rising time from when power is turned on or when reception standby, the CXA1474M/N features a quick charge circuit.
Therefore, the quick charge circuit eliminates the need to insert capacitor between the detector output and the LPF as is the case with conventional ICs, but connects capacitor to Pin 3 to determine the average signal level during steady-state reception.
Connect a signal for controlling the quick charge circuit to Pin 4. Setting this pin high enables the quick charge mode, setting this pin low enables the steady-state reception mode.
Connect Pin 4 to GND when quick charge is not being used.



5) Detector

The detector is a quadrature type. To perform phase shift, connect RLC resonator circuit or ceramic discriminator to Pin 5.
The phase shifting capacitor for the quadrature detector is built in.
This detector attenuates the high frequency components of the demodulated FM (FSK) signal with the internal CR-constructed LPF, and outputs it to DET OUT (Pin 6).
DET OUT output impedance is 200Ω or less.

The CDBM455C25 (MURATA MFG. CO., LTD.) ceramic discriminator for the CXA1474M is recommended.

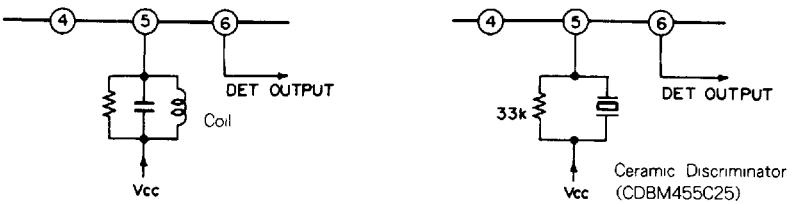


Fig. 3

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6) AMP, NRZ OUT

Two operational amplifiers are built in this IC.
One of them is connected internally to an NRZ comparator.

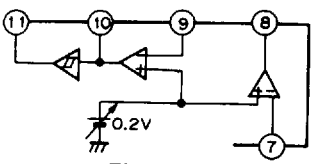


Fig. 4

Using these two operational amplifiers to construct an LPF, remove noise from the demodulated signal and input to the NRZ comparator, which is the next stage.
The NRZ comparator molds waveform of this input signal and outputs it as a square wave. The NRZ comparator output stage is for open collector.
Thus, if the CPU is a CMOS-type and the supply voltage is different, a direct interface as illustrated in the figure below can be implemented.

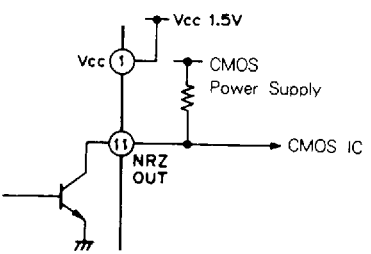


Fig. 5

7) VB SENSE, VB OUT

Controls the base bias of the external transistors.

8) LVA OUT

This pin goes high (open) when the supply voltage becomes low. Since the output is an open collector, it can be used to directly drive CMOS device as can NRZ OUT. The setting voltage of the LVA is 1.15V (typ.), and it possesses a hysteresis with respect to the supply voltage. The hysteresis width is 50mV (typ.).

9) BSV

Operation of the CXA1474M/N can be halted by setting this pin low. This pin also can be connected directly to CMOS device. Also, the current consumption for BSV is 20 μA or less (at 1.5V).

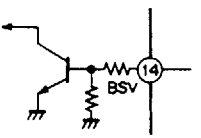


Fig. 6

Principle of Quick Charge Operation

BUF in Fig. 7 is the detector buffer amplifier, and AMP1 and AMP2 are operational amplifiers to construct LPF. COMP is the NRZ comparator. Coupling on conventional system is performed by placing a capacitor between the detector buffer and the LPF operational amplifier, matching of DC is not performed . Thus, this matching capacitor must be charged when restoring the system from reception standby mode to reception mode, within which time signals from the comparator appear at the NRZ output.
To shorten this rise time, as shown in Fig. 7 the CXA1474 adds feedback loop from the comparator input to the input circuit of output. This equalizes the average value of the comparator input voltage to the reference voltage, with the quick charge circuit of CHG being set inside the feedback loop. Switching the current of quick change circuit enables reduction of the rise time.
In this block, CHG is comparator which compares the input voltage and outputs current based on this comparison The current on CHG is switched between high and low at Pin 4. To shorten the time constant when switching from reception standby mode to reception mode, switch the current to high and increase the charge current at C in Fig 7. During steady-state reception mode, switch the current to low, lengthening the charge time constant, and allowing for stable data retrieval.

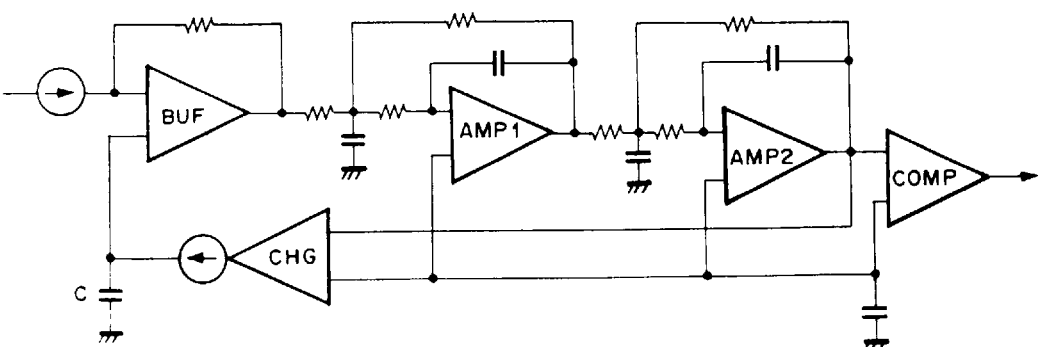
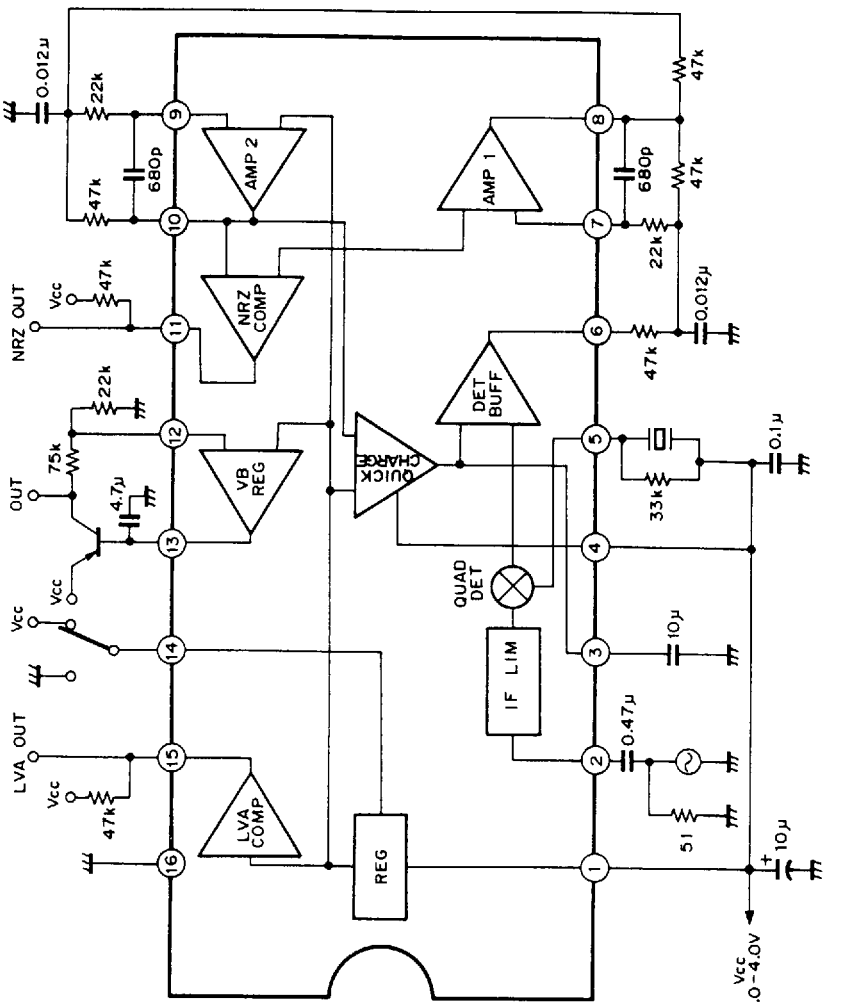


Fig. 7

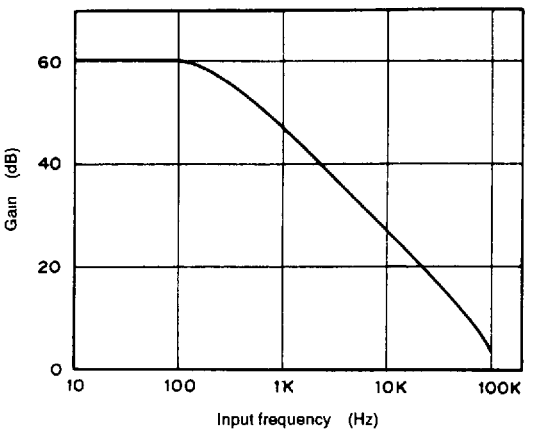
Application Circuit



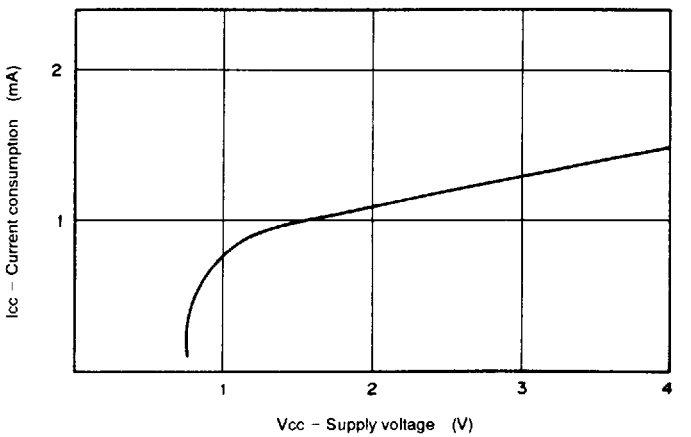
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same

Example of Representative Characteristics

Input frequency vs. Gain

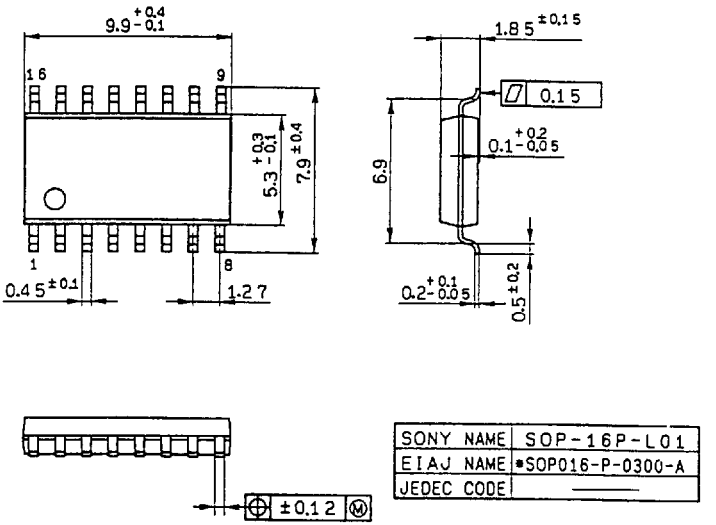


Supply voltage vs. Current consumption



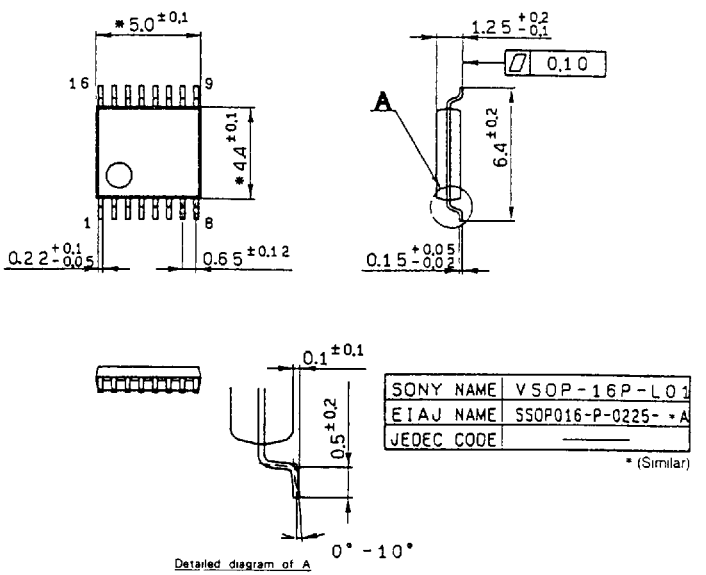
Package Outline Unit : mm

CXA1474M 16pin SOP (Plastic) 300mil 0.2g



SONY NAME	SOP-16P-L01
EIAJ NAME	*SOP016-P-0300-A
JEDEC CODE	———

CXA1474N 16pin VSOP (Plastic) 225mil

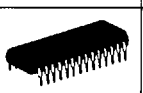
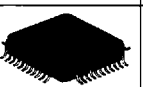
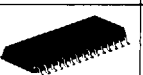
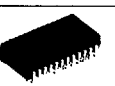


SONY NAME	VSOP-16P-L01
EIAJ NAME	SSOP016-P-0225-*A
JEDEC CODE	———

* (Similar)

Note) Dimensions marked with * does not include resin residue.

Package Name

Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	DIP	DUAL IN-LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		SIP	SINGLE IN LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		ZIP	ZIG ZAG IN-LINE PACKAGE		P	2.54mm (100MIL) Zig-Zag in-line	Through Hole Lead	1-direction
		PGA	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	Package under side
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN-LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction
		SZIP	SHRINK ZIG-ZAG IN-LINE PACKAGE		P	1.778mm (70MIL) Zig-Zag in-line	Through Hole Lead	1-direction
Surface mounted	Standard flat package	QFP	QUAD FLAT L LEADED PACKAGE		P C	1.0mm 0.8mm 0.65mm	Gull-Wing	4-direction
		SOP	SMALL OUTLINE L-LEADED PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Standard 2-direction chip carrier	SOJ	SMALL OUTLINE J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull-Wing	2-direction
		TSOP	THIN SMALL OUTLINE PACKAGE		P	0.5mm (0.55mm)	Gull-Wing	2-direction
	Standard chip carrier	QFJ	QUAD FLAT J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	4-direction
		QFN	QUAD FLAT NON-LEADED PACKAGE		C	1.27mm (50MIL)	Leadless	Package under side

*P·····Plastic, C·····Ceramic